RK3288 IO LIST

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V1.0	2013.04.29	第一版	LX

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0			Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
Part A								
AA23	LCDC0_HSYNC/GPIO1_D0	I/O	down	I	LCDC0_HSYNC	LCDC horizontal sync signal output		LCDC0
AB24	LCDC0_VSYNC/GPIO1_D1	I/O	down	I	LCDC0_VSYNC	LCDC vertical sync signal output		
AA22	LCDC0_DEN/GPIO1_D2	I/O	down	I	LCDC0_DEN	LCDC data enable		
AA24	LCDC0_DCLK/GPIO1_D3	I/O	down	I	LCDC0_DCLK	LCDC pixel clk output		
T27	TRACE_D0/LCDC0_D0/LVDS_D0P	A			LCDC0_D0	LCDC data port	LVDS_D0P	LVDS
T28	TRACE_D1/LCDC0_D1/LVDS_D0N	A			LCDC0_D1	LCDC data port	LVDS_D0N	
U27	TRACE_D2/LCDC0_D2/LVDS_D1P	A			LCDC0_D2	LCDC data port	LVDS_D1P	
U28	TRACE_D3/LCDC0_D3/LVDS_D1N	A			LCDC0_D3	LCDC data port	LVDS_D1N	
W27	TRACE_D4/LCDC0_D4/LVDS_D2P	A			LCDC0_D4	LCDC data port	LVDS_D2P	
W28	TRACE_D5/LCDC0_D5/LVDS_D2N	A			LCDC0_D5	LCDC data port	LVDS_D2N	
Y27	TRACE_D6/LCDC0_D6/LVDS_D3P	A			LCDC0_D6	LCDC data port	LVDS_D3P	
Y28	TRACE_D7/LCDC0_D7/LVDS_D3N	A			LCDC0_D7	LCDC data port	LVDS_D3N	
AA27	TRACE_D8/LCDC0_D8/LVDS_D4P	A			LCDC0_D8	LCDC data port	LVDS_D4P	
AA28	TRACE_D9/LCDC0_D9/LVDS_D4N	A			LCDC0_D9	LCDC data port	LVDS_D4N	
V27	TRACE_D10/LCDC0_D10/LVDS_CLK0P	A			LCDC0_D10	LCDC data port	LVDS_CLK0P	
V28	TRACE_D11/LCDC0_D11/LVDS_CLK0N	A			LCDC0_D11	LCDC data port	LVDS_CLK0N	
U25	TRACE_D12/LCDC0_D12/LVDS_D5P	A			LCDC0_D12	LCDC data port	LVDS_D5P	
U26	TRACE_D13/LCDC0_D13/LVDS_D5N	A			LCDC0_D13	LCDC data port	LVDS_D5N	
V25	TRACE_D14/LCDC0_D14/LVDS_D6P	A			LCDC0_D14	LCDC data port	LVDS_D6P	
V26	TRACE_D15/LCDC0_D15/LVDS_D6N	A			LCDC0_D15	LCDC data port	LVDS_D6N	
AA25	TRACE_CLK/LCDC0_D16/LVDS_D7P	A			LCDC0_D16	LCDC data port	LVDS_D7P	
AA26	TRACE_CTL/LCDC0_D17/LVDS_D7N	A			LCDC0_D17	LCDC data port	LVDS_D7N	
AB27	LCDC0_D18/LVDS_D8P	A			LCDC0_D18	LCDC data port	LVDS_D8P	
AB28	LCDC0_D19/LVDS_D8N	A			LCDC0_D19	LCDC data port	LVDS_D8N	
AC25	LCDC0_D20/LVDS_D9P	A			LCDC0_D20	LCDC data port	LVDS_D9P	
AC26	LCDC0_D21/LVDS_D9N	A			LCDC0_D21	LCDC data port	LVDS_D9N	
Y25	LCDC0_D22/LVDS_CLK1P	A			LCDC0_D22	LCDC data port	LVDS_CLK1P	
Y26	LCDC0_D23/LVDS_CLK1N	A			LCDC0_D23	LCDC data port	LVDS_CLK1N	
V24	LVDS_EXTR	A			LVDS_EXTR	Reference current generate,connect a 2K%1 resistor to VSS.		
AA20	LVDS_AVDD_1V0	AP			LVDS_AVDD_1V0	LVDS power supply		
AB21	LVDS_AVDD_1V8	AP			LVDS_AVDD_1V8	LVDS power supply		
AB23	LVDS_AVDD_3V3	AP			LVDS_AVDD_3V3	LVDS power supply		
Part B								
AG7	JTAG_TMS/SDMMC0_D0/GPIO6_C0	I/O	up	I	SDMMC0_D0	SDMMC0 data port	TMS	
AH6	JTAG_TRSTn/SDMMC0_D1/GPIO6_C1	I/O	up	I	SDMMC0_D1	SDMMC0 data port	TRSTN	

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AD8	JTAG_TDI/SDMMC0_D2/GPIO6_C2	I/O	up	I	SDMMC0_D2	SDMMC0 data port	TDI	SDMMC0
AB9	JTAG_TCK/SDMMC0_D3/GPIO6_C3	I/O	up	I	SDMMC0_D3	SDMMC0 data port	TCK	
AG6	JTAG_TDO/SDMMC0_CLKOUT/GPIO6_C4	O	down	O	SDMMC0_CLKO	SDMMC0 clock output	TDO	
AC8	SDMMC0_CMD/GPIO6_C5	I/O	up	I	SDMMC0_CMD	SDMMC0 command output		
AH5	SDMMC0_DET/GPIO6_C6	I/O	up	I	SDMMC0_DET	SDMMC0 detect input		
AC9	SDMMC0_VDD	P			SDMMC0_VDD	SDMMC0 digital IO power supply		
Part C								
Y23	HOST_D0/TS_D0/CIF_D2/GPIO2_A0	I/O	down	I	CIF_D0	Camera data port	HSADC_D0	DVP
Y21	HOST_D1/TS_D1/CIF_D3/GPIO2_A1	I/O	down	I	CIF_D1	Camera data port	HSADC_D1	
Y22	HOST_D2/TS_D2/CIF_D4/GPIO2_A2	I/O	down	I	CIF_D2	Camera data port	HSADC_D2	
V21	HOST_D3/TS_D3/CIF_D5/GPIO2_A3	I/O	down	I	CIF_D3	Camera data port	HSADC_D3	
U22	HOST_CKINP/TS_D4/CIF_D6/GPIO2_A4	I/O	down	I	CIF_D4	Camera data port	HSADC_D4	
U21	HOST_CKINN/TS_D5/CIF_D7/GPIO2_A5	I/O	down	I	CIF_D5	Camera data port	HSADC_D5	
U23	HOST_D4/TS_D6/CIF_D8/GPIO2_A6	I/O	down	I	CIF_D6	Camera data port	HSADC_D6	
V23	HOST_D5/TS_D7/CIF_D9/GPIO2_A7	I/O	down	I	CIF_D7	Camera data port	HSADC_D7	
R25	HOST_D6/TS_SYNC/CIF_VSYNC/GPIO2_B0	I/O	down	I	CIF_VSYNC	Camera vsync input	TS_SYNC	
R28	HOST_D7/TS_VALID/CIF_HREF/GPIO2_B1	I/O	down	I	CIF_HREF	Camera href input	TS_VALID	
V22	HOST_WKACK/GPS_CLK/TS_CLKOUT/CIF_CLKIN/GPIO2	I/O	down	I	CIF_CLKI	Camera clock input	TS_CLKOUT	
R22	HOST_WKREQ/TS_FAIL/CIF_CLKOUT/GPIO2_B3	I/O	down	I	CIF_CLKO	Camera clock output	TS_FAIL	
R27	CIF_D0/GPIO2_B4	I/O	down	I	CIF_PDN0	Camera power down control output for front	TV_PWR	
R26	CIF_D1/GPIO2_B5	I/O	down	I	CIF_PDN1	Camera power down control output for rear		
R24	CIF_D10/GPIO2_B6	I/O	down	I	CIF_RST0	Camera reset output for front	TV_RST	
R21	CIF_D11/GPIO2_B7	I/O	down	I	CIF_RST1	Camera reset output for rear		
P22	I2C3_SCL/GPIO2_C0	I/O	up	I	I2C3_SCL	I2C serial port 3,for camera,need external pull-up		
R23	I2C3_SDA/GPIO2_C1	I/O	up	I	I2C3_SDA	I2C serial port 3,for camera,need external pull-up		
U20	DVPIO_VDD	P	N/A		DVPIO_VDD	DVP digital IO power supply		
Part D								
M27	NPOR	I	up	I	NPOR	System reset input		MISC
P25	CLKIN_32K	I/O	down	I	CLKIN_32K	32KHz clock input		
P19	EFUSE_VQPS	P			EFUSE	EFUSE digital IO supply,default connect to VSS		
M26	TEST	I	down	I	TEST	Enter into test mode,default connect to VSS		
N27	OSC_XI	I	N/A	I	OSC_XI	Oscillator 24MHz clock input		PMU
N28	OSC_XO	O	N/A	O	OSC_XO	Oscillator 24MHz clock output		
P26	OSC_XVSS	G			OSC_XVSS	Oscillator analog power ground		
P28	PLL_AVDD_1V0	P			PLL_AVDD_1V0	PLL analog power supply		PLL
P27	PLL_AVSS	G			PLL_VSS	PLL analog power ground		
J28	GLOBAL_PWROFF/PMUGPIO0_A0	I/O	down	I	PMIC_SLEEP	PMIC sleep control output		

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J27	DDRIO_PWROFF/PMUGPIO0_A1	I/O	down	I	DDRIO_PWROFF	DDR IO power off control		PMU
J26	DDRIO0_RETEN/PMUGPIO0_A2	I/O	up	I	DDRIO_RETEN	DDR retention enable		
K27	DDRIO1_RETEN/PMUGPIO0_A3	I/O	up	I	EFUSE_PWR	EFUSE VPQS power control output		
K28	PMUGPIO0_A4	I/O	up	I	PMIC_INT	PMIC interrupt input		
L21	PMUGPIO0_A5	I/O	up	I	PWR_KEY	Power key detect input		
L22	PMUGPIO0_A6	I/O	up	I	HALL_INT	Hall sensor interrupt input	MAC_PWR	
L23	PMUGPIO0_A7	I/O	up	I	CHG_INT	Charge interrupt input		
L24	PMUGPIO0_B0	I/O	up	I	DC_DET	Adaptor insert detect input		
L25	PMUGPIO0_B1	I/O	up	I	CHG_DET	Charge status detect input		
L26	OTP_OUT/PMUGPIO0_B2	I/O	down	I	OT_RESET	Over-temperature protection reset power	PWR_HOLD	
L27	PMUGPIO0_B3	I/O	down	I	PHONE_CTL	Headphone out mute control		
M28	PMUGPIO0_B4	I/O	down	I	OTG_VBUS_DRV	USB OTG power control output		
L28	CLK27M_IN/PMUGPIO0_B5	I/O	down	I	CHG_CTL	Charge current control output		
M22	PMUGPIO0_B6	I/O	down	I	HOST_VBUS_DRV	USB HOST power control output		
M25	I2C0_SDA/PMUGPIO0_B7	I/O	up	I	I2C0_SDA_PMIC	I2C serial port 0,for PMIC and RTC,need external pull-up		
M21	I2C0_SCL/PMUGPIO0_C0	I/O	up	I	I2C0_SCL_PMIC	I2C serial port 0,for PMIC and RTC,need external pull-up		
M23	TEST_CLKO/CLK_27M_T1/PMUGPIO0_C1	I/O	down	I	DVP_PWR	DVP power control output	TEST_CLKO	
M24	PMUGPIO0_C2	I/O	up	I	USB_INT	USB insert detect input		
P20	PMUIO_VDD	P			PMUIO_VDD	PMU domain digital IO power		
M20	PMU_VDD_1V0	P			PMU_VDD_1V0	PMU domain logic power		
Part E								
A26	OTG_DM	A			OTG_DM	USB OTG Data Minus port		USB
B26	OTG_DP	A			OTG_DP	USB OTG Data Plus port		
C25	OTG_ID	A			OTG_ID	USB OTG ID detect input,need external pull-up		
D23	OTG_VBUS	A			OTG_DET	USB OTG connected detect input		
D21	OTG_EXTR	A			OTG_EXTR	USB OTG reference current generate,connect a 200ohm resistor to VSS.		
A23	HOST1_DM	A			HOST1_DM	USB HOST1 Data Minus port	No support USB1.1	
B23	HOST1_DP	A			HOST1_DP	USB HOST1 Data Plus port		
C23	HOST1_EXTR	A			HOST1_EXTR	USB HOST1 reference current generate,connect a 200ohm resistor to VSS.		
A22	HOST2_DM	A			HOST2_DM	USB HOST2 Data Minus port		
B22	HOST2_DP	A			HOST2_DP	USB HOST2 Data Plus port		
C21	HOST2_EXTR	A			HOST2_EXTR	USB HOST2 reference current generate,connect a 200ohm resistor to VSS.		
G18	USB_AVDD_1V0	AP			USB_AVDD_1V0	USB digital power supply		
E21	USB_AVDD_1V8	AP			USB_AVDD_1V8	USB analog power supply		
F20	USB_AVDD_3V3	AP			USB_AVDD_3V3	USB analog power supply		

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H18	USB_AVSS1	AG			USB_AVSS1	USB analog power ground		
C24	USB_AVSS2	AG			USB_AVSS2	USB analog power ground		
C26	USB_AVSS3	AG			USB_AVSS3	USB analog power ground		
B21	USB_AVSS4	AG			USB_AVSS4	USB analog power ground		
Part F								
H22	PWM0/GPIO7_A0	I/O	down	I	LCD_BL	LCD panel backlight brightness control output		
G23	PWM1/GPIO7_A1	I/O	down	I	PWM_LOG	PMIC power dynamic voltage scaling control,for LOG_PWM		
D28	GPIO7_A2	I/O	down	I	BL_EN	LCD panel backlight enable output		
F25	GPIO7_A3	I/O	down	I	LCD_EN	Display panel power enable		
E26	GPIO7_A4	I/O	up	I	LCD_CS/LCD_RST	LCD panel chip select output&LCD panel reset output		
G24	GPIO7_A5	I/O	down	I	TP_RST	Touch panel reset output		
F26	GPIO7_A6	I/O	up	I	TP_INT	Touch pannel&Touch key interrupt input		
E27	GPS_MAG/HSADC_D0_T1/UART3_RX/GPIO7_A7	I/O	up	I	HP_DET	headphone insert detect input	GPS_MAG	
J21	GPS_SIG/HSADC_D1_T1/UART3_TX/GPIO7_B0	I/O	down	I	3G_PWR	3G module power enable output	GPS_SIG	
H23	GPS_RFCLK/GPS_CLK_T1/UART3_CTSn/GPIO7_B1	I/O	up	I	WIFI_PWR	WIFI module power enable output	GPS_CLK	
F27	UART3_RTSn/GPIO7_B2	I/O	up	I			GPS_PWR	
E28	eDP_HOTPLUG/GPIO7_B3	I/O	down	I	SDMMC_PWR	SDMMC0 power control output		
J22	ISP_SHUTTEREN/SPI1_CLK/GPIO7_B4	I/O	down	I	5V_DRV	5V boost power enable	SHUTTER_OPEN	APIO1
H24	ISP_FLASHTRIGOUT/SPI1_CSN0/GPIO7_B5	I/O	up	I	FLASH_TRIGOUT	Flash LED trig output		
F28	ISP_PRELIGHTTRIG/SPI1_RXD/GPIO7_B6	I/O	down	I	FLASH_EN	Flash LED power enable output	PRELIGHT_TRIG	
G27	ISP_SHUTTERTRIG/SPI1_TXD/GPIO7_B7	I/O	down	I	SPK_CTL	Speaker out mute control	SHUTTER_TRIG	
G28	ISP_FLASHTRIGIN/EDPHDMI_CEC_T1/GPIO7_C0	I/O	up	I	HDMI_CEC	HDMI CEC communication		
H25	I2C4_SDA/GPIO7_C1	I/O	up	I	I2C4_SDA_TP	I2C serial port 4,for Touch panel,need external pull-up		
J23	I2C4_SCL/GPIO7_C2	I/O	up	I	I2C4_SCL_TP	I2C serial port 4,for Touch panel,need external pull-up		
H26	I2C5_SDA/EDPHDMI_I2C_SDA/GPIO7_C3	I/O	up	I	I2C5_SDA_HDMI	I2C serial port 5,for eDP and HDMI,need external pull-up		
J24	I2C5_SCL/EDPHDMI_I2C_SCL/GPIO7_C4	I/O	up	I	I2C5_SCL_HDMI	I2C serial port 5,for eDP and HDMI,need external pull-up		
H27	GPIO7_C5	I/O	down	I	VIB_CTL	Vibration control output		
J25	UART2_RX/IR_RX/PWM2/GPIO7_C6	I/O	up	I	UART2_RX	Uart2 serial port data input,for debug	IR_RX	
H28	UART2_TX/IR_TX/PWM3/EDPHDMI_CEC/GPIO7_C7	I/O	up	I	UART2_TX	Uart2 serial port data output,for debug	IR_TX	
L20	APIO1_VDD	P			APIO1_VDD	APIO1 digital IO power supply		
Part G								
G20	BS_JTAG_TMS	I	up	I	BS_JTAG_TMS			
F21	BS_JTAG_TDI	I	up	I	BS_JTAG_TDI			
E22	BS_JTAG_TRSTn	I	up	I	BS_JTAG_TRSTn			
E23	BS_JTAG_TCK	I	up	I	BS_JTAG_TCK			
F22	BS_JTAG_TDO	O	N/A	O	BS_JTAG_TDO			
D24	PS2_CLK/GPIO8_A0	I/O	up	I	GSENSOR_INT	G-Sensor interrupt input	PS2_CLK	

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C27	PS2_DATA/GPIO8_A1	I/O	up	I	COMPASS_INT	Compass interrupt input	PS2_DATA	APIO2
G21	SC_DET/GPIO8_A2	I/O	up	I	GYR_INT	Gyroscope interrupt input	SC_DET	
B28	SPI2_CSn1/SC_IO/GPIO8_A3	I/O	up	I	LIGHT_INT	Light sensor IC interrupt input	SC_IO	
A28	I2C1_SDA/SC_RST/GPIO8_A4	I/O	up	I	I2C1_SDA_Sensor	I2C serial port 1,for Sensor,need external pull-up	SC_RST	
E25	I2C1_SCL/SC_CLK/GPIO8_A5	I/O	up	I	I2C1_SCL_Sensor	I2C serial port 1,for Sensor,need external pull-up	SC_CLK	
D26	SPI2_CLK/SC_IO_T1/GPIO8_A6	I/O	down	I	SPI2_CLK			
D27	SPI2_CSn0/SC_DET_T1/GPIO8_A7	I/O	up	I	SPI2_CSn0			
F24	SPI2_RXD/SC_RST_T1/GPIO8_B0	I/O	down	I	SPI2_RXD			
C28	SPI2_TXD/SC_CLK_T1/GPIO8_B1	I/O	down	I	SPI2_TXD			
J20	APIO2_VDD	P			APIO2_VDD	APIO2 digital IO power supply		
Part H								
AH11	UART0_RXD/GPIO4_C0	I/O	up	I	UART0_RXD	UART0 serial port, for BT module		APIO3
AG10	UART0_TXD/GPIO4_C1	I/O	down	I	UART0_TXD	UART0 serial port, for BT module		
AB12	UART0_CTSn/GPIO4_C2	I/O	up	I	UART0_CTSn	UART0 serial port, for BT module		
AB11	UART0_RTSn/GPIO4_C3	I/O	up	I	UART0_RTSn	UART0 serial port, for BT module		
AH9	SDIO0_D0/GPIO4_C4	I/O	up	I	SDIO0_D0	SDIO0 data port, for WIFI module		
AH10	SDIO0_D1/GPIO4_C5	I/O	up	I	SDIO0_D1	SDIO0 data port, for WIFI module		
AG9	SDIO0_D2/GPIO4_C6	I/O	S	I	SDIO0_D2	SDIO0 data port, for WIFI module		
AH7	SDIO0_D3/GPIO4_C7	I/O	up	I	SDIO0_D3	SDIO0 data port, for WIFI module		
AH8	SDIO0_CMD/GPIO4_D0	I/O	up	I	SDIO0_CMD	SDIO0 command output, for WIFI module		
AG8	SDIO0_CLKOUT/GPIO4_D1	I/O	down	I	SDIO0_CLKO	SDIO0 clock output, for WIFI module		
AF9	SDIO0_DET/GPIO4_D2	I/O	up	I	BT_WAKE	CPU wake up BT module		
AE9	SDIO0_WP/GPIO4_D3	I/O	down	I	BT_REG_ON	BT module internal regulators power enable output		
AC11	SDIO0_PWR/GPIO4_D4	I/O	down	I	WIFI_REG_ON	WIFI module internal regulators power enable output		
AF8	SDIO0_BKPWR/GPIO4_D5	I/O	down	I	BT_RST	BT module reset output		
AE8	SDIO0_INTn/GPIO4_D6	I/O	up	I	WIFI_HOST_WAKE	WIFI module wake up CPU		
AD9	GPIO4_D7	I/O	up	I	BT_HOST_WAKE	BT module wake up CPU		
AA11	APIO3_VDD	P			APIO3_VDD	APIO3 digital IO power supply		
Part I								
AD11	I2S_SCLK/GPIO6_A0	I/O	down	I	I2S_SCLK	I2S port, for audio part		APIO4
AG11	I2S_LRCK_RX/GPIO6_A1	I/O	down	I	I2S_LRCK_RX	I2S port, for audio part		
AF11	I2S_LRCK_TX/GPIO6_A2	I/O	down	I	I2S_LRCK_TX	I2S port, for audio part		
AE11	I2S_SDI/GPIO6_A3	I/O	down	I	I2S_SDI	I2S port, for audio part		
AG12	I2S_SDO0/GPIO6_A4	I/O	down	I	I2S_SDO0	I2S port, for audio part		
AH13	I2S_SDO1/GPIO6_A5	I/O	down	I	I2S_SDO1	I2S port, for audio part		
AG13	I2S_SDO2/GPIO6_A6	I/O	down	I	I2S_SDO2	I2S port, for audio part		
AH12	I2S_SDO3/GPIO6_A7	I/O	down	I	I2S_SDO3	I2S port, for audio part		

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AC12	I2S_CLK/GPIO6_B0	I/O	down	I	I2S_CLK	I2S port, for audio part		
AF12	I2C2_SDA/GPIO6_B1	I/O	up	I	I2C2_SDA_AUDIO	I2C serial port 2,for Audio,need external pull-up		
AD12	I2C2_SCL/GPIO6_B2	I/O	up	I	I2C2_SCL_AUDIO	I2C serial port 2,for Audio,need external pull-up		
AE12	SPDIF_TX/GPIO6_B3	I/O	down	I	SPDIF_TX	HDMI Digital audio optical output		
Y12	APIO4_VDD	P			APIO4_VDD	APIO4 digital IO power supply		
Part J								
AF5	UART1_RX/TS0_D0/GPIO5_B0	I/O	up	I	UART1_RXD	UART1 serial port, for 3G module		
AA7	UART1_TX/TS0_D1/GPIO5_B1	I/O	down	I	UART1_TXD	UART1 serial port, for 3G module		
AH4	UART1_CTSn/TS0_D2/GPIO5_B2	I/O	up	I	UART1_CTSn	UART1 serial port, for 3G module		
AD6	UART1_RTSn/TS0_D3/GPIO5_B3	I/O	up	I	UART1_RTSn	UART1 serial port, for 3G module		
AD7	SPI0_CLK/UART4_CTSn/TS0_D4/GPIO5_B4	I/O	up	I	3G_WAKEUP_IN	CPU wakeup 3G module		
AC7	SPI0_CSn0/UART4_RTSn/TS0_D5/GPIO5_B5	I/O	up	I	3G_WAKEUP_OUT	3G module wakeup CPU		
AE5	SPI0_TXD/UART4_TX/TS0_D6/GPIO5_B6	I/O	down	I	3G_DISABLE	3G module disable output		APIO5
AF6	SPI0_RXD/UART4_RX/TS0_D7/GPIO5_B7	I/O	up	I	AP_RDY	AP ready status output		
AG5	SPI0_CSn1/TS0_SYNC/GPIO5_C0	I/O	up	I	BP_RDY	BP ready status input		
AA9	TS0_VALID/GPIO5_C1	I/O	down	I				
AE6	TS0_CLK/GPIO5_C2	I/O	down	I	3G_RST	3G module reset output		
AB8	TS0_ERR/GPIO5_C3	I/O	down	I	3G_REG_ON	3G module internal regulators power enable output		
Y11	APIO5_VDD	P			APIO5_VDD	APIO5 digital IO power supply		
Part K								
B19	DDR0_DQ0	A			DDR0_DQ0	DRAM0 data port		
C18	DDR0_DQ1	A			DDR0_DQ1	DRAM0 data port		
F17	DDR0_DQ2	A			DDR0_DQ2	DRAM0 data port		
F18	DDR0_DQ3	A			DDR0_DQ3	DRAM0 data port		
A19	DDR0_DQ4	A			DDR0_DQ4	DRAM0 data port		
E18	DDR0_DQ5	A			DDR0_DQ5	DRAM0 data port		
C20	DDR0_DQ6	A			DDR0_DQ6	DRAM0 data port		
D20	DDR0_DQ7	A			DDR0_DQ7	DRAM0 data port		
B5	DDR0_DQ8	A			DDR0_DQ8	DRAM0 data port		
A5	DDR0_DQ9	A			DDR0_DQ9	DRAM0 data port		
A3	DDR0_DQ10	A			DDR0_DQ10	DRAM0 data port		
C6	DDR0_DQ11	A			DDR0_DQ11	DRAM0 data port		
E8	DDR0_DQ12	A			DDR0_DQ12	DRAM0 data port		
A6	DDR0_DQ13	A			DDR0_DQ13	DRAM0 data port		
B6	DDR0_DQ14	A			DDR0_DQ14	DRAM0 data port		
F8	DDR0_DQ15	A			DDR0_DQ15	DRAM0 data port		
B15	DDR0_DQ16	A			DDR0_DQ16	DRAM0 data port		

RK3288 IO LIST

Editor: Lin Xu					Ver: 1.0		Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
A16	DDR0_DQ17	A			DDR0_DQ17	DRAM0 data port		DDR0
F15	DDR0_DQ18	A			DDR0_DQ18	DRAM0 data port		
B16	DDR0_DQ19	A			DDR0_DQ19	DRAM0 data port		
D17	DDR0_DQ20	A			DDR0_DQ20	DRAM0 data port		
B18	DDR0_DQ21	A			DDR0_DQ21	DRAM0 data port		
C17	DDR0_DQ22	A			DDR0_DQ22	DRAM0 data port		
A18	DDR0_DQ23	A			DDR0_DQ23	DRAM0 data port		
A2	DDR0_DQ24	A			DDR0_DQ24	DRAM0 data port		
A1	DDR0_DQ25	A			DDR0_DQ25	DRAM0 data port		
D5	DDR0_DQ26	A			DDR0_DQ26	DRAM0 data port		
E6	DDR0_DQ27	A			DDR0_DQ27	DRAM0 data port		
C5	DDR0_DQ28	A			DDR0_DQ28	DRAM0 data port		
F7	DDR0_DQ29	A			DDR0_DQ29	DRAM0 data port		
C4	DDR0_DQ30	A			DDR0_DQ30	DRAM0 data port		
E7	DDR0_DQ31	A			DDR0_DQ31	DRAM0 data port		
A20	DDR0_DQS0	A			DDR0_DQS0	DRAM0 data strobe 0		
B20	DDR0_DQS0n	A			DDR0_DQS0n	DRAM0 data strobe 0		
B7	DDR0_DQS1	A			DDR0_DQS1	DRAM0 data strobe 1		
A7	DDR0_DQS1n	A			DDR0_DQS1n	DRAM0 data strobe 1		
B17	DDR0_DQS2	A			DDR0_DQS2	DRAM0 data strobe 2		
A17	DDR0_DQS2n	A			DDR0_DQS2n	DRAM0 data strobe 2		
B4	DDR0_DQS3	A			DDR0_DQS3	DRAM0 data strobe 3		
A4	DDR0_DQS3n	A			DDR0_DQS3n	DRAM0 data strobe 3		
E17	DDR0_DM0	A			DDR0_DM0	DRAM0 data mask 0		
F9	DDR0_DM1	A			DDR0_DM1	DRAM0 data mask 1		
A15	DDR0_DM2	A			DDR0_DM2	DRAM0 data mask 2		
B3	DDR0_DM3	A			DDR0_DM3	DRAM0 data mask 3		
G17	DDR0_PZQ	A			DDR0_PZQ	DRAM0 reference pin for ZQ calibration,,connect a 240R%1 resistor to VSS		
G8	DDR0_RETLE	A			DDR0_RETLE	DRAM0 retention enable input		
G12	DDR0_ATO	A			DDR0_ATO	DRAM0 analog signal test out		
H15	DDR0_DTO1	A			DDR0_DTO1	DRAM0 digital signal test out1		
H17	DDR0_DTO0	A			DDR0_DTO0	DRAM0 digital signal test out0		
B10	DDR0_A0	A			DDR0_A0	DRAM0 address port		
C11	DDR0_A1	A			DDR0_A1	DRAM0 address port		
A10	DDR0_A2	A			DDR0_A2	DRAM0 address port		
E12	DDR0_A3	A			DDR0_A3	DRAM0 address port		

RK3288 IO LIST

Editor: Lin Xu					Ver: 1.0		Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
F12	DDR0_A4	A			DDR0_A4	DRAM0 address port		
B12	DDR0_A5	A			DDR0_A5	DRAM0 address port		
C12	DDR0_A6	A			DDR0_A6	DRAM0 address port		
A12	DDR0_A7	A			DDR0_A7	DRAM0 address port		
B13	DDR0_A8	A			DDR0_A8	DRAM0 address port		
A14	DDR0_A9	A			DDR0_A9	DRAM0 address port		
A13	DDR0_A10	A			DDR0_A10	DRAM0 address port		
D14	DDR0_A11	A			DDR0_A11	DRAM0 address port		
F14	DDR0_A12	A			DDR0_A12	DRAM0 address port		
C14	DDR0_A13	A			DDR0_A13	DRAM0 address port		
B14	DDR0_A14	A			DDR0_A14	DRAM0 address port		
C15	DDR0_A15	A			DDR0_A15	DRAM0 address port		
B11	DDR0_CLK	A			DDR0_CLK	DRAM0 differential clock output		
A11	DDR0_CLKn	A			DDR0_CLKn	DRAM0 differential clock output		
D8	DDR0_BA0	A			DDR0_BA0	DRAM0 bank select 0		
A9	DDR0_BA1	A			DDR0_BA1	DRAM0 bank select 1		
E11	DDR0_BA2	A			DDR0_BA2	DRAM0 bank select 2		
E14	DDR0_ODT0	A			DDR0_ODT0	DRAM0 on die termination control 0		
E15	DDR0_ODT1	A			DDR0_ODT1	DRAM0 on die termination control 1		
B8	DDR0_CSN0	A			DDR0_CSN0	DRAM0 chip select 0		
F11	DDR0_CSN1	A			DDR0_CSN1	DRAM0 chip select 1		
C9	DDR0_CKE0	A			DDR0_CKE0	DRAM0 clock enable 0		
C8	DDR0_CKE1	A			DDR0_CKE1	DRAM0 clock enable 1		
D11	DDR0_RASN	A			DDR0_RASN	DRAM0 row address strobe output		
A8	DDR0_CASN	A			DDR0_CASN	DRAM0 column address strobe output		
B9	DDR0_WEN	A			DDR0_WEN	DRAM0 write enable strobe output		
E9	DDR0_RESET	A			DDR0_RESET	DRAM0 reset output		
H12	DDR0_VREF	P			DDR0_VREF	DARM0 reference voltage input		
H11	DDR0_VREFAO	P			DDR0_VREFAO	DARM0 reference voltage input always on		
G14	NC1		N/A	N/A	NC	Reverse		
G15	NC2		N/A	N/A	NC	Reverse		
G11	NC3		N/A	N/A	NC	Reverse		
H9	DDR0_VDD1	P			DDR0_VDD1	DRAM0 Digital power supply		
J11	DDR0_VDD2	P			DDR0_VDD2	DRAM0 Digital power supply		
J12	DDR0_VDD3	P			DDR0_VDD3	DRAM0 Digital power supply		
J14	DDR0_VDD4	P			DDR0_VDD4	DRAM0 Digital power supply		
J15	DDR0_VDD5	P			DDR0_VDD5	DRAM0 Digital power supply		

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0			Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
H14	DDR0_VDDAO	P			DDR0_VDDAO	DRAM0 Digital IO power always on		
Part L								
W2	DDR1_DQ0	A			DDR1_DQ0	DRAM1 data port		
V3	DDR1_DQ1	A			DDR1_DQ1	DRAM1 data port		
Y1	DDR1_DQ2	A			DDR1_DQ2	DRAM1 data port		
U6	DDR1_DQ3	A			DDR1_DQ3	DRAM1 data port		
W1	DDR1_DQ4	A			DDR1_DQ4	DRAM1 data port		
Y2	DDR1_DQ5	A			DDR1_DQ5	DRAM1 data port		
V5	DDR1_DQ6	A			DDR1_DQ6	DRAM1 data port		
Y3	DDR1_DQ7	A			DDR1_DQ7	DRAM1 data port		
E2	DDR1_DQ8	A			DDR1_DQ8	DRAM1 data port		
E1	DDR1_DQ9	A			DDR1_DQ9	DRAM1 data port		
C1	DDR1_DQ10	A			DDR1_DQ10	DRAM1 data port		
F3	DDR1_DQ11	A			DDR1_DQ11	DRAM1 data port		
H5	DDR1_DQ12	A			DDR1_DQ12	DRAM1 data port		
H4	DDR1_DQ13	A			DDR1_DQ13	DRAM1 data port		
J5	DDR1_DQ14	A			DDR1_DQ14	DRAM1 data port		
J6	DDR1_DQ15	A			DDR1_DQ15	DRAM1 data port		
T2	DDR1_DQ16	A			DDR1_DQ16	DRAM1 data port		
R6	DDR1_DQ17	A			DDR1_DQ17	DRAM1 data port		
T1	DDR1_DQ18	A			DDR1_DQ18	DRAM1 data port		
R5	DDR1_DQ19	A			DDR1_DQ19	DRAM1 data port		
U4	DDR1_DQ20	A			DDR1_DQ20	DRAM1 data port		
V1	DDR1_DQ21	A			DDR1_DQ21	DRAM1 data port		
U3	DDR1_DQ22	A			DDR1_DQ22	DRAM1 data port		
V2	DDR1_DQ23	A			DDR1_DQ23	DRAM1 data port		
B1	DDR1_DQ24	A			DDR1_DQ24	DRAM1 data port		
B2	DDR1_DQ25	A			DDR1_DQ25	DRAM1 data port		
E4	DDR1_DQ26	A			DDR1_DQ26	DRAM1 data port		
G6	DDR1_DQ27	A			DDR1_DQ27	DRAM1 data port		
E3	DDR1_DQ28	A			DDR1_DQ28	DRAM1 data port		
F5	DDR1_DQ29	A			DDR1_DQ29	DRAM1 data port		
C2	DDR1_DQ30	A			DDR1_DQ30	DRAM1 data port		
H6	DDR1_DQ31	A			DDR1_DQ31	DRAM1 data port		
AA2	DDR1_DQS0	A			DDR1_DQS0	DRAM1 data strobe 0		
AA1	DDR1_DQS0n	A			DDR1_DQS0n	DRAM1 data strobe 0		
G2	DDR1_DQS1	A			DDR1_DQS1	DRAM1 data strobe 1		

RK3288 IO LIST

Editor: Lin Xu					Ver: 1.0		Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
G1	DDR1_DQS1n	A			DDR1_DQS1n	DRAM1 data strobe 1		DDR1
U2	DDR1_DQS2	A			DDR1_DQS2	DRAM1 data strobe 2		
U1	DDR1_DQS2n	A			DDR1_DQS2n	DRAM1 data strobe 2		
D2	DDR1_DQS3	A			DDR1_DQS3	DRAM1 data strobe 3		
D1	DDR1_DQS3n	A			DDR1_DQS3n	DRAM1 data strobe 3		
U5	DDR1_DM0	A			DDR1_DM0	DRAM1 data mask 0		
G5	DDR1_DM1	A			DDR1_DM1	DRAM1 data mask 1		
R3	DDR1_DM2	A			DDR1_DM2	DRAM1 data mask 2		
D3	DDR1_DM3	A			DDR1_DM3	DRAM1 data mask 3		
U7	DDR1_PZQ	A			DDR1_PZQ	DRAM1 reference pin for ZQ calibration,,connect a 12K%1 resistor to VSS		
H7	DDR1_RETLE	A			DDR1_RETLE	DRAM1 retention enable input		
M7	DDR1_ATO	A			DDR1_ATO	DRAM1 analog signal test out		
R8	DDR1_DTO1	A			DDR1_DTO1	DRAM1 digital signal test out1		
U8	DDR1_DTO0	A			DDR1_DTO0	DRAM1 digital signal test out0		
L3	DDR1_A0	A			DDR1_A0	DRAM1 address port		
K2	DDR1_A1	A			DDR1_A1	DRAM1 address port		
K1	DDR1_A2	A			DDR1_A2	DRAM1 address port		
M5	DDR1_A3	A			DDR1_A3	DRAM1 address port		
M6	DDR1_A4	A			DDR1_A4	DRAM1 address port		
M2	DDR1_A5	A			DDR1_A5	DRAM1 address port		
M1	DDR1_A6	A			DDR1_A6	DRAM1 address port		
M3	DDR1_A7	A			DDR1_A7	DRAM1 address port		
N1	DDR1_A8	A			DDR1_A8	DRAM1 address port		
P1	DDR1_A9	A			DDR1_A9	DRAM1 address port		
N2	DDR1_A10	A			DDR1_A10	DRAM1 address port		
P4	DDR1_A11	A			DDR1_A11	DRAM1 address port		
P6	DDR1_A12	A			DDR1_A12	DRAM1 address port		
P3	DDR1_A13	A			DDR1_A13	DRAM1 address port		
P2	DDR1_A14	A			DDR1_A14	DRAM1 address port		
R1	DDR1_A15	A			DDR1_A15	DRAM1 address port		
L2	DDR1_CLK	A			DDR1_CLK	DRAM1 differential clock output		
L1	DDR1_CLKn	A			DDR1_CLKn	DRAM1 differential clock output		
L4	DDR1_BA0	A			DDR1_BA0	DRAM1 bank select 0		
J1	DDR1_BA1	A			DDR1_BA1	DRAM1 bank select 1		
L5	DDR1_BA2	A			DDR1_BA2	DRAM1 bank select 2		
P5	DDR1_ODT0	A			DDR1_ODT0	DRAM1 on die termination control 0		

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0			Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
R2	DDR1_ODT1	A			DDR1_ODT1	DRAM1 on die termination control 1		
H2	DDR1_CSN0	A			DDR1_CSN0	DRAM1 chip select 0		
J3	DDR1_CSN1	A			DDR1_CSN1	DRAM1 chip select 1		
F1	DDR1_CKE0	A			DDR1_CKE0	DRAM1 clock enable 0		
H3	DDR1_CKE1	A			DDR1_CKE1	DRAM1 clock enable 1		
L6	DDR1_RASN	A			DDR1_RASN	DRAM1 row address strobe output		
H1	DDR1_CASN	A			DDR1_CASN	DRAM1 column address strobe output		
J2	DDR1_WEN	A			DDR1_WEN	DRAM1 write enable strobe output		
F2	DDR1_RESET	A			DDR1_RESET	DRAM1 reset output		
M8	DDR1_VREF	P			DDR1_VREF	DARM1 reference voltage input		
L8	DDR1_VREFAO	P			DDR1_VREFAO	DARM1 reference voltage input always on		
P7	NC4		N/A	N/A	NC	Reverse		
R7	NC5		N/A	N/A	NC	Reverse		
L7	NC6		N/A	N/A	NC	Reverse		
J8	DDR1_VDD1	P			DDR1_VDD1	DRAM1 Digital power supply		
L9	DDR1_VDD2	P			DDR1_VDD2	DRAM1 Digital power supply		
M9	DDR1_VDD3	P			DDR1_VDD3	DRAM1 Digital power supply		
P9	DDR1_VDD4	P			DDR1_VDD4	DRAM1 Digital power supply		
R9	DDR1_VDD5	P			DDR1_VDD5	DRAM1 Digital power supply		
P8	DDR1_VDDAO	P			DDR1_VDDAO	DRAM1 Digital IO power always on		
Part M								
C3	VSS1	G			VSS	Common ground and substrate connection		
D6	VSS2	G			VSS	Common ground and substrate connection		
D9	VSS3	G			VSS	Common ground and substrate connection		
D12	VSS4	G			VSS	Common ground and substrate connection		
D15	VSS5	G			VSS	Common ground and substrate connection		
D18	VSS6	G			VSS	Common ground and substrate connection		
E20	VSS7	G			VSS	Common ground and substrate connection		
U24	VSS8	G			VSS	Common ground and substrate connection		
A21	VSS9	G			VSS	Common ground and substrate connection		
Y24	VSS10	G			VSS	Common ground and substrate connection		
AC24	VSS11	G			VSS	Common ground and substrate connection		
F4	VSS12	G			VSS	Common ground and substrate connection		
J4	VSS13	G			VSS	Common ground and substrate connection		
J9	VSS14	G			VSS	Common ground and substrate connection		
U9	VSS15	G			VSS	Common ground and substrate connection		
J17	VSS16	G			VSS	Common ground and substrate connection		

RK3288 IO LIST

Editor: Lin Xu					Ver: 1.0		Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
W10	VSS17	G			VSS	Common ground and substrate connection		
K10	VSS18	G			VSS	Common ground and substrate connection		
K11	VSS19	G			VSS	Common ground and substrate connection		
K12	VSS20	G			VSS	Common ground and substrate connection		
K13	VSS21	G			VSS	Common ground and substrate connection		
K14	VSS22	G			VSS	Common ground and substrate connection		
K15	VSS23	G			VSS	Common ground and substrate connection		
K16	VSS24	G			VSS	Common ground and substrate connection		
K17	VSS25	G			VSS	Common ground and substrate connection		
K18	VSS26	G			VSS	Common ground and substrate connection		
K19	VSS27	G			VSS	Common ground and substrate connection		
J18	VSS28	G			VSS	Common ground and substrate connection		
L10	VSS29	G			VSS	Common ground and substrate connection		
L11	VSS30	G			VSS	Common ground and substrate connection		
L13	VSS31	G			VSS	Common ground and substrate connection		
L14	VSS32	G			VSS	Common ground and substrate connection		
L15	VSS33	G			VSS	Common ground and substrate connection		
M4	VSS34	G			VSS	Common ground and substrate connection		
M10	VSS35	G			VSS	Common ground and substrate connection		
M11	VSS36	G			VSS	Common ground and substrate connection		
M13	VSS37	G			VSS	Common ground and substrate connection		
M14	VSS38	G			VSS	Common ground and substrate connection		
Y18	VSS39	G			VSS	Common ground and substrate connection		
N10	VSS40	G			VSS	Common ground and substrate connection		
N11	VSS41	G			VSS	Common ground and substrate connection		
N13	VSS42	G			VSS	Common ground and substrate connection		
N14	VSS43	G			VSS	Common ground and substrate connection		
N15	VSS44	G			VSS	Common ground and substrate connection		
P10	VSS45	G			VSS	Common ground and substrate connection		
P11	VSS46	G			VSS	Common ground and substrate connection		
P13	VSS47	G			VSS	Common ground and substrate connection		
P14	VSS48	G			VSS	Common ground and substrate connection		
P15	VSS49	G			VSS	Common ground and substrate connection		
P16	VSS50	G			VSS	Common ground and substrate connection		
P17	VSS51	G			VSS	Common ground and substrate connection		
P18	VSS52	G			VSS	Common ground and substrate connection		
R4	VSS53	G			VSS	Common ground and substrate connection		

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0				Date: 2014-04-29
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
R10	VSS54	G			VSS	Common ground and substrate connection		
R13	VSS55	G			VSS	Common ground and substrate connection		
R16	VSS56	G			VSS	Common ground and substrate connection		
R17	VSS57	G			VSS	Common ground and substrate connection		
R18	VSS58	G			VSS	Common ground and substrate connection		
R19	VSS59	G			VSS	Common ground and substrate connection		
T10	VSS60	G			VSS	Common ground and substrate connection		
R14	VSS61	G			VSS	Common ground and substrate connection		
T13	VSS62	G			VSS	Common ground and substrate connection		
Y20	VSS63	G			VSS	Common ground and substrate connection		
T15	VSS64	G			VSS	Common ground and substrate connection		
T16	VSS65	G			VSS	Common ground and substrate connection		
T17	VSS66	G			VSS	Common ground and substrate connection		
T18	VSS67	G			VSS	Common ground and substrate connection		
T19	VSS68	G			VSS	Common ground and substrate connection		
V9	VSS69	G			VSS	Common ground and substrate connection		
U10	VSS70	G			VSS	Common ground and substrate connection		
R15	VSS71	G			VSS	Common ground and substrate connection		
U13	VSS72	G			VSS	Common ground and substrate connection		
V4	VSS73	G			VSS	Common ground and substrate connection		
V10	VSS74	G			VSS	Common ground and substrate connection		
V11	VSS75	G			VSS	Common ground and substrate connection		
V12	VSS76	G			VSS	Common ground and substrate connection		
V13	VSS77	G			VSS	Common ground and substrate connection		
W11	VSS78	G			VSS	Common ground and substrate connection		
W12	VSS79	G			VSS	Common ground and substrate connection		
W13	VSS80	G			VSS	Common ground and substrate connection		
W14	VSS81	G			VSS	Common ground and substrate connection		
W15	VSS82	G			VSS	Common ground and substrate connection		
W16	VSS83	G			VSS	Common ground and substrate connection		
W17	VSS84	G			VSS	Common ground and substrate connection		
W18	VSS85	G			VSS	Common ground and substrate connection		
W19	VSS86	G			VSS	Common ground and substrate connection		
Part N								
AA12	eDP_TP_OUT/SATA_EXTR	A			eDP_TP_OUT	eDP dc test point		
AC17	eDP_CLK24M_IN/MIPI_LLI_EXTR	A			eDP_CLK24M_IN	eDP 24M input reference clock		
AG14	eDP_TX0P	A			eDP_TX0P	eDP differential lane 0 positive output		

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0			Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
AH14	eDP_TX0N	A			eDP_TX0N	eDP differential lane 0 negative output		EDP
AG15	eDP_TX1P	A			eDP_TX1P	eDP differential lane 1 positive output		
AH15	eDP_TX1N	A			eDP_TX1N	eDP differential lane 1 negative output		
AG16	eDP_TX2P	A			eDP_TX2P	eDP differential lane 2 positive output		
AH16	eDP_TX2N	A			eDP_TX2N	eDP differential lane 2 negative output		
AG17	eDP_TX3P	A			eDP_TX3P	eDP differential lane 3 positive output		
AH17	eDP_TX3N	A			eDP_TX3N	eDP differential lane 3 negative output		
AH18	eDP_AXUN	A			eDP_AXUN	eDP differential AUX channel negative output		
AG18	eDP_AXUP	A			eDP_AXUP	eDP differential AUX channel positive output		
AC18	eDP_EXTR	A			eDP_EXTR	eDP reference current generate,connect a 12K%1 resistor to		
Y17	eDP_AVDD_1V0	P			eDP_AVDD_1V0	eDP digital power supply		
AA17	eDP_AVDD_1V8	P			eDP_AVDD_1V8	eDP I/O power supply		
Part O								
AB19	HDMI_HPD	A			HDMI_HPD	HDMI Hot Plug Detection interrupt		HDMI
AG19	HDMI_TXCP	A			HDMI_TXCP	HDMI differential pixel clock positive		
AH19	HDMI_TXCN	A			HDMI_TXCN	HDMI differential pixel clock negative		
AG20	HDMI_TX0P	A			HDMI_TX0P	HDMI channel 0 differential serial data positive		
AH20	HDMI_TX0N	A			HDMI_TX0N	HDMI channel 0 differential serial data negative		
AG21	HDMI_TX1P	A			HDMI_TX1P	HDMI channel 1 differential serial data positive		
AH21	HDMI_TX1N	A			HDMI_TX1N	HDMI channel 1 differential serial data negative		
AG22	HDMI_TX2P	A			HDMI_TX2P	HDMI channel 2 differential serial data positive		
AH22	HDMI_TX2N	A			HDMI_TX2N	HDMI channel 2 differential serial data negative		
AB17	HDMI_EXTR	A			HDMI_EXTR	HDMI reference current generate,connect a 1.62K%1 resistor to		
AA18	HDMI_AVDD_1V0	P			HDMI_AVDD_1V0	HDMI digital power supply		
AB20	HDMI_AVDD_1V8	P			HDMI_AVDD_1V8	HDMI I/O power supply		
AF14	HDMI_AVSS1	AG			HDMI_AVSS	Analog power ground for		HDMI/MIPI/ edp
AF15	HDMI_AVSS2	AG			HDMI_AVSS	Analog power ground for		
AF17	HDMI_AVSS3	AG			HDMI_AVSS	Analog power ground for		
AF18	HDMI_AVSS4	AG			HDMI_AVSS	Analog power ground for		
AD20	HDMI_AVSS5	AG			HDMI_AVSS	Analog power ground for		
AD23	HDMI_AVSS6	AG			HDMI_AVSS	Analog power ground for		
AD26	HDMI_AVSS7	AG			HDMI_AVSS	Analog power ground for		
AF26	HDMI_AVSS8	AG			HDMI_AVSS	Analog power ground for		
Part P								
AE3	FLASH0_D0/EMMC_D0/GPIO3_A0	I/O	up	I	EMMC_D0	Nand Flash/EMMC data port	FLASH0_D0	
AD3	FLASH0_D1/EMMC_D1/GPIO3_A1	I/O	up	I	EMMC_D1	Nand Flash/EMMC data port	FLASH0_D1	
AF3	FLASH0_D2/EMMC_D2/GPIO3_A2	I/O	up	I	EMMC_D2	Nand Flash/EMMC data port	FLASH0_D2	

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0			Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
AF1	FLASH0_D3/EMMC_D3/GPIO3_A3	I/O	up	I	EMMC_D3	Nand Flash/EMMC data port	FLASH0_D3	FLASH0/ EMMC
AF2	FLASH0_D4/EMMC_D4/GPIO3_A4	I/O	up	I	EMMC_D4	Nand Flash/EMMC data port	FLASH0_D4	
AG3	FLASH0_D5/EMMC_D5/GPIO3_A5	I/O	up	I	EMMC_D5	Nand Flash/EMMC data port	FLASH0_D5	
AG1	FLASH0_D6/EMMC_D6/GPIO3_A6	I/O	up	I	EMMC_D6	Nand Flash/EMMC data port	FLASH0_D6	
AG2	FLASH0_D7/EMMC_D7/GPIO3_A7	I/O	up	I	EMMC_D7	Nand Flash/EMMC data port	FLASH0_D7	
AH2	FLASH0_RDY/GPIO3_B0	I/O	up	I			FLASH0_RDY	
AH1	FLASH0_WP/EMMC_PWREN/GPIO3_B1	I/O	down	I	EMMC_PWR	EMMC power enable	FLASH0_WP	
Y6	FLASH0_RDN/GPIO3_B2	I/O	up	I			FLASH0_RDN	
AF4	FLASH0_ALE/GPIO3_B3	I/O	down	I			FLASH0_ALE	
AH3	FLASH0_CLE/GPIO3_B4	I/O	down	I			FLASH0_CLE	
AG4	FLASH0_WRN/GPIO3_B5	I/O	up	I			FLASH0_WRN	
AC5	FLASH0_CSn0/GPIO3_B6	I/O	up	I			FLASH0_CSn0	
AD4	FLASH0_CSn1/GPIO3_B7	I/O	up	I			FLASH0_CSn1	
AC4	FLASH0_CSn2/EMMC_CMD/GPIO3_C0	I/O	up	I	EMMC_CMD	EMMC command port	FLASH0_CSn2	
Y7	FLASH0_CSn3/EMMC_RSTNOUT/GPIO3_C1	I/O	up	I	EMMC_RST	EMMC reset output	FLASH0_CSn3	
AB6	FLASH0_DQS/EMMC_CLKOUT/GPIO3_C2	I/O	down	I	EMMC_CLKO	EMMC clock out	FLASH0_DQS	
Y8	FLASH0_VOLTAGE_SEL/GPIO3_C3	I/O	down	I	FLASH0_VOLTAGE_SEL	Nand Flash default power supply voltage select for boot		
Y9	FLASH0_VDD	P			FLASH0_VDD	FLASH0 digital IO power supply		
Part Q								
Y4	HOST_D0/MAC_TXD2/SDIO1_D0/FLASH1_D0/GPIO3_D0	I/O	up	I	MAC_TXD2	MAC transmit data	FLASH1_D0	FLASH1
V6	HOST_D1/MAC_TXD3/SDIO1_D1/FLASH1_D1/GPIO3_D1	I/O	up	I	MAC_TXD3	MAC transmit data	FLASH1_D1	
AB1	HOST_D2/MAC_RXD2/SDIO1_D2/FLASH1_D2/GPIO3_D2	I/O	up	I	MAC_RXD2	MAC receive data	FLASH1_D2	
AC1	HOST_D3/MAC_RXD3/SDIO1_D3/FLASH1_D3/GPIO3_D3	I/O	up	I	MAC_RXD3	MAC receive data	FLASH1_D3	
AD1	HOST_D4/MAC_TXD0/SDIO1_DET/FLASH1_D4/GPIO3_D	I/O	up	I	MAC_TXD0	MAC transfer data	FLASH1_D4	
AB2	HOST_D5/MAC_TXD1/SDIO1_WRPRT/FLASH1_D5/GPIO3_D5	I/O	up	I	MAC_TXD1	MAC transmit data	FLASH1_D5	
AA3	HOST_D6/MAC_RXD0/SDIO1_BKPWR/FLASH1_D6/GPIO3_D6	I/O	up	I	MAC_RXD0	MAC receive data	FLASH1_D6	
AA4	HOST_D7/MAC_RXD1/SDIO1_INTn/FLASH1_D7/GPIO3_D7	I/O	up	I	MAC_RXD1	MAC receive data	FLASH1_D7	
AC3	HOST_CKOUTP/MAC_MDC/FLASH1_RDY/GPIO4_A0	I/O	up	I	MAC_MDC	MAC management clock	FLASH1_RDY	
AC2	HOST_CKOUTN/MAC_RXDV/FLASH0_CSn4/FLASH1_WP/GPIO4_A1	I/O	up	I	MAC_RXDV	MAC receive data valid	FLASH1_WP	
AE1	HOST_D8/MAC_RXER/FLASH0_CSn5/FLASH1_RDN/GPIO4_A2	I/O	up	I	MAC_RXER	MAC receive error	FLASH1_RDN	
AE2	HOST_D9/MAC_CLK/FLASH0_CSn6/FLASH1_ALE/GPIO4_A3	I/O	up	I	MAC_MCLK	MAC reference clock output	FLASH1_ALE	
AD2	HOST_D10/MAC_TXEN/FLASH0_CSn7/FLASH1_CLE/GPIO4_A4	I/O	up	I	MAC_TXEN	MAC transmit enable	FLASH1_CLE	

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0			Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
Y5	HOST_D11/MAC_MDIO/FLASH1_WRN/GPIO4_A5	I/O	up	I	MAC_MDIO	MAC management command and data	FLASH1_WRN	
AB5	HOST_D12/MAC_RXCLK/SDIO1_CMD/FLASH1_CSn0/GPIO4_A6	I/O	up	I	MAC_RXCLK	MAC receive clock	FLASH1_CSn0	
AA6	HOST_D13/MAC_CRS/SDIO1_CLKOUT/FLASH1_CSn1/GPIO4_A7	I/O	up	I	MAC_CRS	MAC carrier sense detect	FLASH1_CSn1	
AA5	HOST_D14/MAC_COL/FLASH1_DQS/FLASH1_CSn3/GPIO4_B0	I/O	up	I	MAC_COL	MAC collision detect	FLASH1_DQS	
V7	HOST_D15/MAC_TXCLK/SDIO1_PWREN/FLASH1_CSn2/GPIO4_B1	I/O	up	I	MAC_TXCLK	MAC transmit clock	FLASH1_CSn2	
V8	FLASH1_VDD	P			FLASH1_VDD	FLASH1 digital IO power supply		
Part R								
U14	CPU_VDD1	P			CPU_VDD1	ARM core power supply		
U15	CPU_VDD2	P			CPU_VDD2	ARM core power supply		
U16	CPU_VDD3	P			CPU_VDD3	ARM core power supply		
U17	CPU_VDD4	P			CPU_VDD4	ARM core power supply		
U18	CPU_VDD5	P			CPU_VDD5	ARM core power supply		
U19	CPU_VDD6	P			CPU_VDD6	ARM core power supply		
V14	CPU_VDD7	P			CPU_VDD7	ARM core power supply		
V15	CPU_VDD8	P			CPU_VDD8	ARM core power supply		
V16	CPU_VDD9	P			CPU_VDD9	ARM core power supply		
V17	CPU_VDD10	P			CPU_VDD10	ARM core power supply		
V18	CPU_VDD11	P			CPU_VDD11	ARM core power supply		
V19	CPU_VDD12	P			CPU_VDD12	ARM core power supply		
T14	CPU_VDD_COM	P			CPU_VDD_COM	ARM core power feedback ouput		
V20	LCD_VDD	P			LCDC0_POWER	LCD digital IO power supply		
L16	GPU_VDD1	P			GPU_VDD1	GPU core power supply		
L17	GPU_VDD2	P			GPU_VDD2	GPU core power supply		
L18	GPU_VDD3	P			GPU_VDD3	GPU core power supply		
L19	GPU_VDD4	P			GPU_VDD4	GPU core power supply		
M16	GPU_VDD5	P			GPU_VDD5	GPU core power supply		
M17	GPU_VDD6	P			GPU_VDD6	GPU core power supply		
M18	GPU_VDD7	P			GPU_VDD7	GPU core power supply		
M19	GPU_VDD8	P			GPU_VDD8	GPU core power supply		
N16	GPU_VDD9	P			GPU_VDD9	GPU core power supply		
N17	GPU_VDD10	P			GPU_VDD10	GPU core power supply		
N18	GPU_VDD11	P			GPU_VDD11	GPU core power supply		
N19	GPU_VDD12	P			GPU_VDD12	GPU core power supply		
M15	GPU_VDD_COM	P			GPU_VDD_COM	GPU core power feedback ouput		

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0			Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
L12	LOGIC_VDD1	P			LOGIC_VDD1	Logic power supply		
M12	LOGIC_VDD2	P			LOGIC_VDD2	Logic power supply		
N12	LOGIC_VDD3	P			LOGIC_VDD3	Logic power supply		
P12	LOGIC_VDD4	P			LOGIC_VDD4	Logic power supply		
R12	LOGIC_VDD5	P			LOGIC_VDD5	Logic power supply		
T12	LOGIC_VDD6	P			LOGIC_VDD6	Logic power supply		
U12	LOGIC_VDD7	P			LOGIC_VDD7	Logic power supply		
R11	LOGIC_VDD8	P			LOGIC_VDD8	Logic power supply		
T11	LOGIC_VDD9	P			LOGIC_VDD9	Logic power supply		
U11	LOGIC_VDD10	P			LOGIC_VDD10	Logic power supply		
Part S								
G9	NC7		N/A	N/A	NC	Reverse		
J7	NC8		N/A	N/A	NC	Reverse		
A25	NC9		N/A	N/A	NC	Reverse		
B25	NC10		N/A	N/A	NC	Reverse		
A24	NC11		N/A	N/A	NC	Reverse		
B24	NC12		N/A	N/A	NC	Reverse		
AB15	NC13		N/A	N/A	NC	Reverse		
AB14	NC14		N/A	N/A	NC	Reverse		
AC15	NC15		N/A	N/A	NC	Reverse		
AC14	NC16		N/A	N/A	NC	Reverse		
Y15	NC17		N/A	N/A	NC	Reverse		
AA15	NC18		N/A	N/A	NC	Reverse		
AE14	NC19		N/A	N/A	NC	Reverse		
AD14	NC20		N/A	N/A	NC	Reverse		
AE17	NC21		N/A	N/A	NC	Reverse		
AD17	NC22		N/A	N/A	NC	Reverse		
AE15	NC23		N/A	N/A	NC	Reverse		
AD15	NC24		N/A	N/A	NC	Reverse		
AE18	NC25		N/A	N/A	NC	Reverse		
AD18	NC26		N/A	N/A	NC	Reverse		
Y14	NC27		N/A	N/A	NC	Reverse		
AA14	NC28		N/A	N/A	NC	Reverse		
Part T								
P24	ADC_IN0	A			BAT_DET	Battery voltage input		SARADC
P21	ADC_IN1	A			ADKEY_IN	AD keyboard input		
P23	ADC_IN2	A			GPS_LRADC	GPS VTUNE ADC input		

RK3288 IO LIST

Editor: Lin Xu				Ver: 1.0			Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
R20	ADC_AVDD_1V8	AP			ADC_AVDD_1V8	SAR-ADC analog power supply		
Part U								
B27	HSIC_STROBE	A			HSIC_STROBE	HSIC data strobe signal		HSIC
A27	HSIC_DATA	A			HSIC_DATA	HSIC DDR data signal		
H20	HSIC_AVDD_1V2	AP			HSIC_AVDD_1V2	HSIC Transmitter power supply		
Part V								
AG27	MIPI_TX_D0P	A			MIPI_TX_D0P	MIPI-DSI differential lane 0 positive		MIPI_TX
AG28	MIPI_TX_D0N	A			MIPI_TX_D0N	MIPI-DSI differential lane 0 negative		
AF27	MIPI_TX_D1P	A			MIPI_TX_D1P	MIPI-DSI differential lane 1 positive		
AF28	MIPI_TX_D1N	A			MIPI_TX_D1N	MIPI-DSI differential lane 1 negative		
AE27	MIPI_TX_CLKP	A			MIPI_TX_CLKP	MIPI-DSI differential clock lane positive		
AE28	MIPI_TX_CLKN	A			MIPI_TX_CLKN	MIPI-DSI differential clock lane negative		
AD27	MIPI_TX_D2P	A			MIPI_TX_D2P	MIPI-DSI differential lane 2 positive		
AD28	MIPI_TX_D2N	A			MIPI_TX_D2N	MIPI-DSI differential lane 2 negative		
AC27	MIPI_TX_D3P	A			MIPI_TX_D3P	MIPI-DSI differential lane 3 positive		
AC28	MIPI_TX_D3N	A			MIPI_TX_D3N	MIPI-DSI differential lane 3 negative		
AE26	MIPI_TX_REXT	A			MIPI_TX_REXT	MIPI-DSI reference current generate,connect a 4.02K%1 resistor to VSS		
AC22	MIPI_TX_AVDD_1V8	AP			MIPI_TX_AVDD_1V8	MIPI-DSI power supply		
Part W								
AG23	MIPI_RX_D0P	A			MIPI_RX_D0P	MIPI-CSI differential lane 0 positive		MIPI_RX
AH23	MIPI_RX_D0N	A			MIPI_RX_D0N	MIPI-CSI differential lane 0 negative		
AG24	MIPI_RX_D1P	A			MIPI_RX_D1P	MIPI-CSI differential lane 1 positive		
AH24	MIPI_RX_D1N	A			MIPI_RX_D1N	MIPI-CSI differential lane 1 negative		
AG25	MIPI_RX_CLKP	A			MIPI_RX_CLKP	MIPI-CSI differential clock lane positive		
AH25	MIPI_RX_CLKN	A			MIPI_RX_CLKN	MIPI-CSI differential clock lane negative		
AG26	MIPI_RX_D2P	A			MIPI_RX_D2P	MIPI-CSI differential lane 2 positive		
AH26	MIPI_RX_D2N	A			MIPI_RX_D2N	MIPI-CSI differential lane 2 negative		
AH28	MIPI_RX_D3P	A			MIPI_RX_D3P	MIPI-CSI differential lane 3 positive		
AH27	MIPI_RX_D3N	A			MIPI_RX_D3N	MIPI-CSI differential lane 3 negative		
AD21	MIPI_RX_REXT	A			MIPI_RX_REXT	MIPI-CSI reference current generate,connect a 4.02K%1 resistor to VSS		
AC20	MIPI_RX_AVDD_1V8	AP			MIPI_RX_AVDD_1V8	MIPI-CSI power supply		
Part X								
AE20	MIPI_TX/RX_D0P	A			MIPI_TX/RX_D0P	MIPI-DSI/CSI differential lane 0 positive		
AF20	MIPI_TX/RX_D0N	A			MIPI_TX/RX_D0N	MIPI-DSI/CSI differential lane 0 negative		
AE21	MIPI_TX/RX_D1P	A			MIPI_TX/RX_D1P	MIPI-DSI/CSI differential lane 1 positive		
AF21	MIPI_TX/RX_D1N	A			MIPI_TX/RX_D1N	MIPI-DSI/CSI differential lane 1 negative		

RK3288 IO LIST

Editor: Lin Xu					Ver: 1.0		Date: 2014-04-29	
Pin	**Ball Pin Name**	**Pad type**	**IO Pull**	**Reset State**	**Default function**	**Defual function description**	**Function 2**	**IO Domain**
AE23	MIPI_TX/RX_CLKP	A			MIPI_TX/RX_CLKP	MIPI-DSI/CSI differential clock lane positive		MIPI_TX/RX
AF23	MIPI_TX/RX_CLKN	A			MIPI_TX/RX_CLKN	MIPI-DSI/CSI differential clock lane negative		
AE24	MIPI_TX/RX_D2P	A			MIPI_TX/RX_D2P	MIPI-DSI/CSI differential lane 2 positive		
AF24	MIPI_TX/RX_D2N	A			MIPI_TX/RX_D2N	MIPI-DSI/CSI differential lane 2 negative		
AF25	MIPI_TX/RX_D3P	A			MIPI_TX/RX_D3P	MIPI-DSI/CSI differential lane 3 positive		
AD25	MIPI_TX/RX_D3N	A			MIPI_TX/RX_D3N	MIPI-DSI/CSI differential lane 3 negative		
AD22	MIPI_TX/RX_REXT	A			MIPI_TX/RX_REXT	MIPI-DSI/CSI reference current generate,connect a 4.02K%1 resistor to VSS		
AC21	MIPI_TX/RX_AVDD_1V8	AP			MIPI_TX/RX_AVDD_1V8	MIPI-DSI/CSI power supply		