


Reference Schematic For RK1808

RK1808_Ref_Bref_V1.0

PMIC: RK809-2 (5BUCK + 9LDO + Codec)
RAM: DDR3 /LPDDR3/DDR4
ROM: eMMC + TF card
Interface: MIPI CSI/MIPI DSI/UART/I2S/RMII/LCDC/PCIE/USB3

Rockchip Confidential

 Fuzhou Rockchip Electronics	
Project: RK_EVB_1808_lp3_sch_V12	
File: 00.Cover Page	
Date: Friday, February 15, 2019	Rev: V1.0
Designed by: Raf	Sheet: 0 of 99

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Note

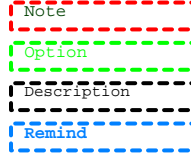
NOTE 1:

Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2:

Please use our recommended components to avoid too many changes. For more informations about the second source, please refer to our AVL.



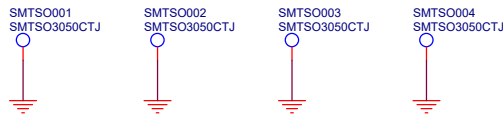
Bill of Materials

Header:

Item\Part\Description\PCB Footprint\Reference\Quantity\Option


Combined property string:

{Item}\{Value}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}



Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project: RK_EVB_1808_lp3_sch_V12			
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Version	Date	Author	Change List	Approved
V1.0	20180712		First edition for RK1808	RZF
V1.1	20181107			RZF
V1.2	20190215		1.PLL_AVDD_0V8(pin ac15)电源供电改成VDDA_0V8;PLL_AVDD_1V8(pin aa15)供电改成VCCA_1V8. 2.ADC_AVDD_1V8(pin N31)电源供电改成VCCA_1V8. 3.C6105 电容22P改成18P. 4.C2001 电容改成100nF,C2004 电容改成100P.	RZF

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Project: RK_EVB_1808_ip3_sch_V12	
File: 02.Revision History	
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5

4

3

2

1

D

D

C

C

B

B

A

A


5

4

3


2

1

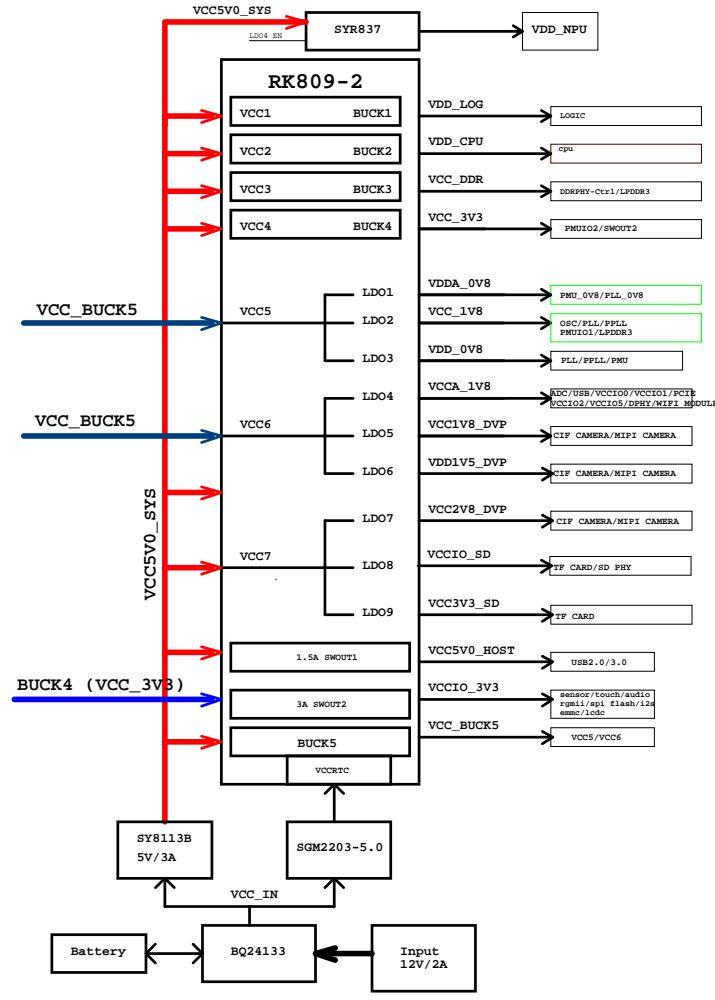
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Project:	RK_EVb_1808_lp3_sch_V12
File:	03.Block Diagram
Date:	Friday, February 15, 2019
Designed by:	Rzf
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I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	I2C0_SCL/GPI00_B0_u I2C0_SDA/GPI00_B1_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC_3V3	Rockchip RK809	0x20	PMIC	100kHz, 400kHz
					SY837		BUCK	100kHz, 400kHz
I2C1	I2C1_SCL/GPI00_C0_u I2C1_SDA/GPI00_C1_u	PMUIO2	I2C1_SCL I2C1_SDA	VCC_3V3	GSL1680		Touch IC	100kHz, 400kHz
								100kHz, 400kHz
I2C2	I2C1_SCL/GPI01_B4_U I2C1_SDA/GPI01_B5_U	VCCIO_3V3			NC			100kHz, 400kHz
I2C3	GPIO2_D0/I2C3_SCL_U GPIO2_D1/I2C3_SDA_U	VCCA_1V8		VCCA_1V8	MIPI CAMERA			
					CIF CAMERA			
					BT1120			
I2C4	GPIO3_C2/I2C4_SCL_U GPIO3_C3/I2C4_SDA_U	VCCIO_3V3		VCCIO_3V3	DIGITAL MIC			
					RGB LCD			
					PCIEX4			
					SENSOR			

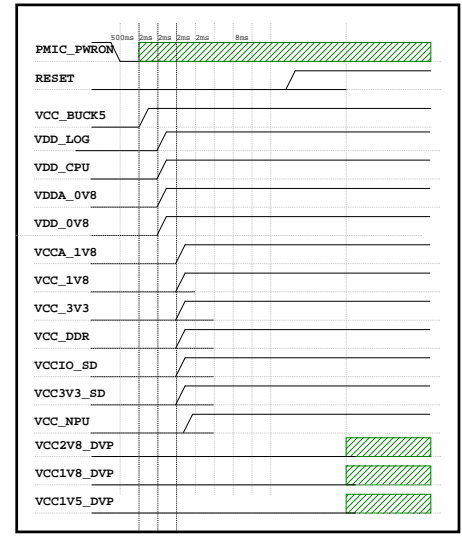
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Project:	RK_EVB_1808_ip3_sch_V12
File:	04.I2C MAP
Date:	Friday, February 15, 2019
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POWER DIAGRAM



RK809-2 Power-on Sequence

PowerName	PMIC Channel	Time Slot (step, 2ms)	Default Voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VCC_0V9	EXTERNAL(SY837)	S105-13A	1V	6A	ON	OFF	4A
VDD_DAG	BUCK3	S105-12	0.85V	2.5A	ON	OFF	1.25A
VCC_0V9	BUCK3	S105-12	0.85V	2.5A	ON	OFF	1.25A
VCC_0V8	BUCK1	S105-13	FB+0.5V	1.5A	ON	ON	150mA
VCC_1V8	BUCK4	S105-14	1.8V	1.5A	ON	ON	ON
VCC_BUCK5	BUCK5	S105-15	2.5V	2.5A	ON	ON	ON
VCC_1V8	LDO2	S105-13	0.8V	400mA	ON	ON	ON
VDD_0V8	LDO3	S105-12	0.8V	100mA	ON	ON	ON
VCC_1V8	LDO4	S105-13	1.8V	500mA	ON	OFF	OFF
VCC1V8_DVP	LDO5	S105-13	1.8V	400mA	OFF	OFF	OFF
VDD1V5_DVP	LDO6	S105-13	1.5V	400mA	OFF	OFF	OFF
VCC2V8_DVP	LDO7	S105-13	2.8V	400mA	OFF	OFF	OFF
VCCIO_0V	LDO8	S105-14	1.8V	400mA	ON	OFF	OFF
VCC3V3_SD	LDO9	S105-14	3.3V	400mA	ON	OFF	OFF
VCCIO_3V3	SWOUT2	S105-14	3.3V	3A	ON	OFF	OFF
VCC5V0_HOST	SWOUT1	S105-14	5V	1.5A	OFF	OFF	OFF
RESET	RES07B	S105-10	0V				



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Project: RK_EVB_1808_ip3_sch_V12

File: 05.Power diagram and Sequence

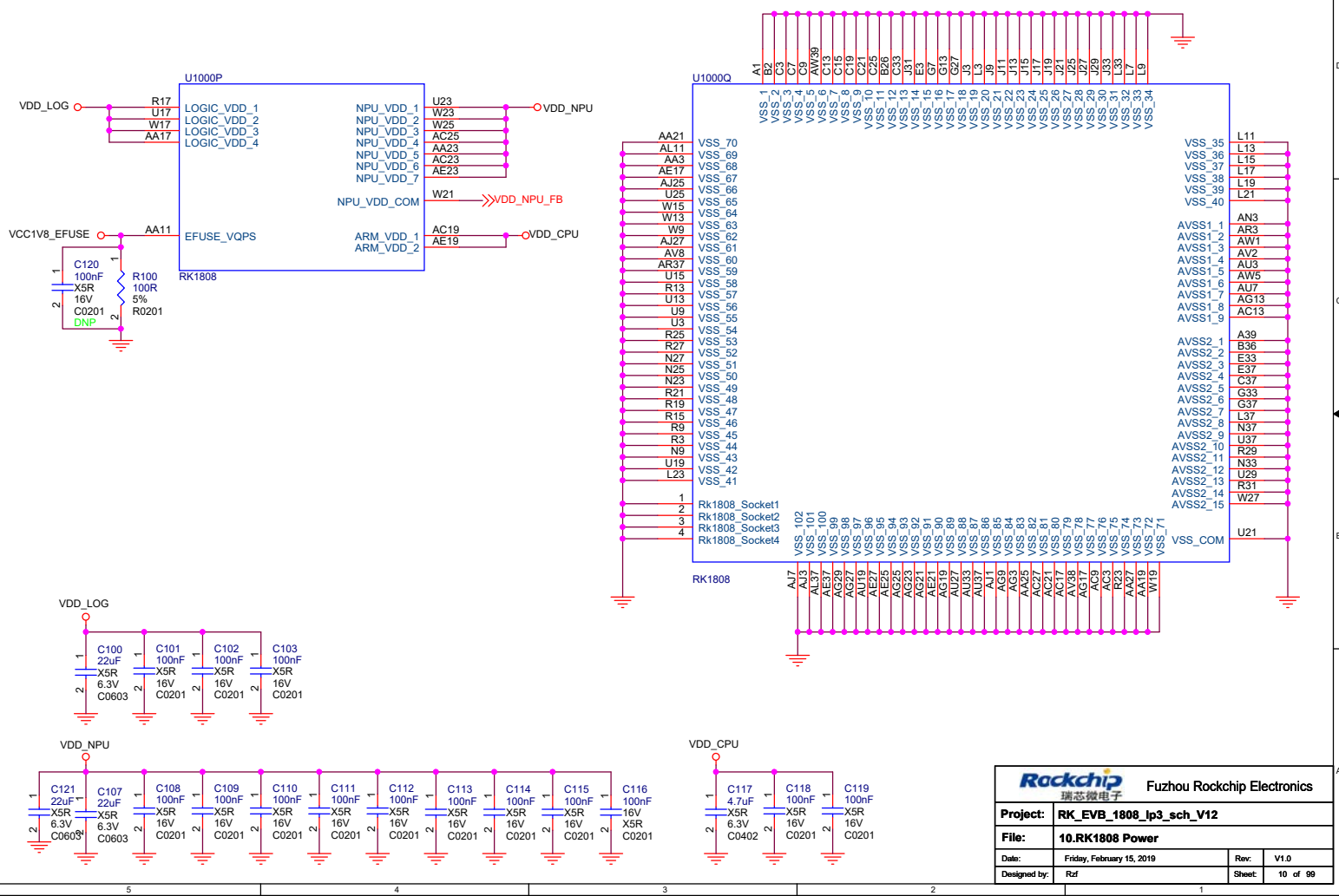
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Rev: V1.0

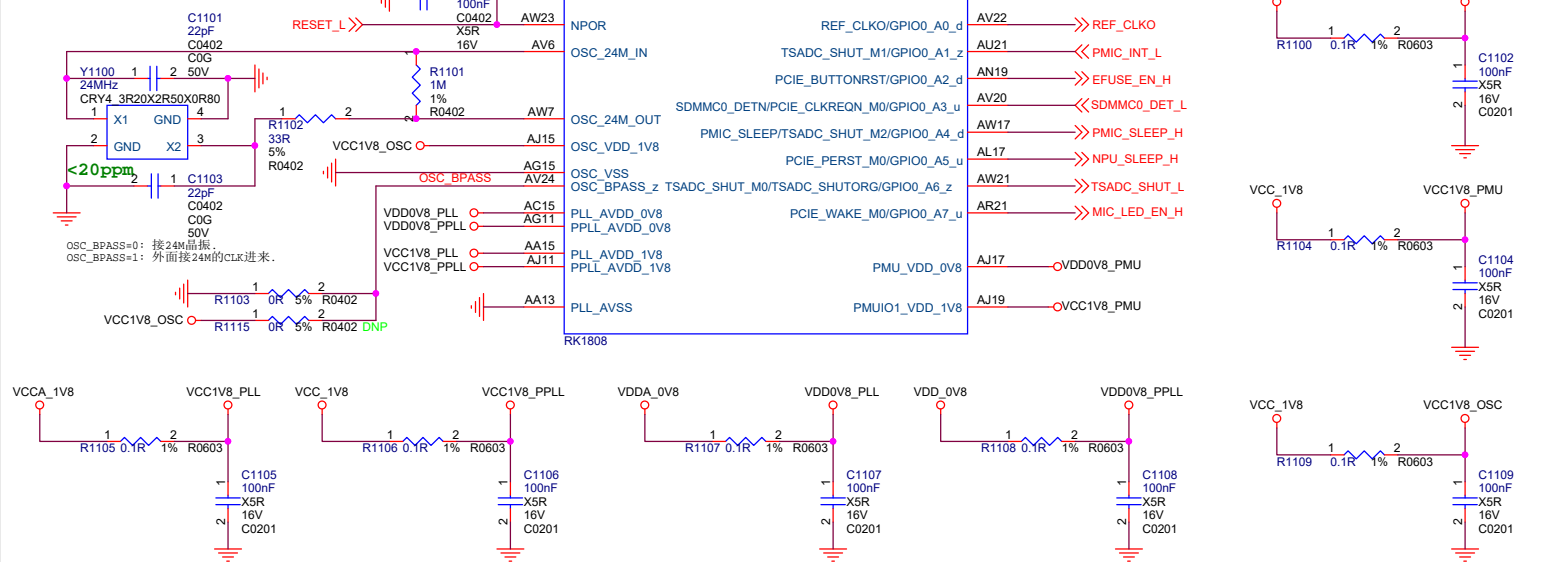
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RK1808 Power

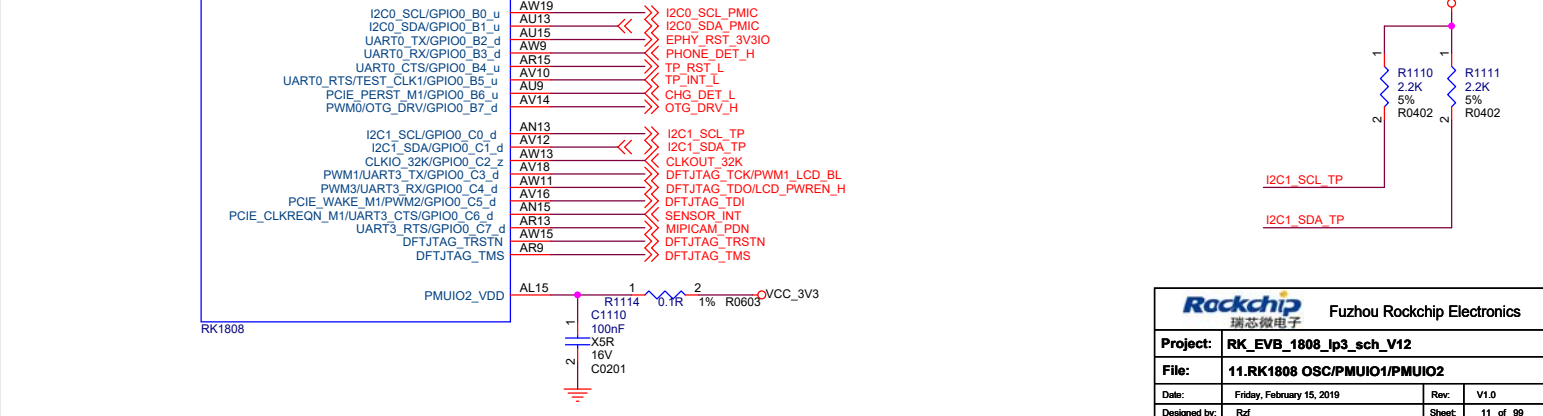


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Project:	RK_EVB_1808_ip3_sch_V12		
File:	10.RK1808 Power		
Date:	Friday, February 15, 2019	Rev:	V1.0
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PMUIO1 / OSC



PMUIO2

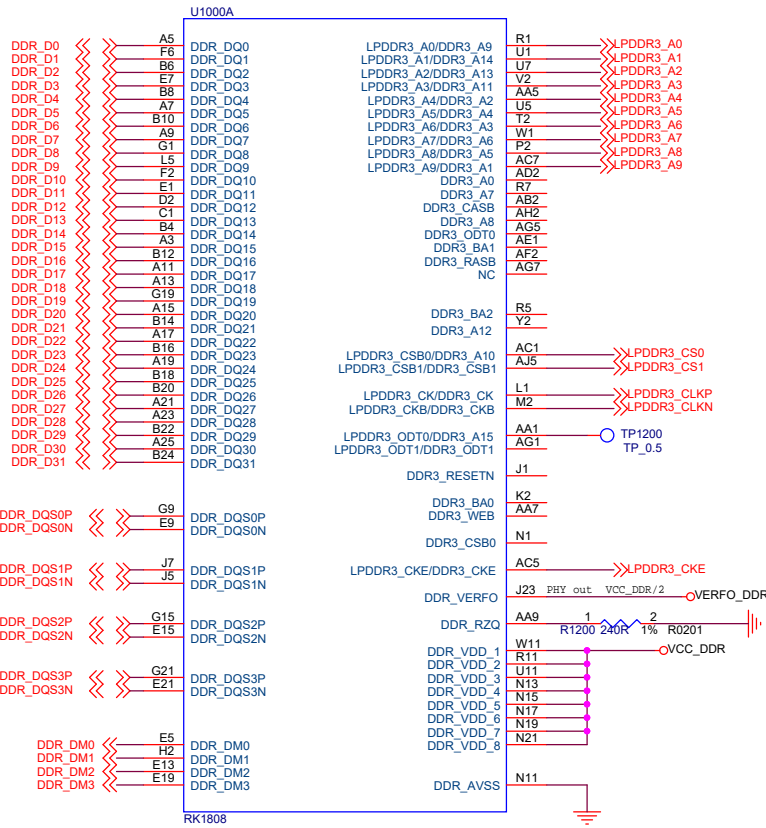


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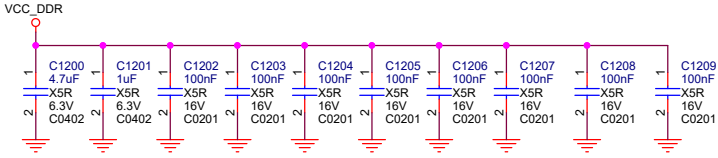
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Project:	RK_EVB_1808_ip3_sch_V12		
File:	11.RK1808 OSC/PMUIO1/PMUIO2		
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DDR Controller



LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
	A0
	A7
	CASB
	A8
	ODT0
	BA1
	RASB
	CSB0
	BA2
	A12
	BA0
	WEB
CK	CK
CKE	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
	RESETN



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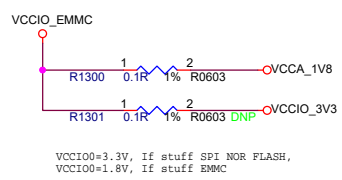
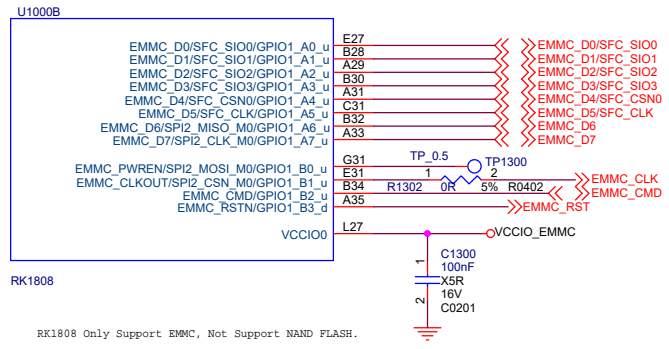
Project: RK_EVB_1808_ip3_sch_V12

File: 12.RK1808 DDR Controller

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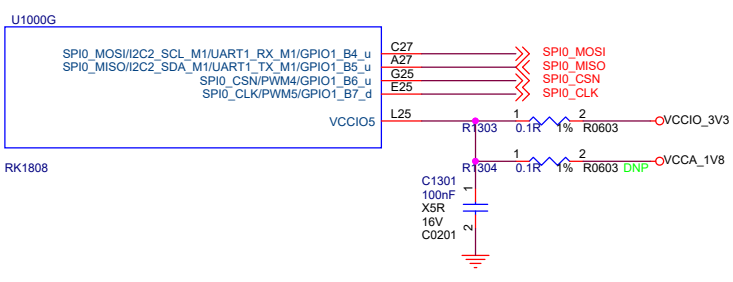
EMMC/SFC Controller



RK1808

RK1808 Only Support EMMC, Not Support NAND FLASH.

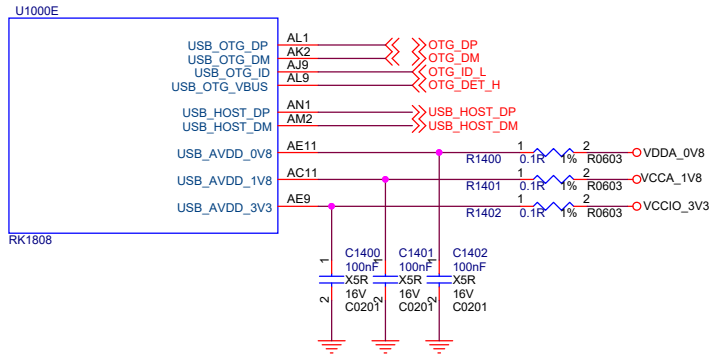
SPI0 Controller



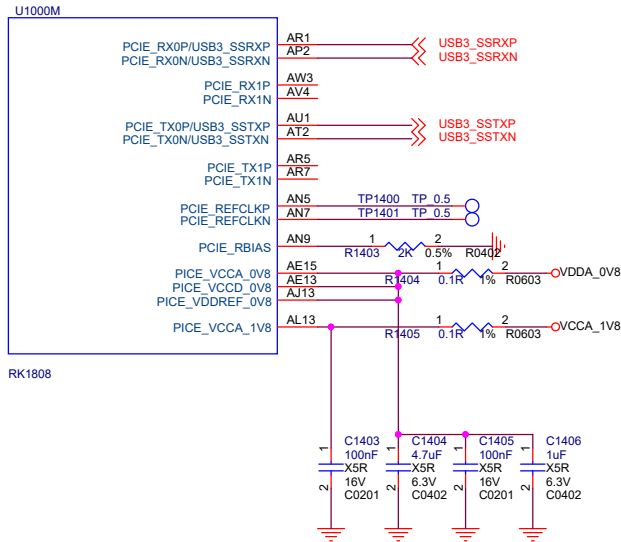
RK1808

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Project:	RK_EVB_1808_ip3_sch_V12		
File:	13.RK1808 EMMC /SPI Controller		
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USB Controller

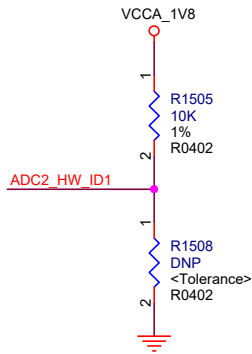
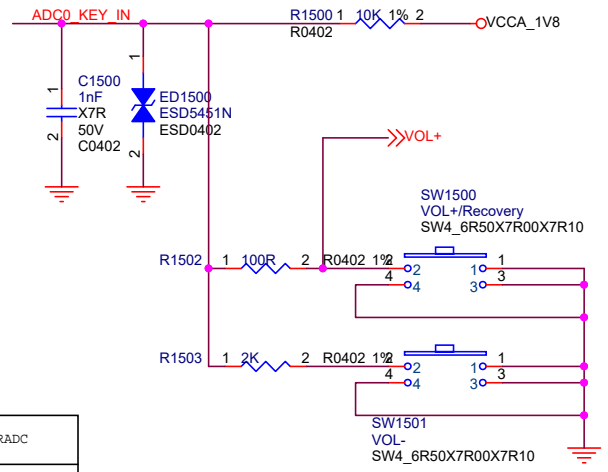
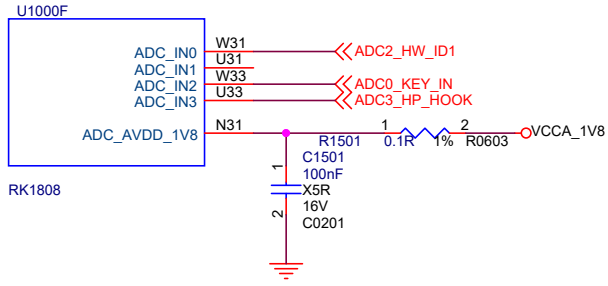


PCIE Controller



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Project:	RK_EVB_1808_ip3_sch_V12		
File:	14.RK1808 USB/PCIE Controller		
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SARADC/KEY

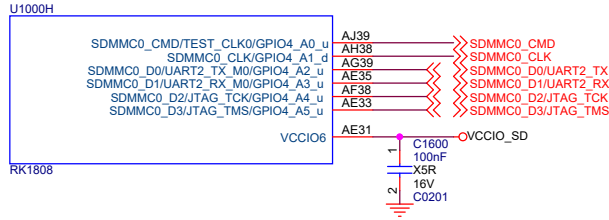


Key Name	SARADC
VOL+/RECOVERY	10
VOL-	170

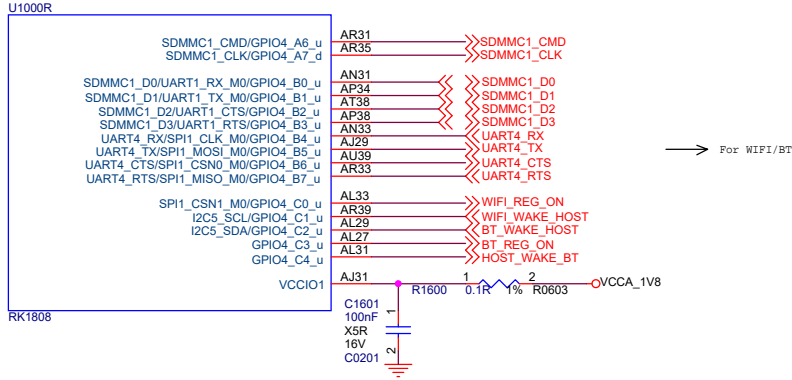
Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics

Project:	RK_EVB_1808_ip3_sch_V12		
File:	15.RK1808 SARADC/KEY		
Date:	Friday, February 15, 2019	Rev:	V1.0
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SDMMC0 Controller



SDMMC1 Controller

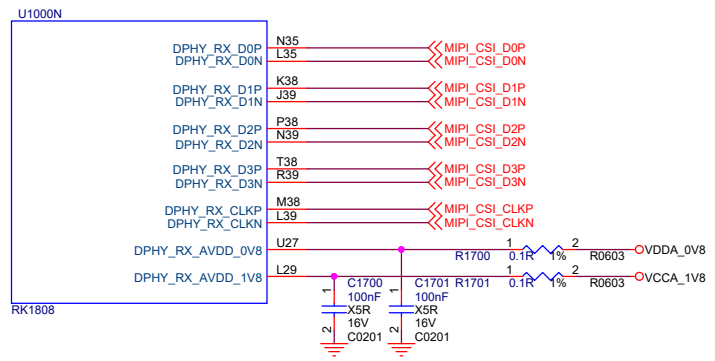


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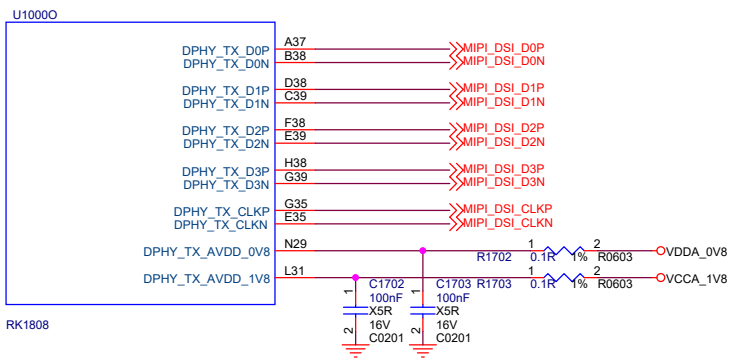
Fuzhou Rockchip Electronics

Project:	RK_EVB_1808_ip3_sch_V12		
File:	16.RK1808 SDMMC0/SDMMC1		
Date:	Friday, February 15, 2019	Rev:	V1.0
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MIPI CSI Controller



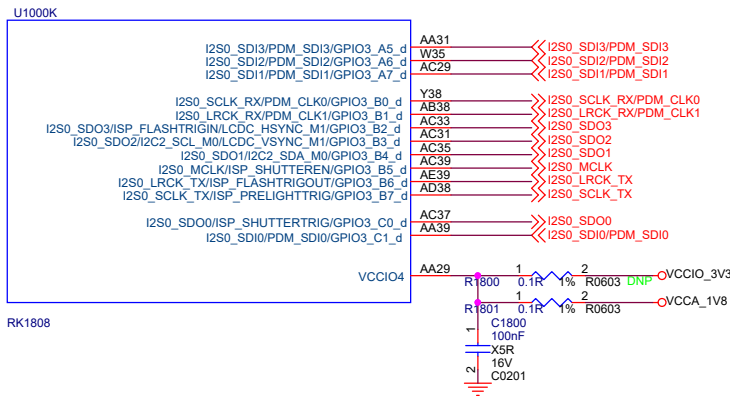
MIPI DSI Controller



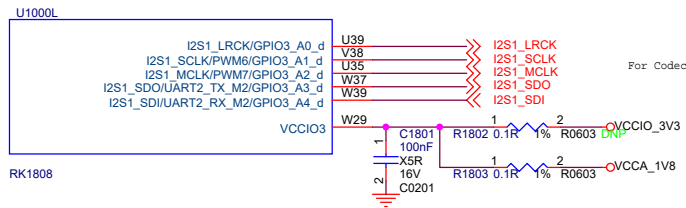
Rackchip 瑞芯微电子 Fuzhou Rockchip Electronics

Project:	RK_EVB_1808_ip3_sch_V12		
File:	17.RK1808 MIPI DSI/CSI		
Date:	Friday, February 15, 2019	Rev:	V1.0
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I2S0 Controller

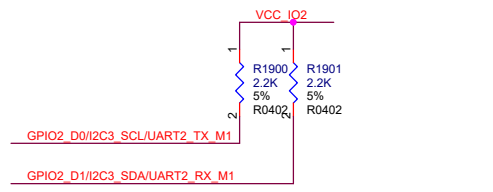
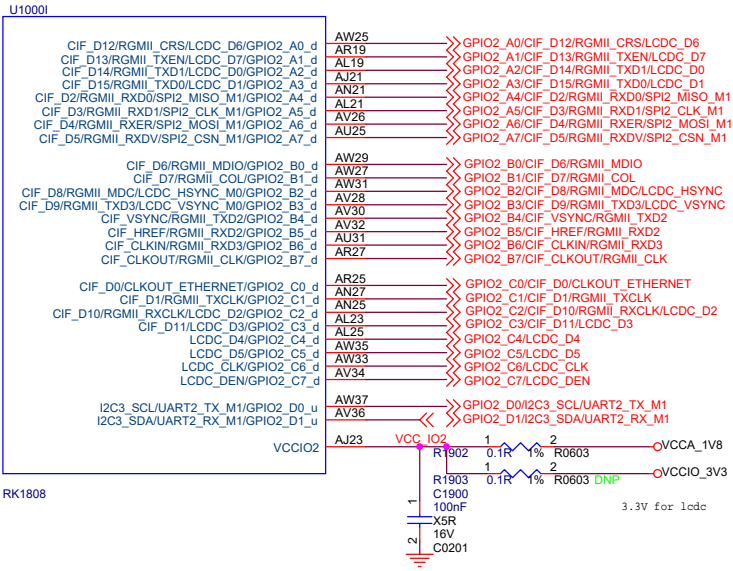


I2S1 Controller

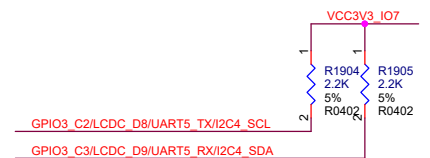
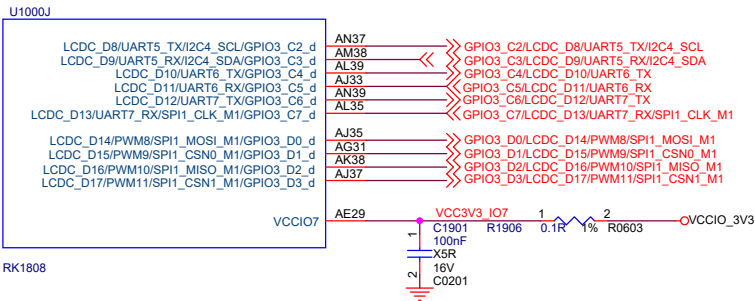


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Project:	RK_EVB_1808_ip3_sch_V12		
File:	18.RK1808 I2S0/I2S1		
Date:	Friday, February 15, 2019	Rev:	V1.0
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CIF/RGMII/LCDC Controller

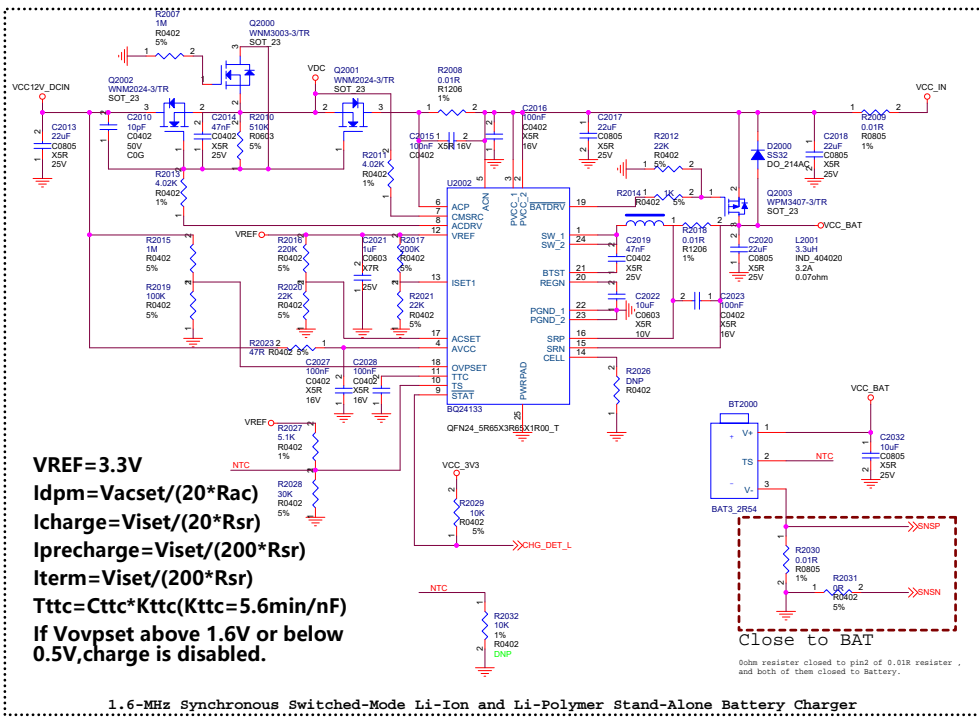
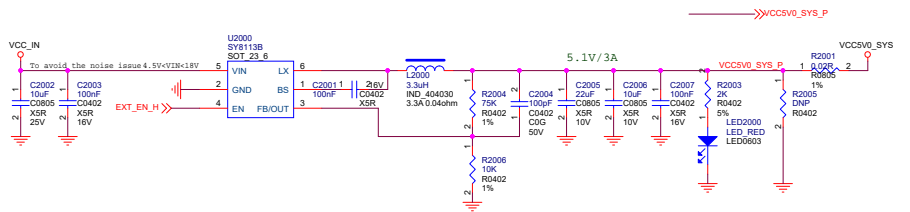
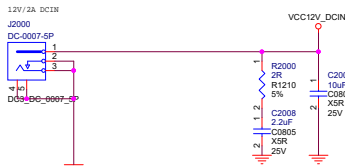


LCDC Controller



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Project: RK_EVB_1808_ip3_sch_V12			
File: 19.RK1808 RGMII/LCDC/CIF			
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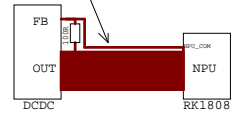
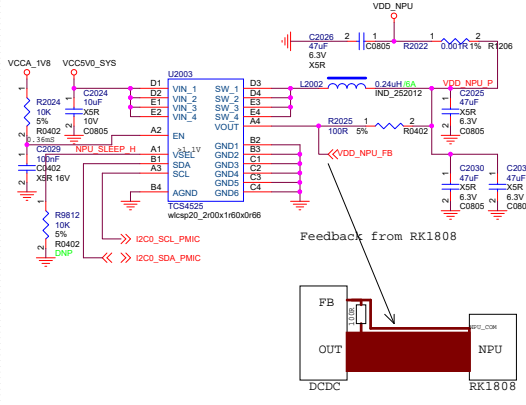
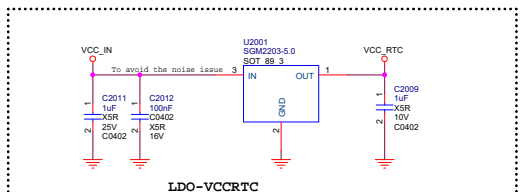
DC IN&SYSTEM Power



VREF=3.3V
 $I_{dpm} = V_{acset} / (20 * R_{ac})$
 $I_{charge} = V_{iset} / (20 * R_{sr})$
 $I_{precharge} = V_{iset} / (200 * R_{sr})$
 $I_{term} = V_{iset} / (200 * R_{sr})$
 $t_{ttc} = Ct_{tc} * K_{ttc} (K_{ttc} = 5.6 \text{min/nF})$
 If Vovpset above 1.6V or below 0.5V, charge is disabled.

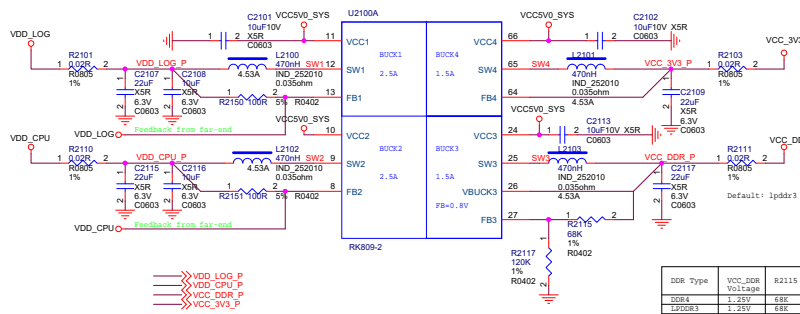
1.6-MHz Synchronous Switched-Mode Li-Ion and Li-Polymer Stand-Alone Battery Charger

Close to BAT
 0ohm resistor closed to pin2 of 0.01R resistor and both of them closed to Battery.

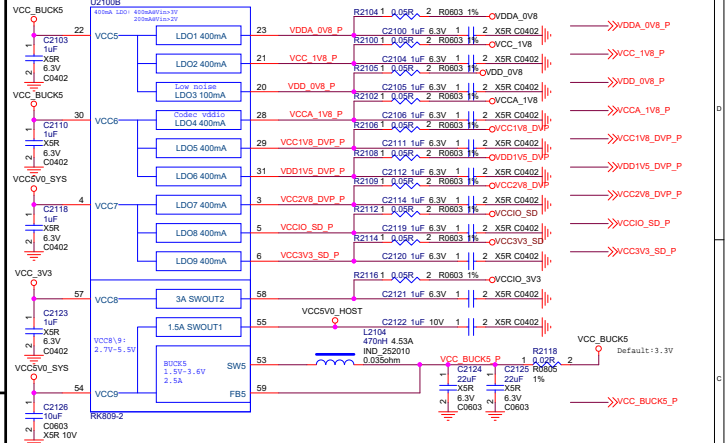


Rockchip Fuzhou Rockchip Electronics	
Project:	RK_EVB_1808_lp3_sch_V12
File:	20_Power-DC IN
Date:	Friday, February 15 2019
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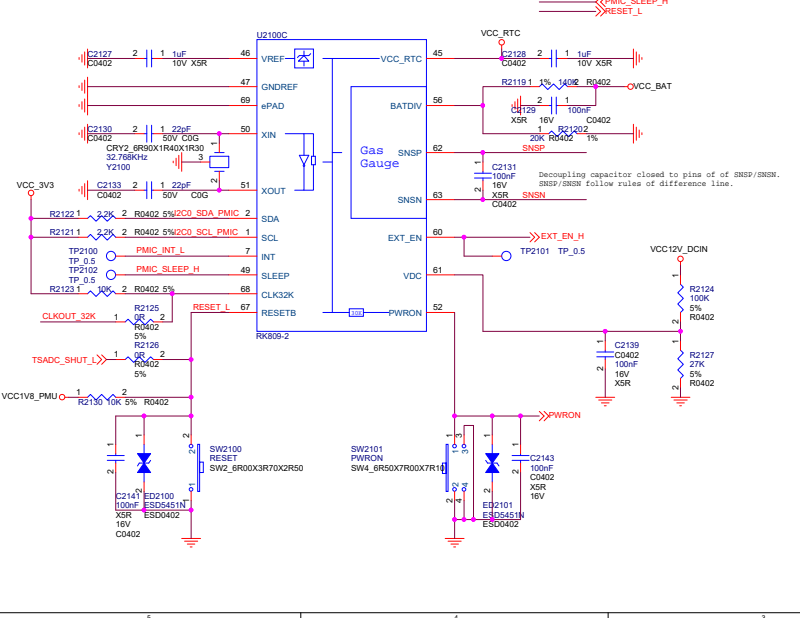
PMIC RK809-1 DCDC



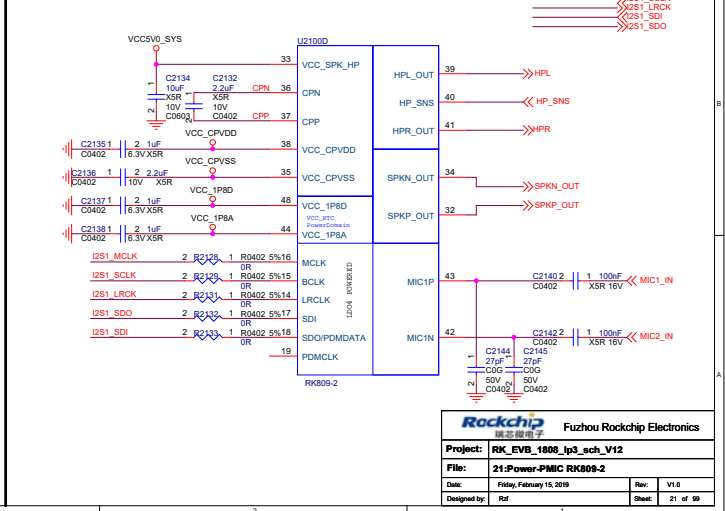
PMIC RK809-1 LDO



PMIC RK809-1 Management



PMIC RK809-1 CODEC



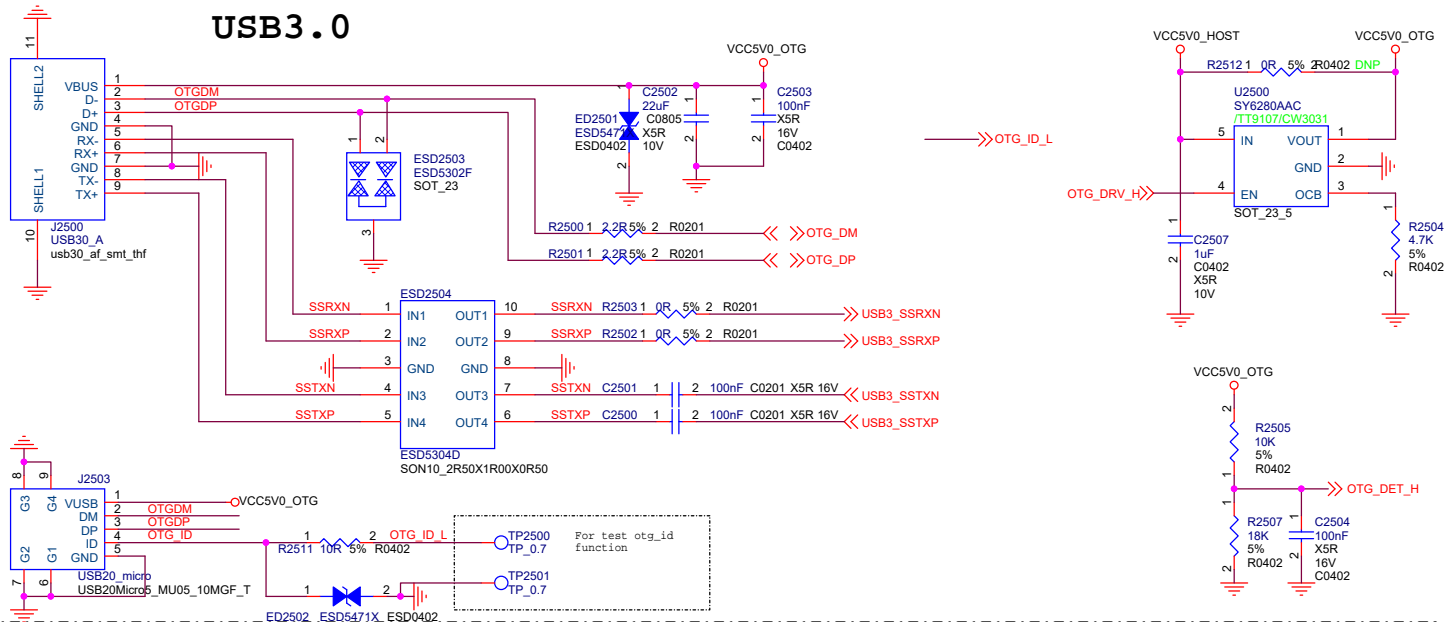
Rockchip
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Project: RK_EVb_1808_lp3_sch_V12
File: 21-Power-PMIC RK809-2

Date: Friday, February 15, 2019
Designed by: Raf

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USB3.0

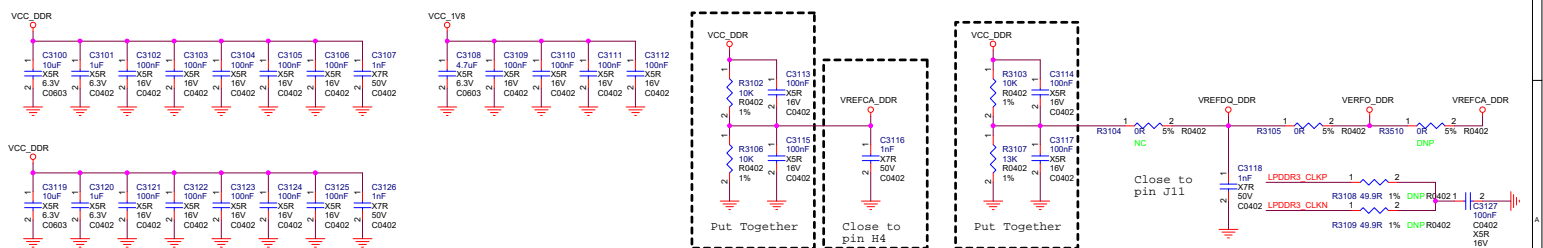
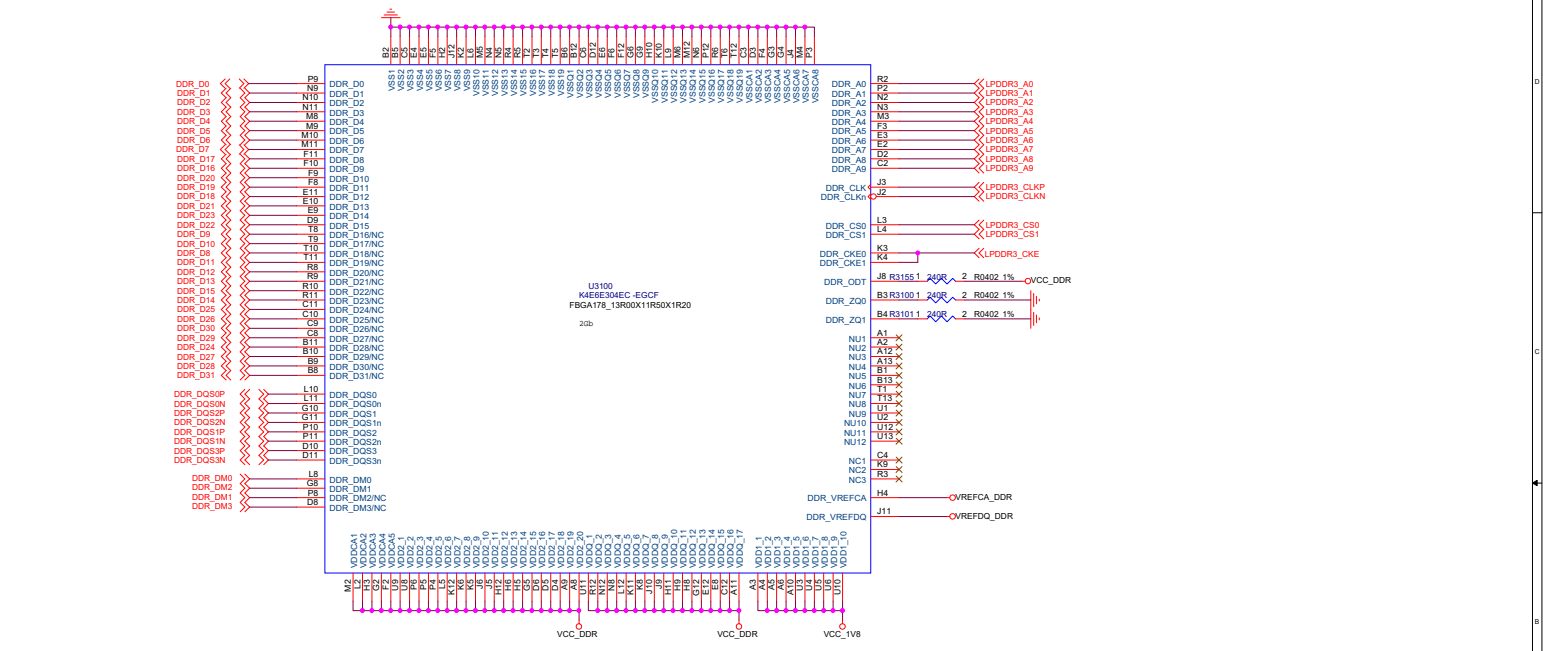


USB HOST



Rackchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project: RK_EVB_1808_Ip3_sch_V12			
File: 25.USB 3.0/USB2.0 HOST			
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LPDDR3 1x32bit



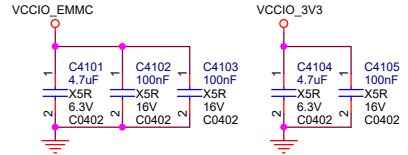
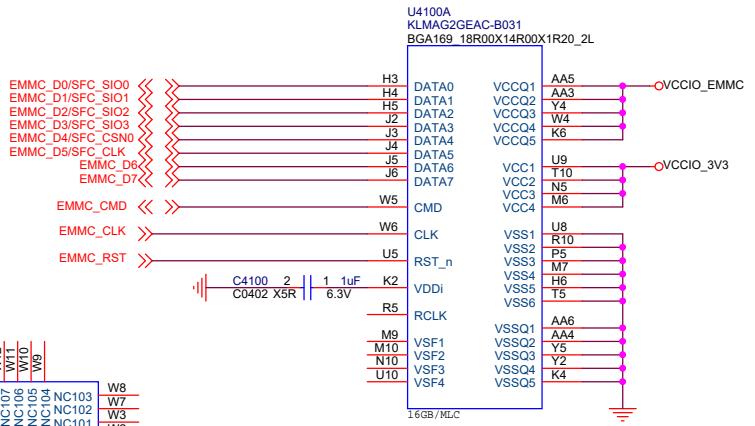
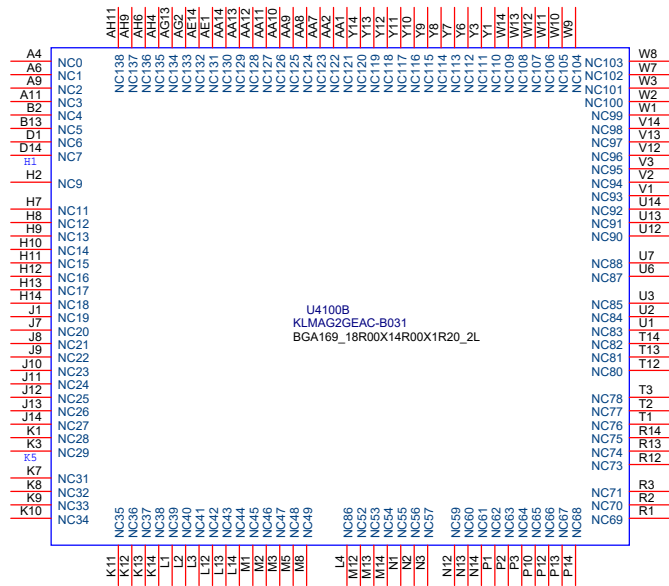
Note:
 $V_{ih} = VCC$
 $V_{il} = VCC * Ron / (Ron + Rodt)$
 $VREFDQ_DDR = (V_{ih} + V_{il}) / 2$
 eg: $VCC = 1.2V, Ron = 34ohm, Rodt = 240ohm$
 so, $V_{ih} = 1.2V, V_{il} = 0.149V, VREFDQ_DDR = 0.674V$

Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics

Project: RK_EVB_1808_lp3_sch_V12
 File: 31_RAM-LPDDR3 1x32bit

Date: Friday, February 15, 2019 Rev: V1.0
 Designed by: Raf Sheet: 31 of 99

Note: All the power filter capacitors should be placed close to the power pins of LPDDR3

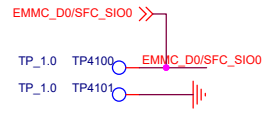


Note:
Reserve TestPoint for firmware update.
If FLASH_CLE=0V at power-on reset,
then system will enter into Maskrom mode.

Maskrom

EMMC_D0/SFC_SIO0

R0400
SW4100
TS-1125HS
SW2_6R00X3R70X2R50

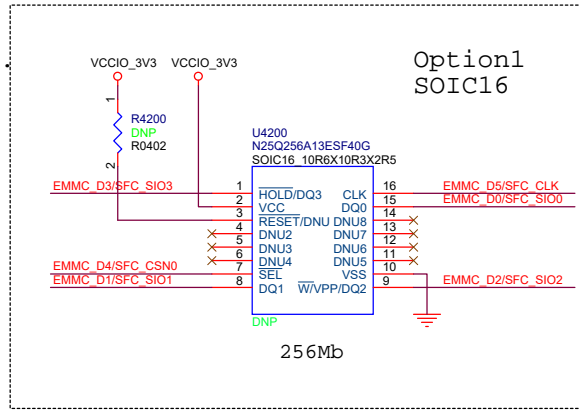
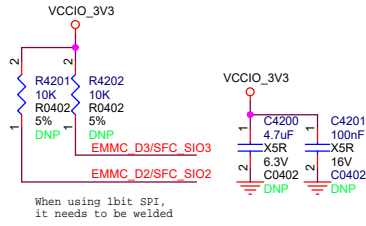


Fuzhou Rockchip Electronics 瑞芯微电子	
Project:	RK_EVB_1808_ip3_sch_V12
File:	41.EMMC
Date:	Friday, February 15, 2019
Designed by:	Rzf
Rev:	V1.0
Sheet:	41 of 99

Remind: Refer to the latest AVL for parts selection.

SPI NOR Flash

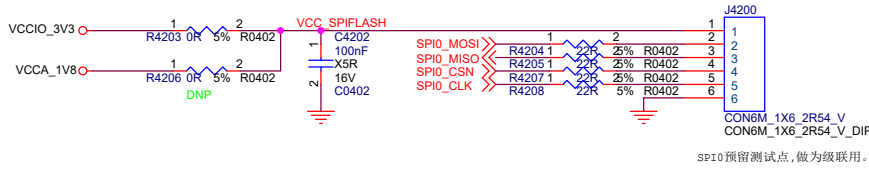
Reserved for minimal system.



- << >>EMMC_D0/SFC_SIO0
- << >>EMMC_D1/SFC_SIO1
- << >>EMMC_D2/SFC_SIO2
- << >>EMMC_D3/SFC_SIO3
- << >>EMMC_D4/SFC_CSNO
- << >>EMMC_D5/SFC_CLK

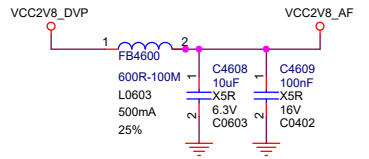
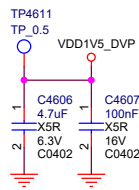
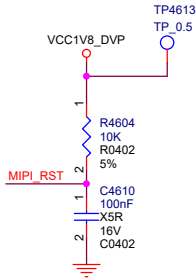
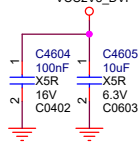
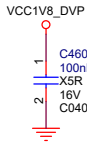
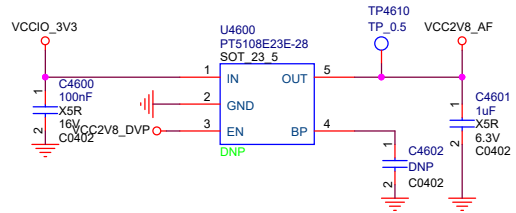
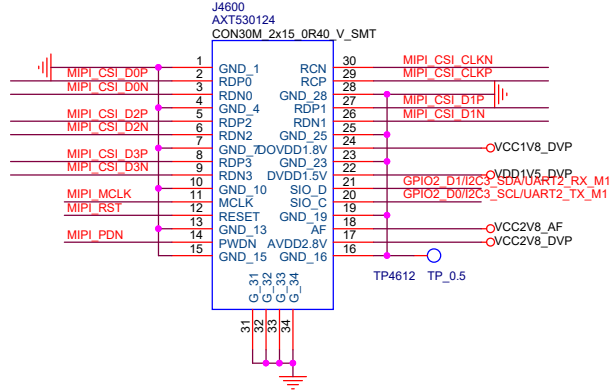
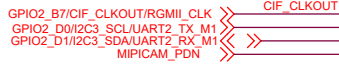
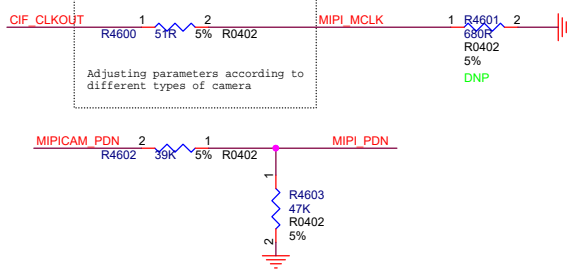
Remind: Refer to the latest AVL for parts selection.

SPI0 Interface



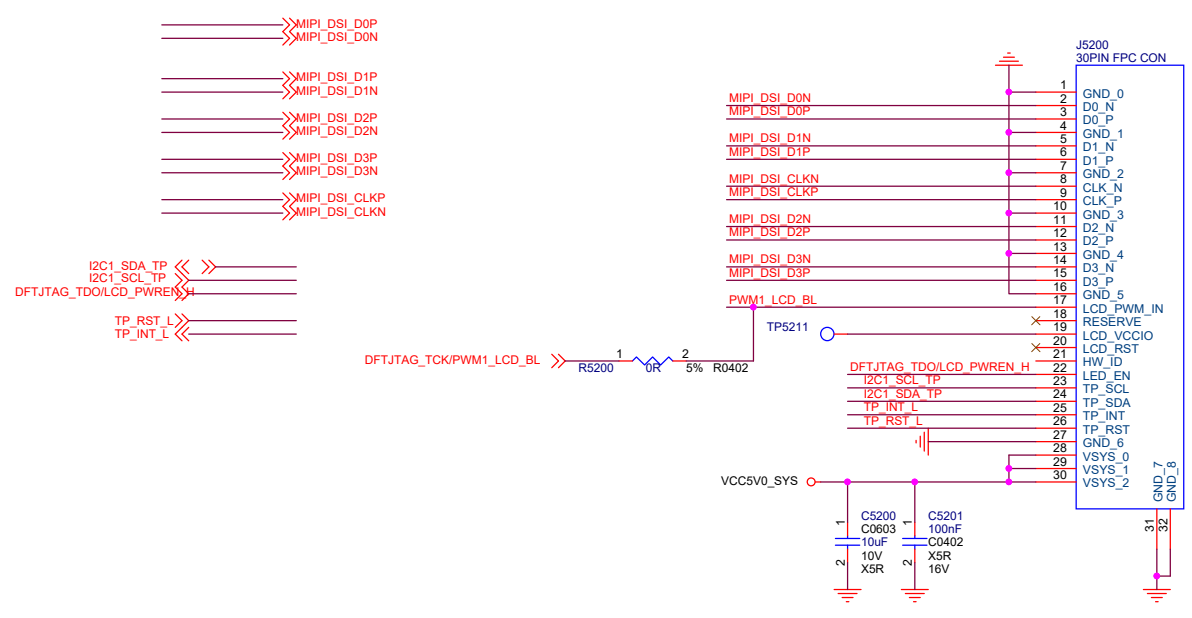
Rackchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK_EVB_1808_ip3_sch_V12		
File:	42.SPI Flash		
Date:	Friday, February 15, 2019	Rev:	V1.0
Designed by:	Rzf	Sheet:	42 of 99

MIPI Camera



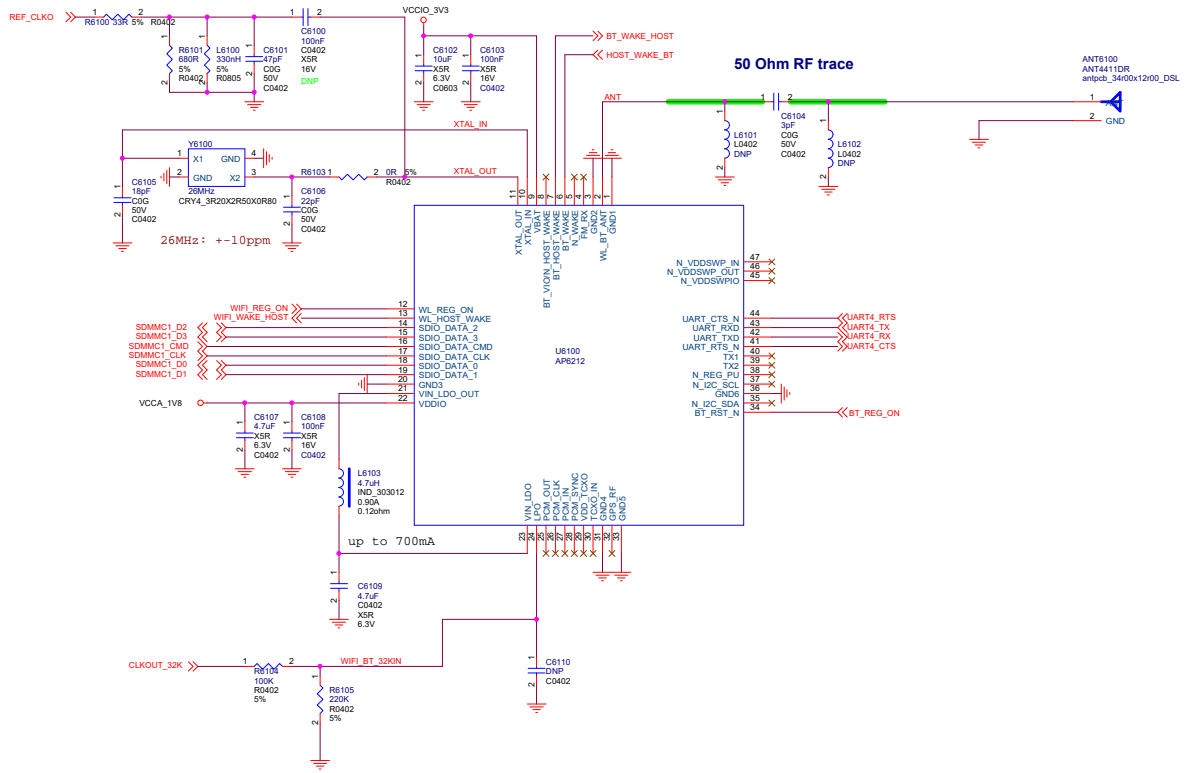
Rackchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK_EVB_1808_ip3_sch_V12		
File:	46.Camera-MIPI CSI		
Date:	Friday, February 15, 2019	Rev:	V1.0
Designed by:	Rzf	Sheet:	46 of 99

MIPI Panel

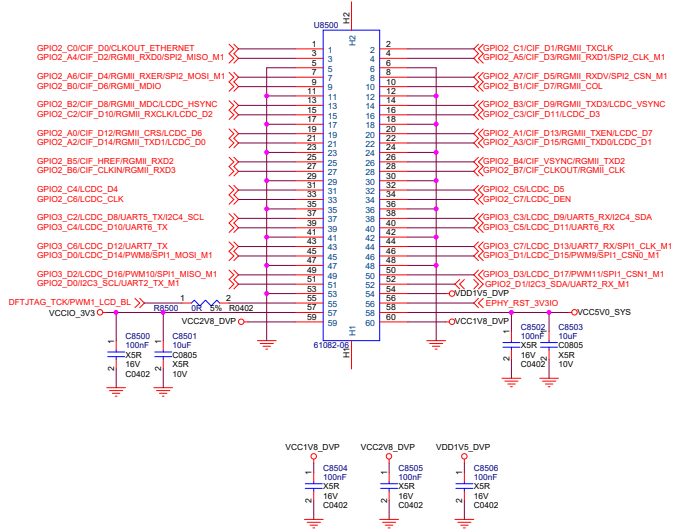
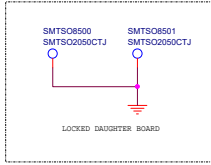


Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project: RK_EVB_1808_ip3_sch_V12			
File: 52.LCM-MIPI Panel			
Date: Friday, February 15, 2019		Rev: V1.0	
Designed by: Rzf		Sheet: 52 of 99	

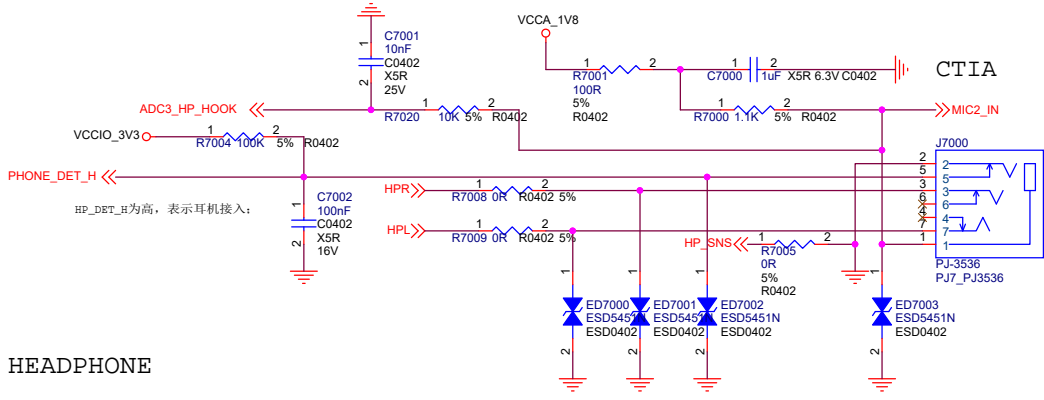
WIFI/BT MODULE



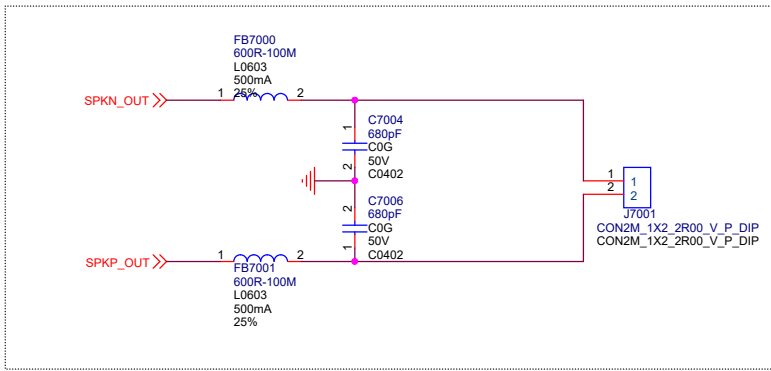
Rockchip 福州岩芯电子		Fuzhou Rockchip Electronics	
Project: RK_EVb_1808_ip3_sch_V12			
File: 61.SDIO WIFI/BT AP6212			
Date: Friday, February 15, 2019	Rev: V1.0		
Designed by: Raf	Sheet: 61 of 99		



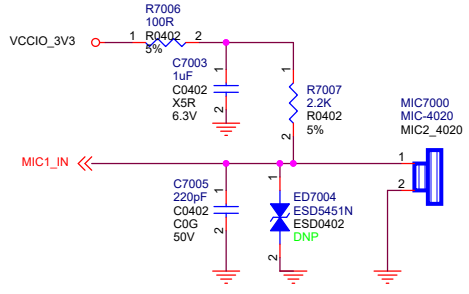
Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project: RK_EVb_1800_ip3_sch_V12			
File: 85.INTERFACE			
Date: Friday, February 15, 2019		Rev: V1.0	
Designed by: Raf		Sheet: 85 of 99	



HEADPHONE

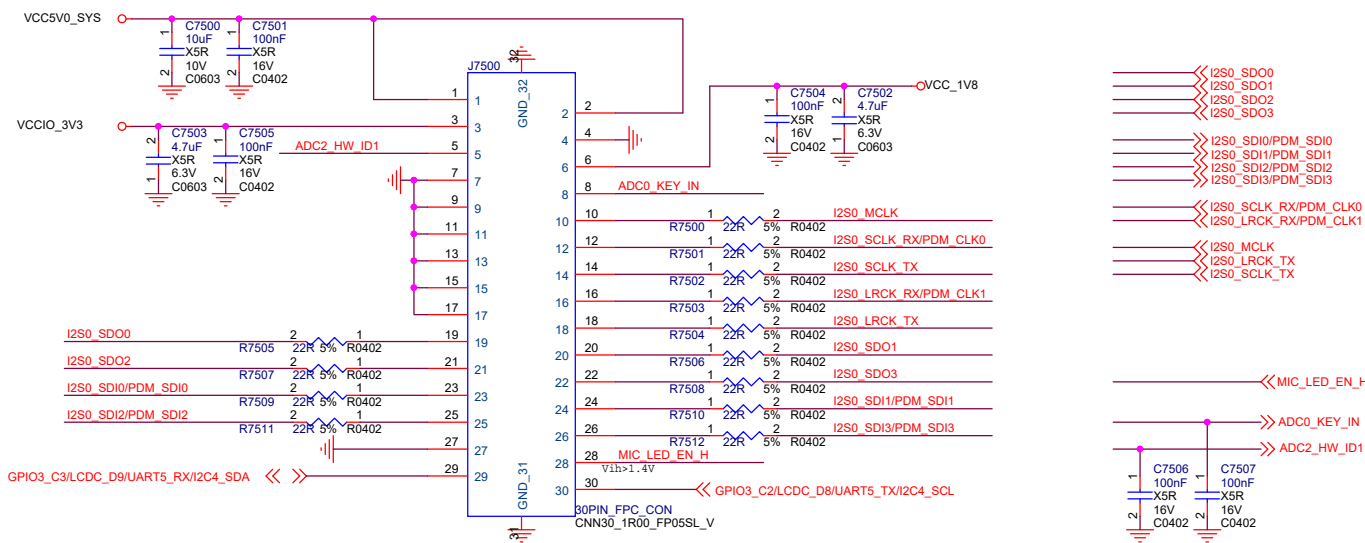


SPEAKER



MIC

Rackchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK_EVB_1808_ip3_sch_V12		
File:	70.AUDIO1		
Date:	Friday, February 15, 2019	Rev:	V1.0
Designed by:	Rzf	Sheet:	70 of 99



MIC Array-Digital Interface

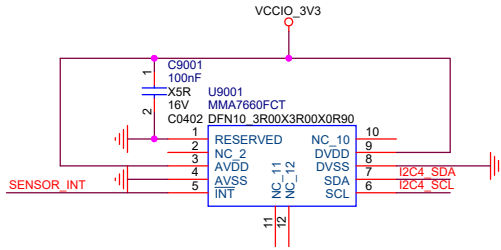
Rackchip 瑞芯微电子
Fuzhou Rockchip Electronics

Project:	RK_EVB_1808_ip3_sch_V12		
File:	75.AUDIO2-MIC Array Connector		
Date:	Friday, February 15, 2019	Rev:	V1.0
Designed by:	Rzf	Sheet:	75 of 99

I2C4_SDA <<< >> GPIO3_C3/LCDC_D9/UART5_RX/I2C4_SDA
 I2C4_SCL <<< >> GPIO3_C2/LCDC_D8/UART5_TX/I2C4_SCL

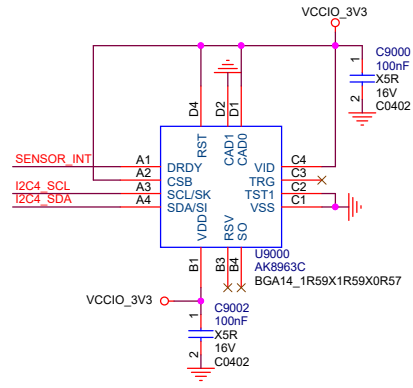
SENSOR_INT

G-sensor



Compass

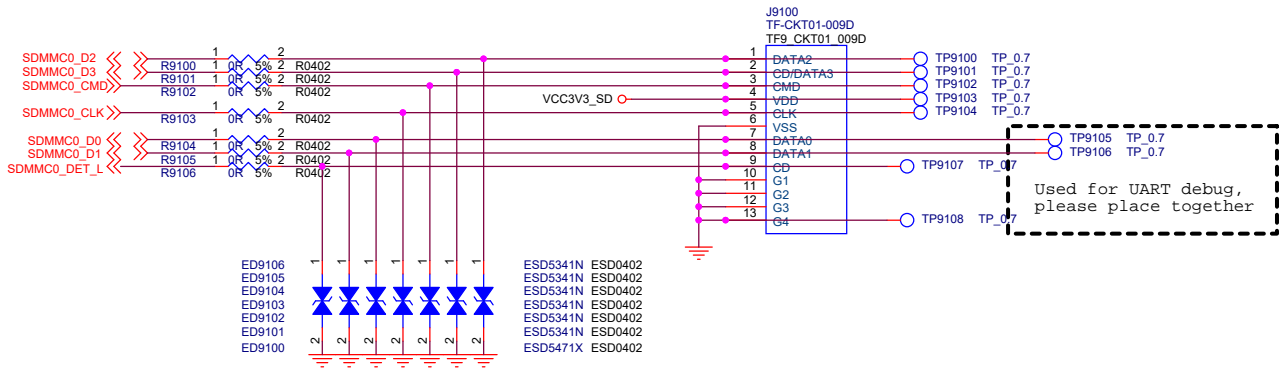
Note:
 The first pin of AK8963C must be place on the lower left corner of PCB.



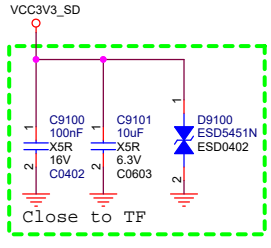
Rackchip 瑞芯微电子 Fuzhou Rockchip Electronics


Project:	RK_EVB_1808_ip3_sch_V12		
File:	90.Sensor		
Date:	Friday, February 15, 2019	Rev:	V1.0
Designed by:	Rzf	Sheet:	90 of 99

TF Card

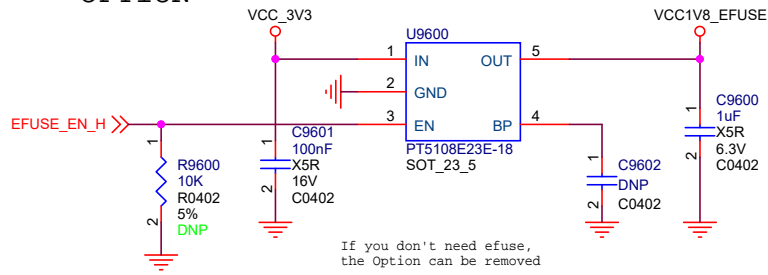



Used for UART debug,
please place together

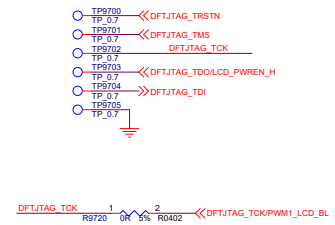
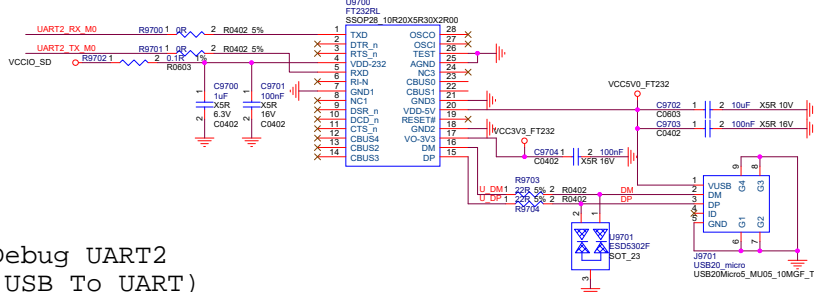


 Fuzhou Rockchip Electronics 瑞芯微电子	
Project:	RK_EVB_1808_ip3_sch_V12
File:	91.TF Card
Date:	Friday, February 15, 2019
Designed by:	Rzf
Rev:	V1.0
Sheet:	91 of 99

OPTION

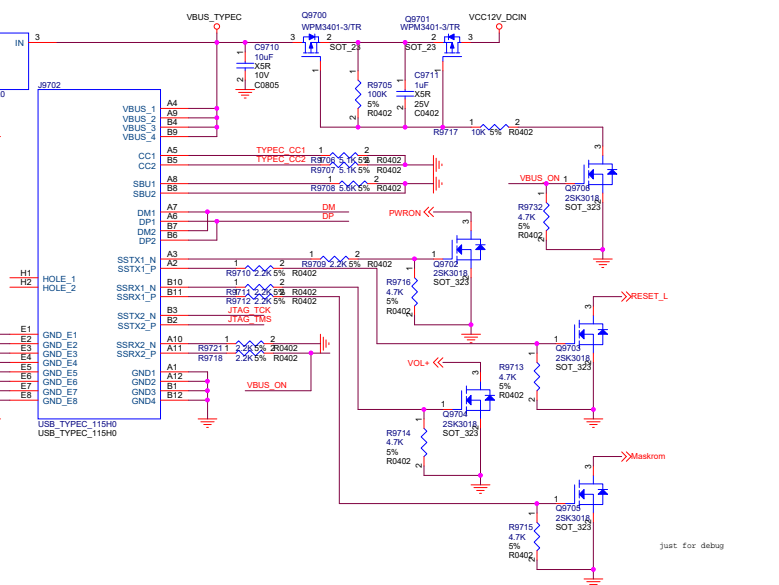
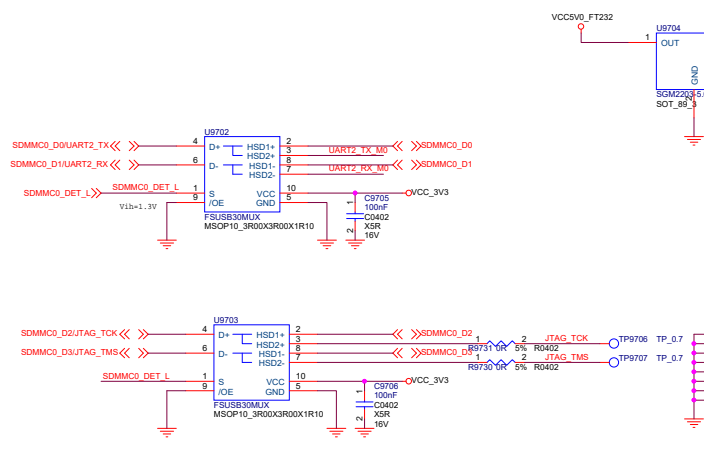


		Fuzhou Rockchip Electronics 瑞芯微电子	
Project:	RK_EVB_1808_ip3_sch_V12		
File:	96.EFUSE		
Date:	Friday, February 15, 2019	Rev:	V1.0
Designed by:	Rzf	Sheet:	96 of 99



Debug UART2
(USB To UART)

JTAG



Truth Table

S	OE	Function
X	H	Disconnect
L	L	D+, D- = HSD1 _n
H	L	D+, D- = HSD2 _n

Rockchip
Fuzhou Rockchip Electronics

Project: RK_EVb_1808_ip3_sch_V12

File: 97.DEBUG

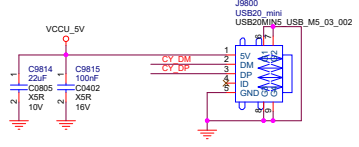
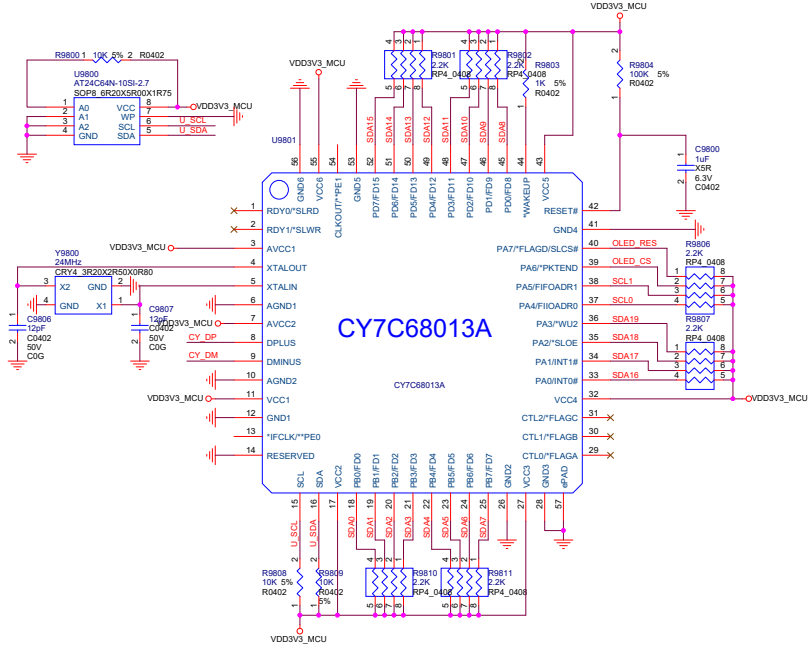
Date: Friday, February 15, 2019

Designed by: Rzf

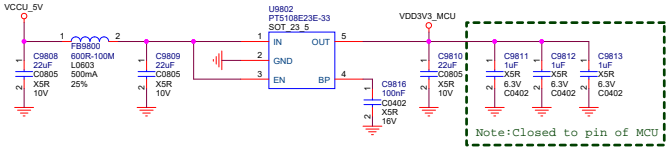
Rev: V1.0

Sheet: 97 of 99

Current Detection MCU

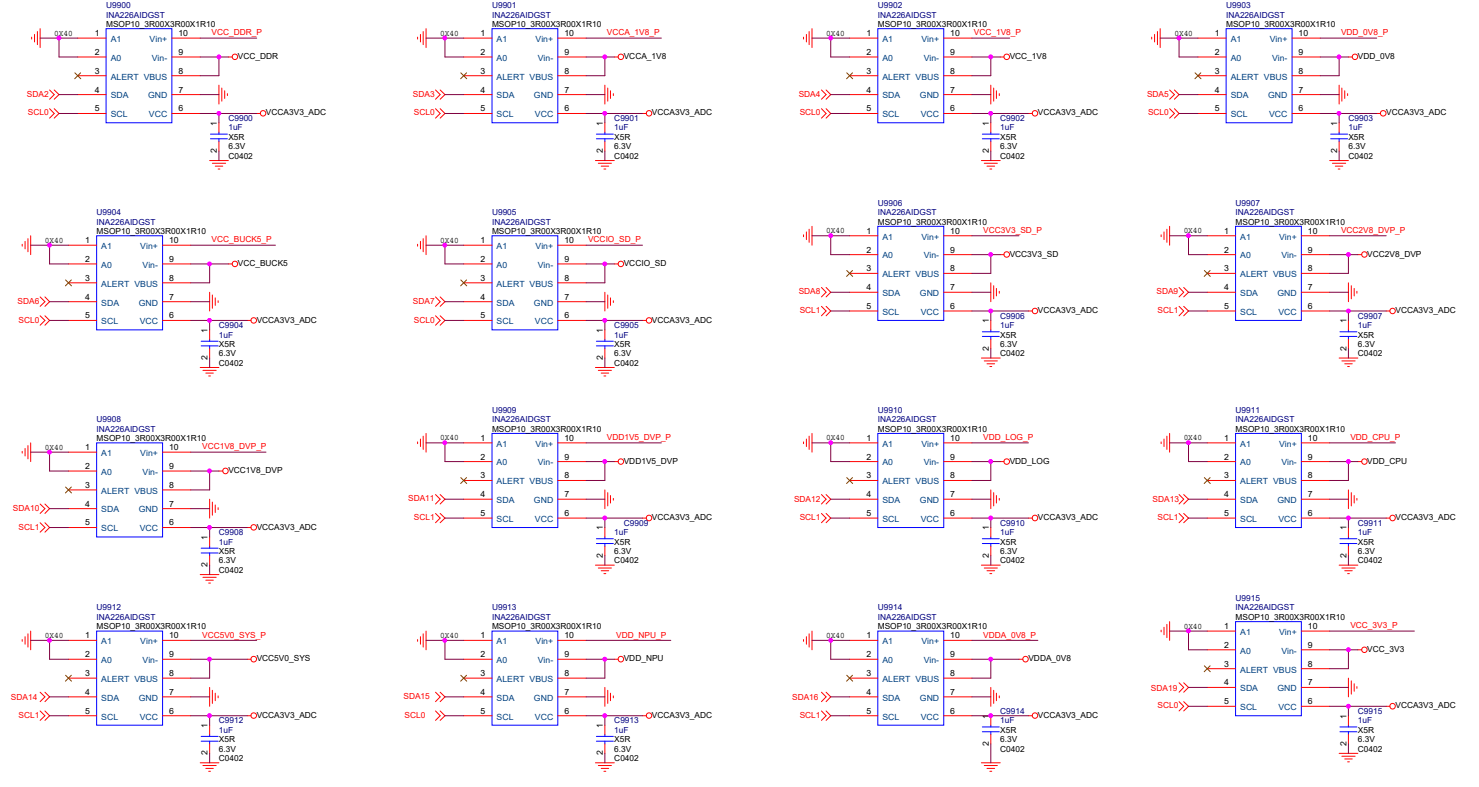


Power

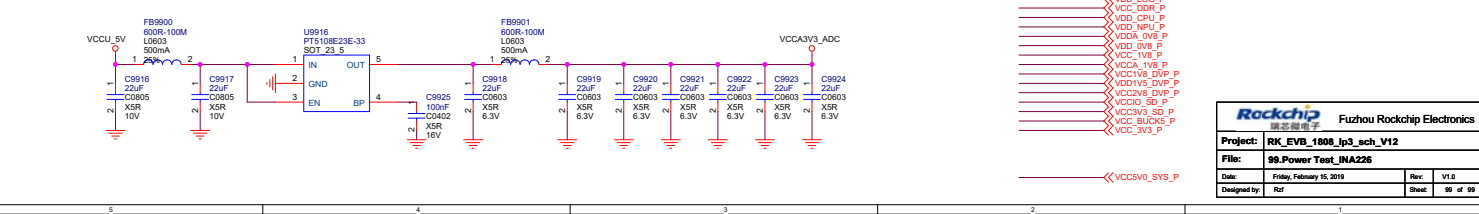


Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project: RK_EVB_1608_lp3_sch_V12			
File: 98_Power Test_MCU			
Date: Friday, February 15, 2019	Rev: V1.0		
Designed by: RZ	Draw: 98 of 99		

ADC Array



ADC Power



Fuzhou Rockchip Electronics
 Project: RK_EVB_1608_tp3_sch_V12
 File: 99_Power Test_INA228
 Date: Friday, February 15, 2019 Rev: V1.0
 Designed by: RZT Sheet: 99 of 99