

EVB Schematic For RK3399Pro

RK3399Pro_Ref_Draft_V1.1

PMIC: RK809-3 (5BUCK + 9LDO + Codec)
RAM: LPDDR3
ROM: eMMC + TF card
Interface: MIPI CSI/MIPI DSI/UART/I2S/RMII/LCDC/PCIE/USB2/TYPEC/HDMI

Index

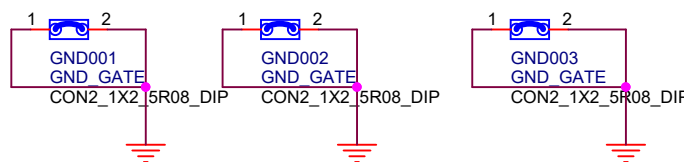
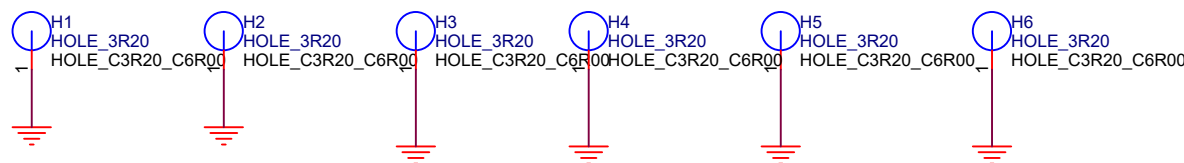
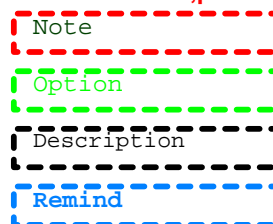
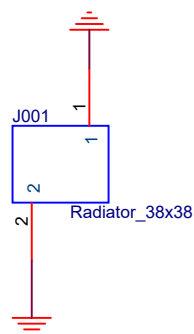
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Note

NOTE 1: Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

NOTE 2: Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.



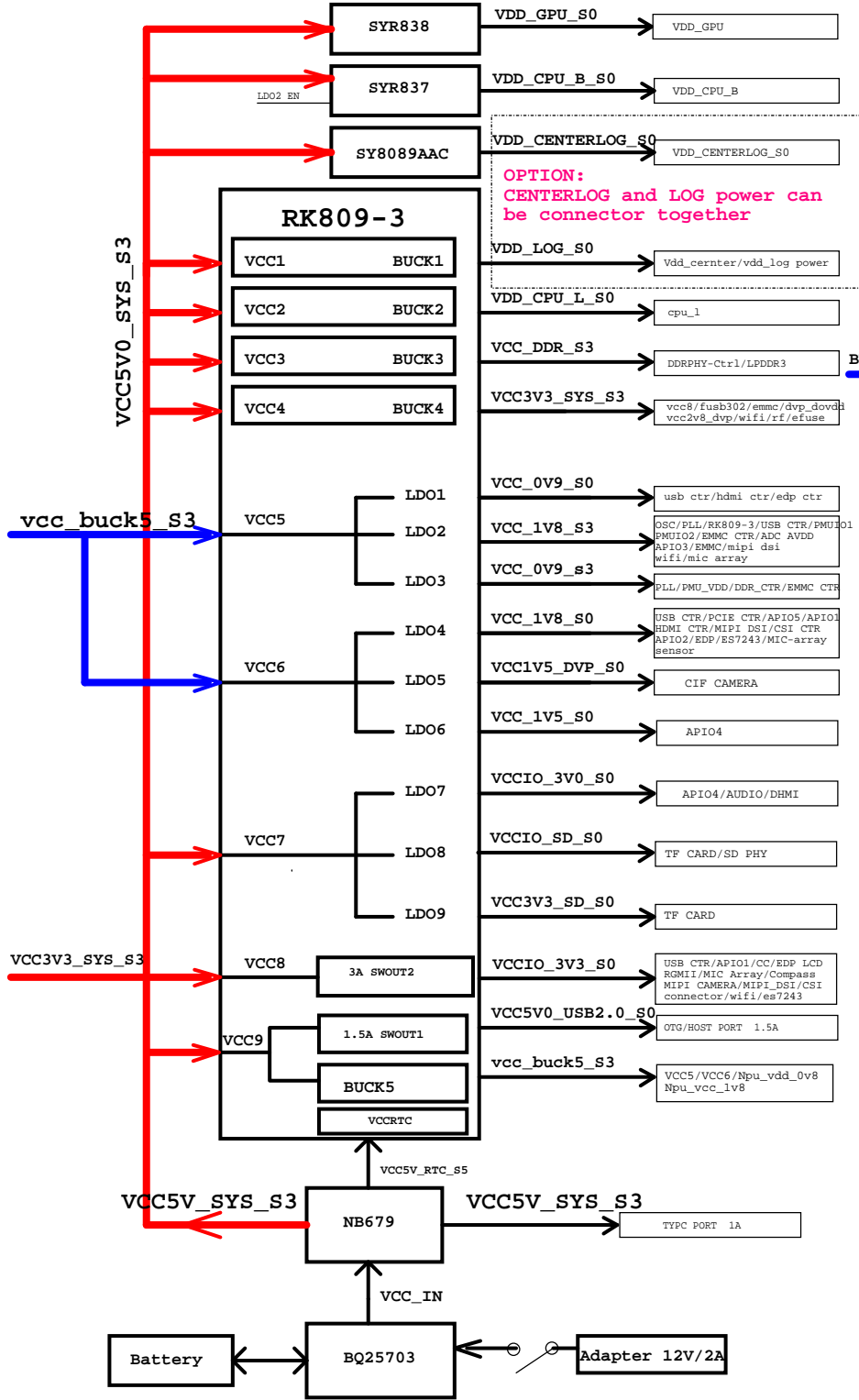
		Fuzhou Rockchip Electronics	
瑞芯微电子			
Project:	RK3399Pro LP3S178P232DD8		
File:	01.Index		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	1 of 99

Version	Date	Author	Change List	Approved
V1.0	20180904		First edition for RK3399Pro	RZF
V1.1	20181112		Second edition for RK3399Pro	RZF

I2C MAP

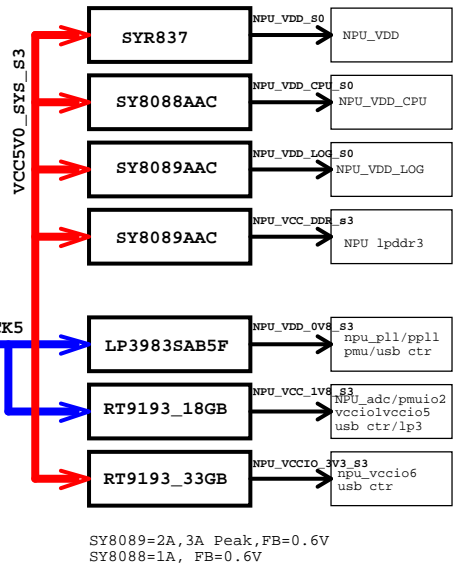
Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	I2C0_SCL/GPIO1_C0_u I2C0_SDA/GPIO1_B7_u	PMUIO2	I2C0_SCL_PMIC I2C0_SDA_PMIC	VCC_1V8	1.RK809 2.BQ25703 3.TCS4525 4.TCS4536			100kHz, 400kHz
I2C1	I2C1_SCL/GPIO4_A2_u I2C1_SDA/GPIO4_A1_u	APIO5	I2C1_SCL_1V8 I2C1_SDA_1V8	VCCA_1V8	1.MIPI_RX_CAMERA 2.CIF_CAMERA 3.G-SENSOR 4.COMPASS 5.PCIEX4 6.ES7243 7. mic-array			100kHz, 400kHz
I2C2	I2C2_SCL/GPIO2_A1_u I2C2_SDA/GPIO2_A0_u	APIO2	NC		GSL1680			
I2C3	I2C3_SCL/GPIO4_C1_u I2C3_SDA/GPIO4_C0_u	APIO4	I2C4_SCL_HDMI I2C4_SDA_HDMI	VCCIO_3V0	HDMI			100kHz, 400kHz
I2C4	I2C4_SCL/GPIO1_B4_u I2C4_SDA/GPIO1_B3_u	PMUIO2	I2C4_SCL_TP I2C4_SDA_TP	VCC_1V8	TOUCH		Touch IC	100kHz, 400kHz
I2C5	I2C5_SCL/GPIO3_B3_u I2C5_SDA/GPIO3_B2_u	APIO1	NC					
I2C6	I2C6_SCL/GPIO2_B2_u I2C6_SDA/GPIO2_B1_u	APIO2	NC					
I2C7	I2C7_SCL/GPIO2_B0_u I2C7_SDA/GPIO2_A7_u	APIO2	NC					
I2C8	I2C8_SCL/GPIO1_C5_u I2C8_SDA/GPIO1_C4_u	PMUIO2	I2C8_SCL_CC I2C8_SDA_CC	VCC_1V8	FUSB302B			100kHz, 400kHz
I2C9	I2C1_SCL/NPU_GPIO0_C0_u I2C1_SDA/NPU_GPIO0_C1_u	NPU_VCC_1V8	NPU_I2C1_SCL NPU_I2C1_SDA	NPU_VCC_1V8				100kHz, 400kHz

 Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8		
File:	04.I2C MAP		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	4 of 99



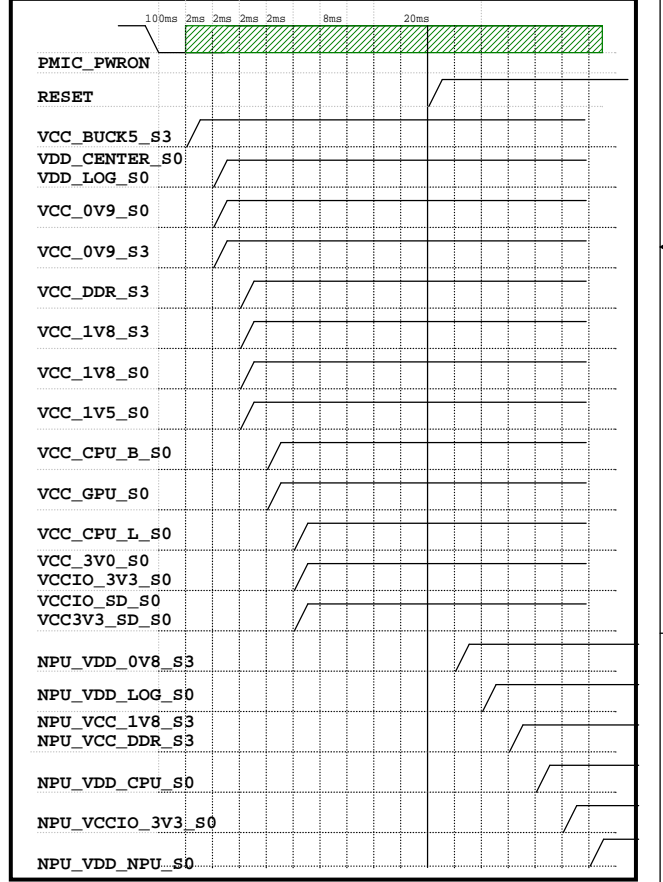
OPTION:
CENTERLOG and LOG power can
be connector together

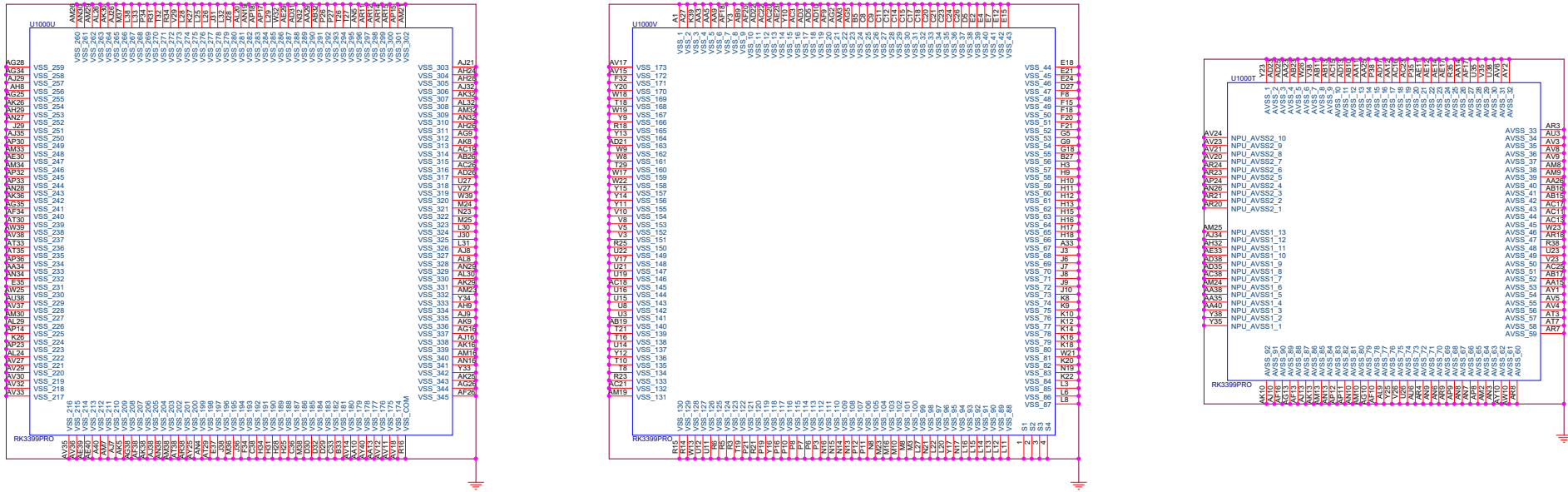
POWER DIAGRAM



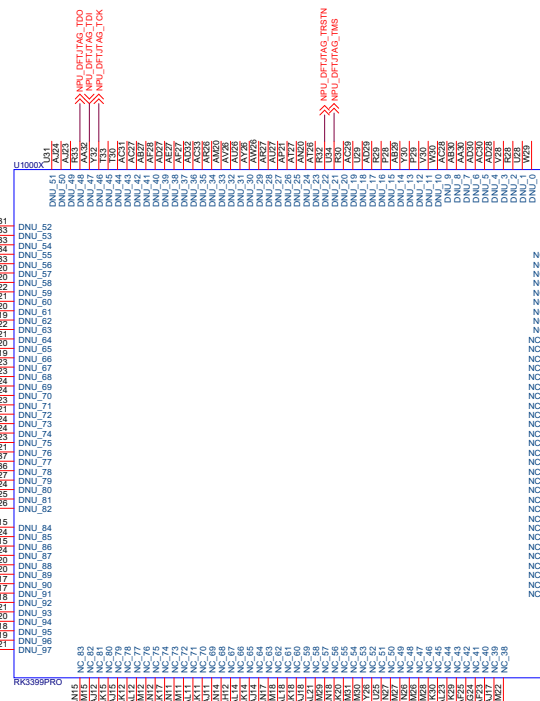
SY8089=2A, 3A Peak, FB=0.6V
SY8088=1A, FB=0.6V

RK809-3 Power-on Sequence							
PowerName	PMIC Channel	Time slot (step 2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current
VCC5V0_SYS_S3	ext(NB679/7A)	0	5V		ON	ON	
VCC_BUCK5_S3	BUCK5(2.5A)	1	3.3V		ON	ON	
VDD_LOG_S0	BUCK1(2.5A)	2	0.9V		ON	OFF	VDD_CENTER
VCC_OV9_S0	LDO1(400mA)	2	0.9V		ON	OFF	
VCC_DDR_S3	BUCK3(1.5A)	3	1.25V		ON	ON	
VCC_IV8_s3	LDO2(400mA)	3	1.8V		ON	ON	
VCC_IV8_S0	LDO4(400mA)	3	1.8V		ON	OFF	
VCC_IV5_S0	LDO6(400mA)	3	1.5V		ON	OFF	
VCC_GPU_S0	ext(SYR837/6A)	3B	0.9V		ON	OFF	4.5A
VDD_CPU_B_S0	ext(SYR837/6A)	3A	0.9V		ON	OFF	4.5A
VCC_CPU_L_S0	BUCK2(2.5A)	4	0.9V		ON	OFF	
VCCIO_3V0_S0	LDO7(400mA)	5	3.0V		ON	OFF	
VCCIO_3V3_S0	SMOUT2(3A)	5	3.3V		ON	OFF	
VCC3V3_SYS_S3	BUCK4(1.5A)	5	3.3V		ON	OFF	
VCCIO_SD_S0	LDO8(400mA)	5	3.3V		ON	OFF	
VCC3V3_SD_S0	LDO9(400mA)	5	3.3V		ON	OFF	
VCCIV5_DVP_S0	LDO5(400mA)		1.5V		OFF	OFF	
VCCIV8_DVP_S0	ext(rt9193)		1.8V		OFF	OFF	
VCC2V8_DVP_S0	ext(rt9193)		2.8V		OFF	OFF	
VCC5V0_USB2.0_S0	SMOUT1(1.5A)		5V		OFF	OFF	
RK809 sent out reset signal							for rk3399(timing:10 ; Then RK3399 sent out NPU's pwr on signal
NPU_VDD_OV8_S3	ext(lp3983)	11	0.8V		ON	ON	
NPU_VDD_LOG_S0	ext(sy8089aac)	12	0.85V		ON	ON	1.25A
NPU_VCC_IV8_S3	ext(rt9193)	13	1.8V		ON	ON	
NPU_VCC_DDR_S3	ext(sy8089aac)	13	1.25V		ON	ON	
NPU_VDD_CPU_S0	ext(sy8089aac)	14	0.85V		ON	OFF	750mA
NPU_VCCIO_3V3_S3	ext(rt9193)	15	3.3V		ON	ON	
NPU_VDD_NPU_S0	ext(SYR837)	16	0.85V		ON	OFF	4A
NPU_REF_CLK							RK3399 sent out 24M clk for npu.
NPU_RESET							RK3399 send out Reset signal for npu.

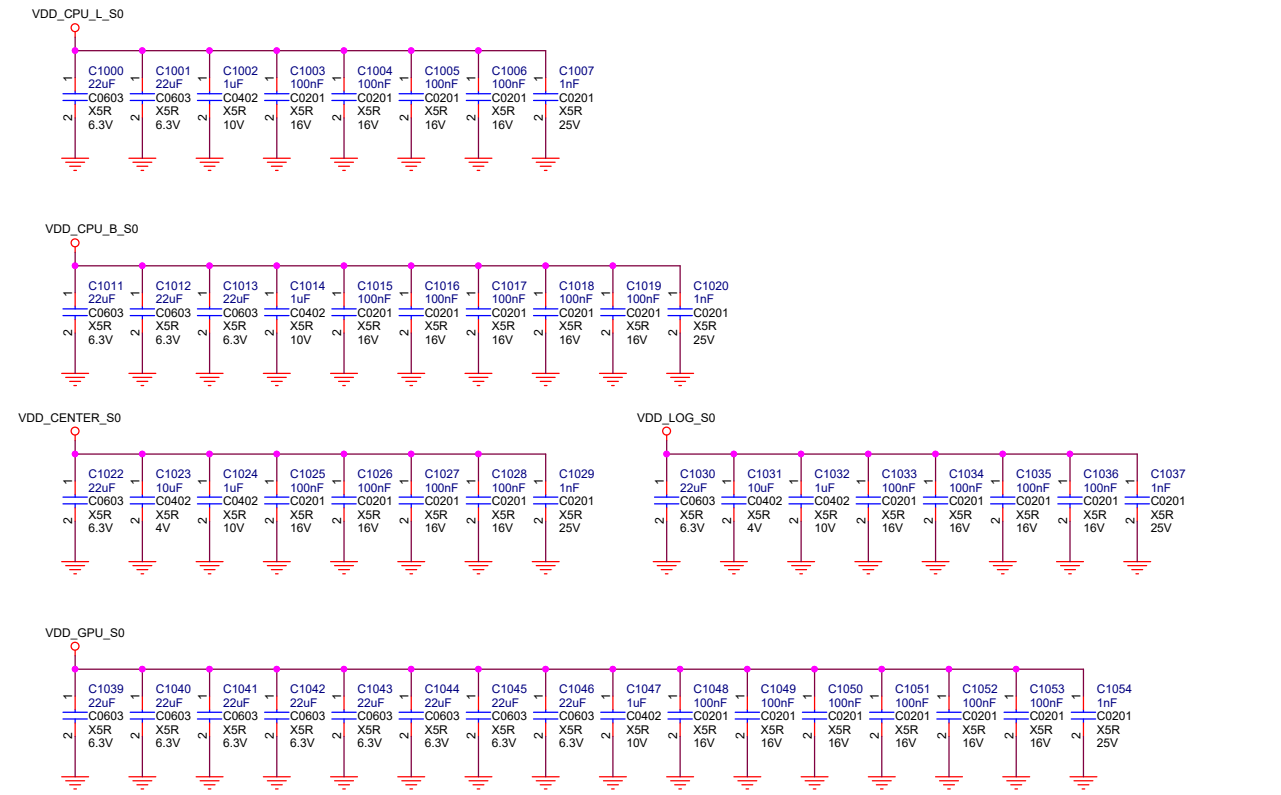
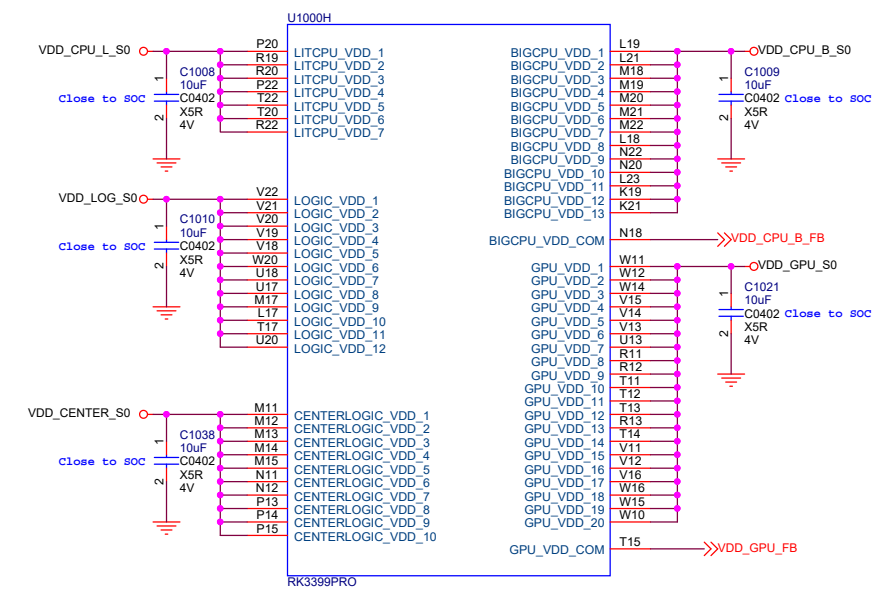




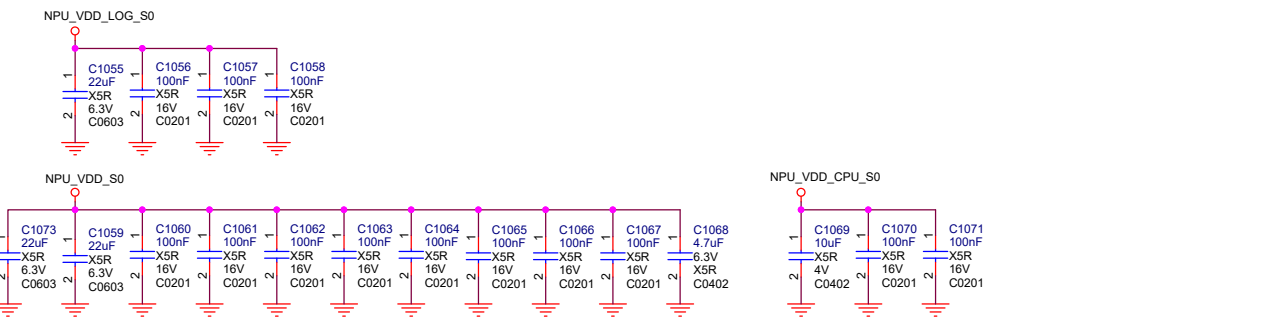
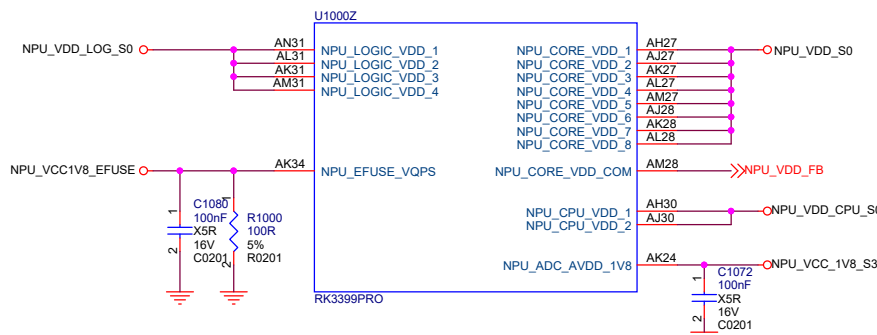
NC & DNU



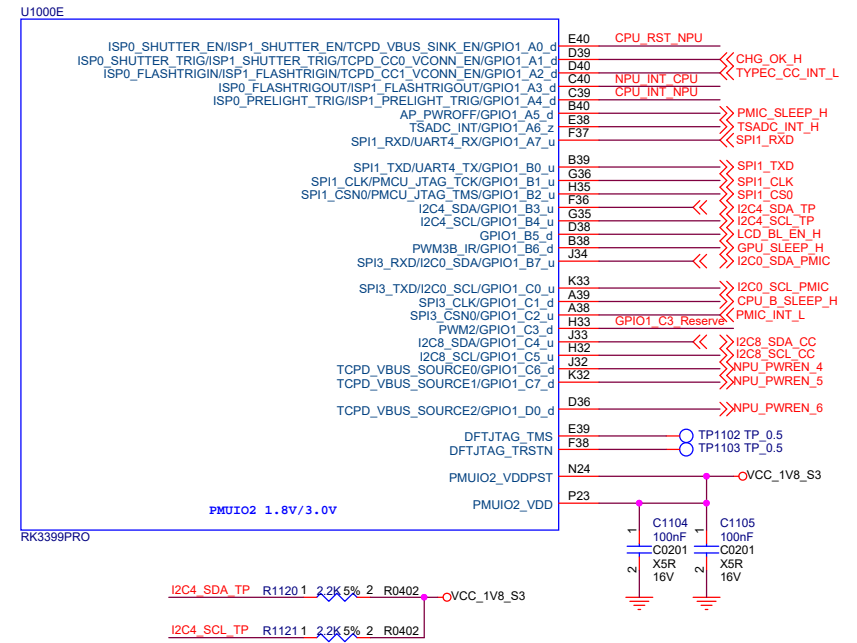
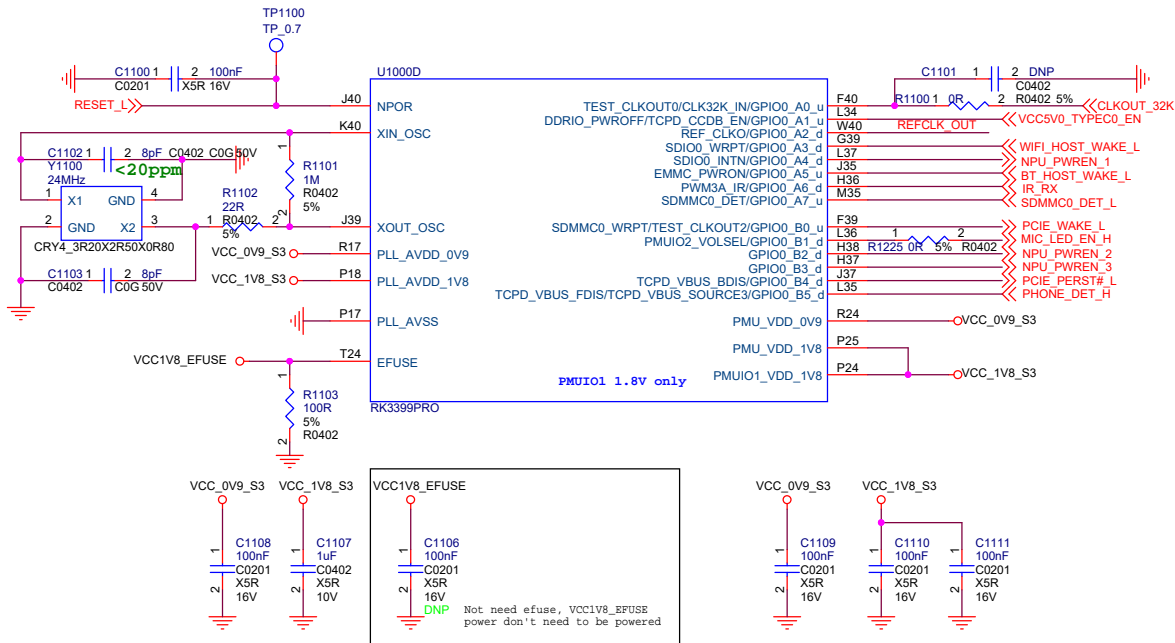
Power



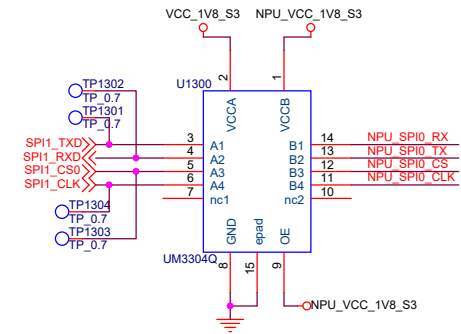
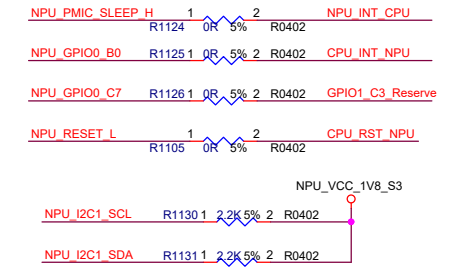
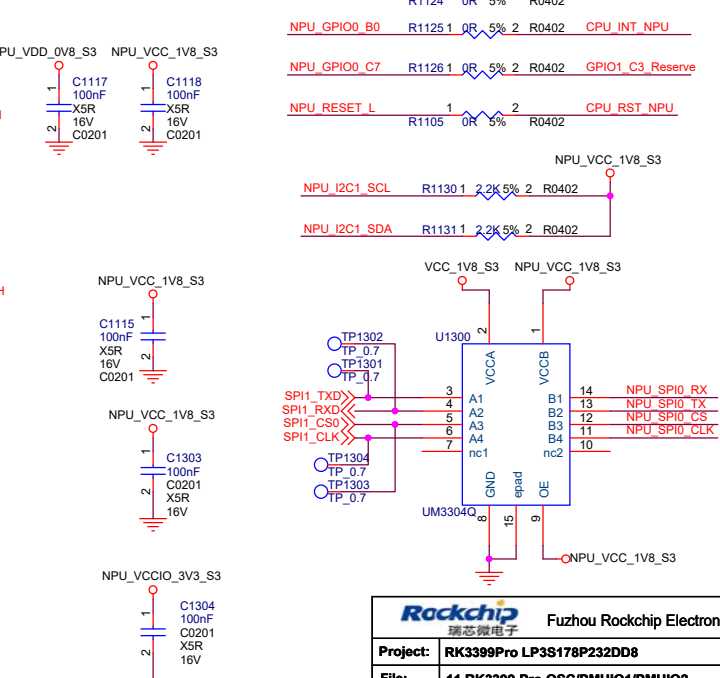
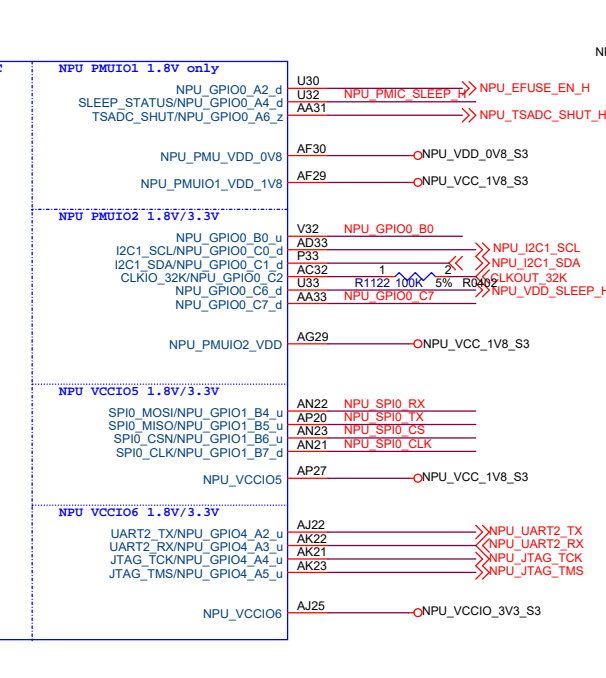
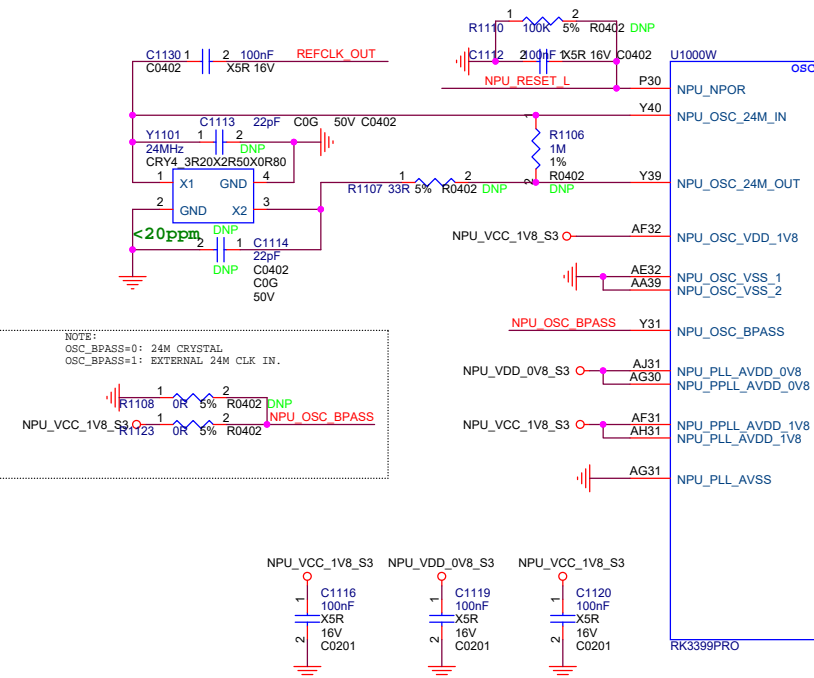
NPU Power



PMUIO1/PMUIO2



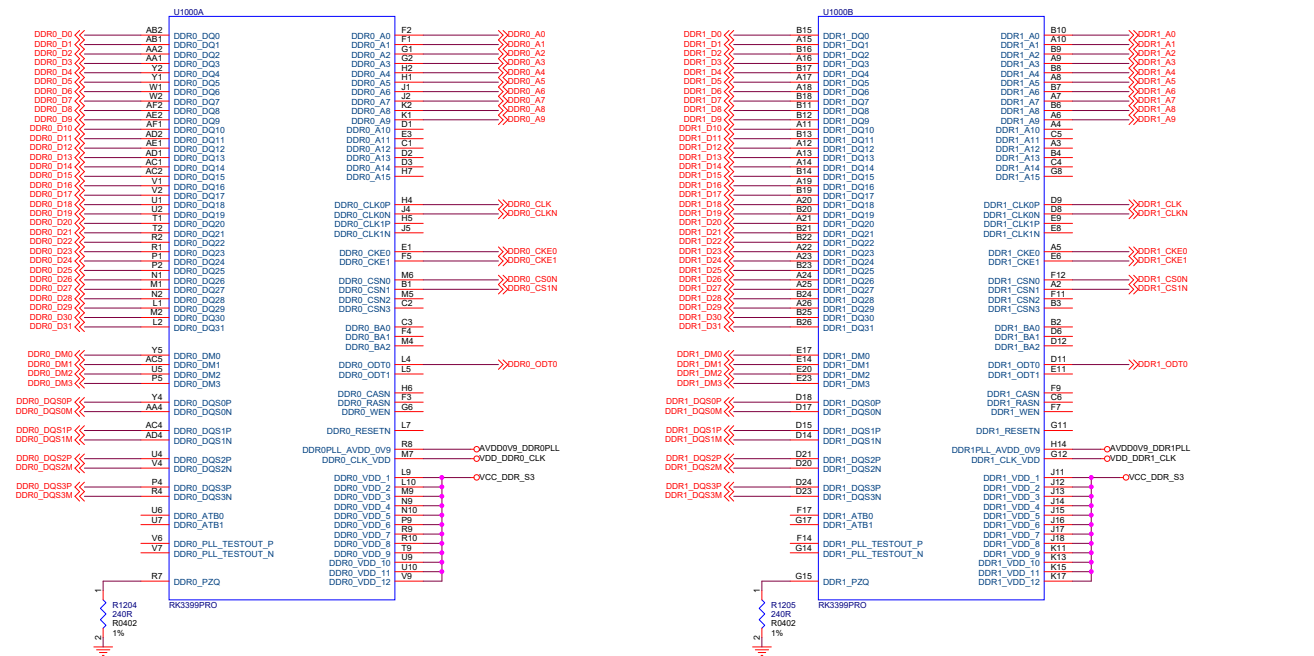
NPU PMUIO1/PMUIO2/GPIO



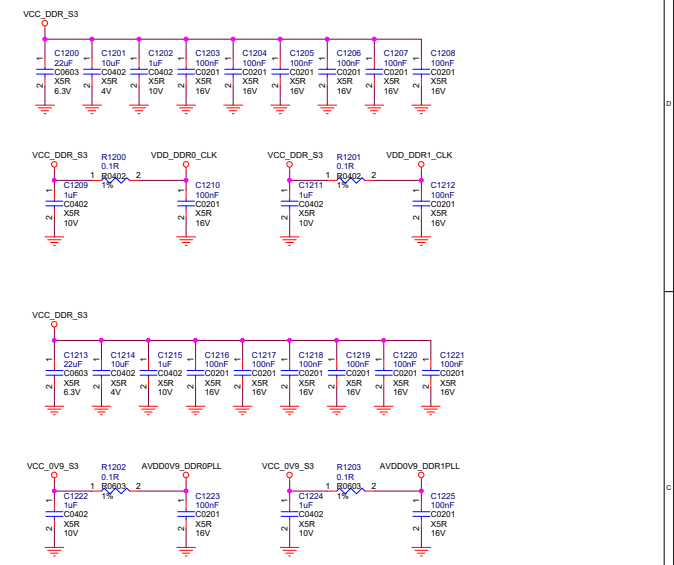
Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics

Project:	RK3399Pro LP3S178P232DD8
File:	11.RK3399 Pro OSC/PMUIO1/PMUIO2
Date:	Thursday, November 15, 2018
Designed by:	Rzf
Rev:	V1.0
Sheet:	11 of 90

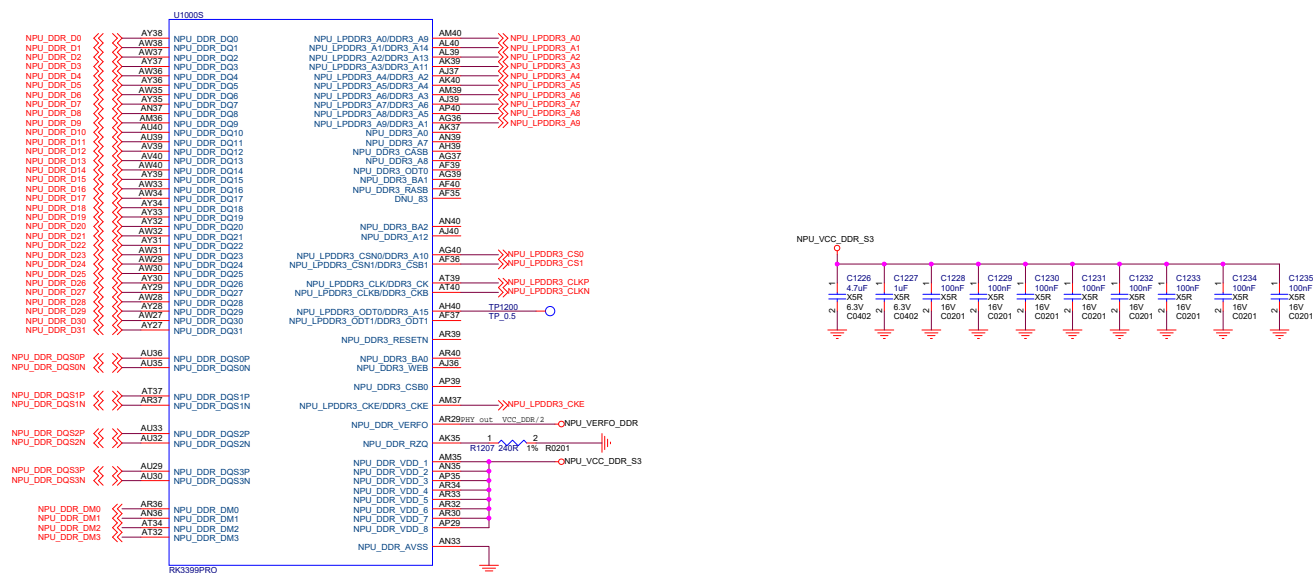
DDR Controller



DDR FILTER

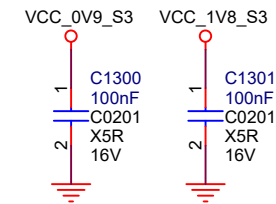
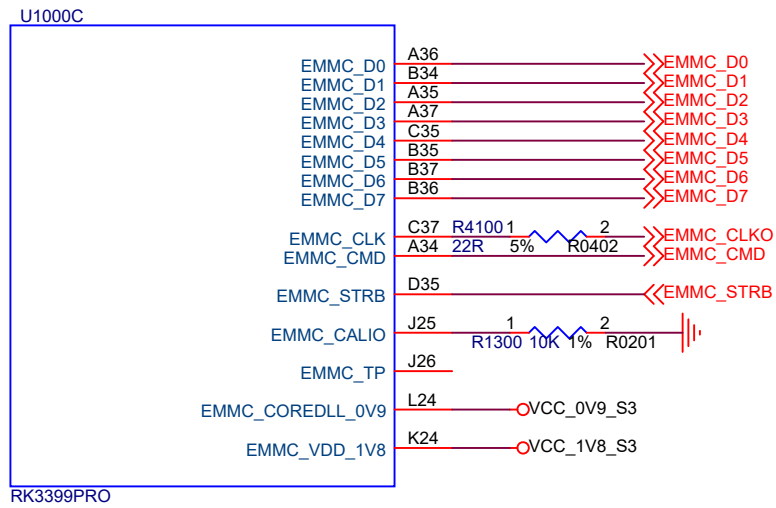


NPU DDR Controller

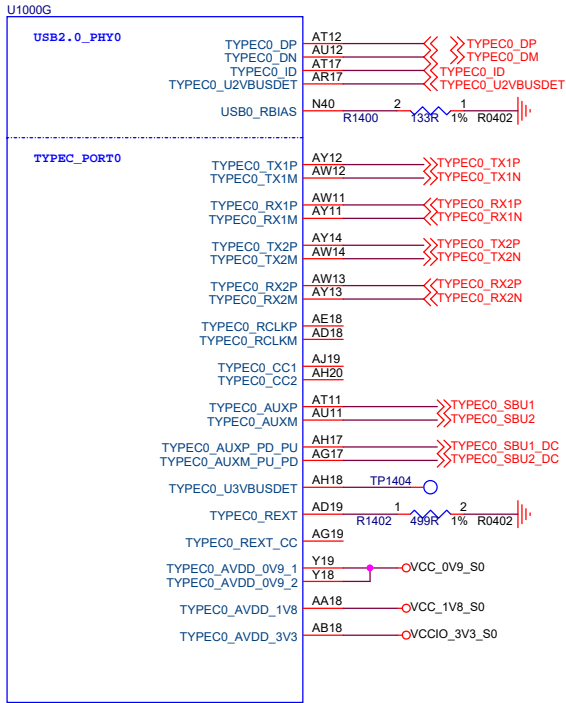


LPDDR3/LPDDR2	DDR3
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
	A0
	A7
	CASB
	A8
	ODT0
	BA1
	RASB
	CSB0
	BA2
	A12
	BA0
	WEB
CK	CK
CKB	CKB
CKE	CKE
CSB0	A10
CSB1	CSB1
ODT0	A15
ODT1	ODT1
RESETN	RESETN

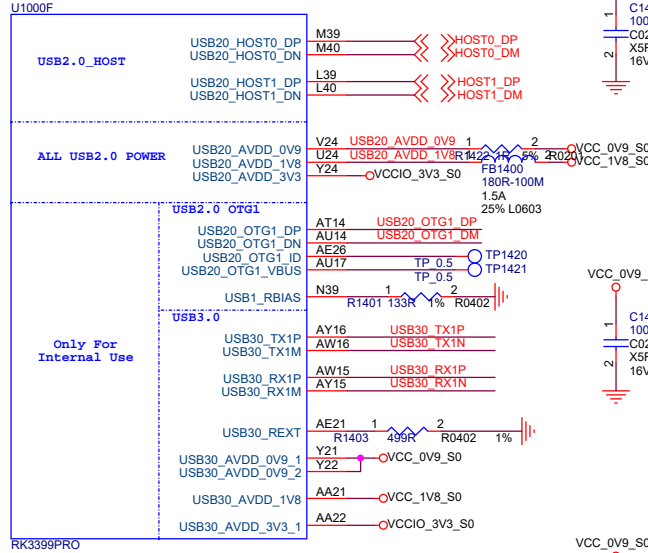
EMMC



USB/TYPEC

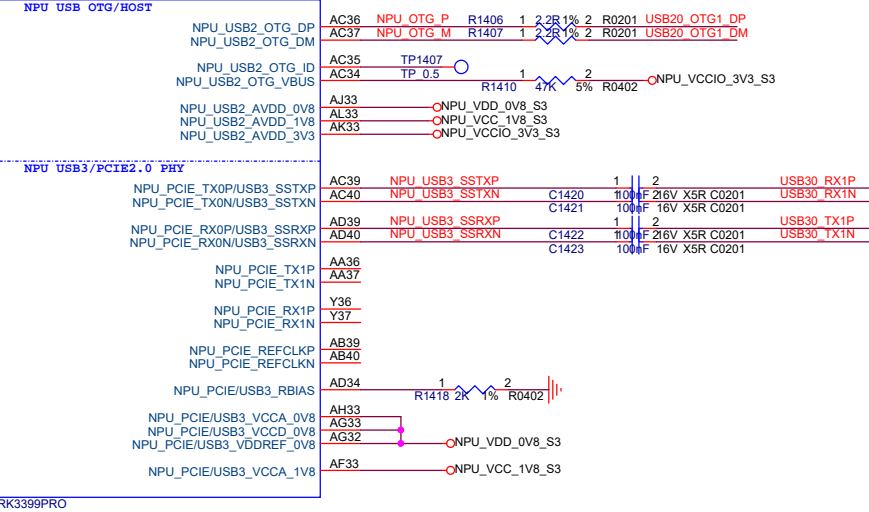


RK3399PRO



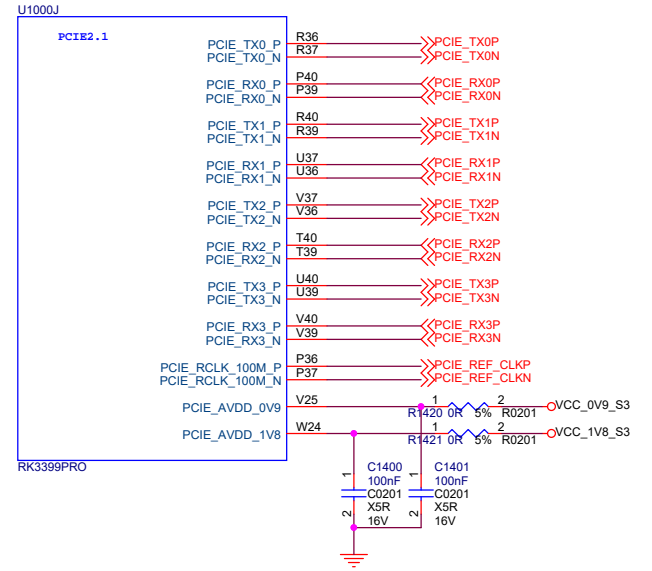
NOTE:
Pin Y24 and Pin AA22 connected to
together internal.

U1000Y

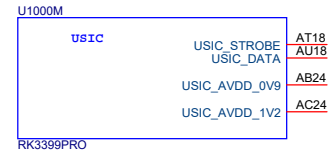


RK3399PRO

PCIe

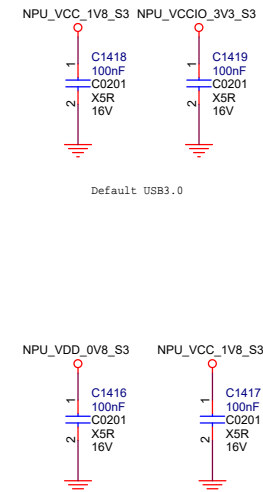


USIC



RK3399PRO

NPU PCIe/USB3.0



Default USB3.0

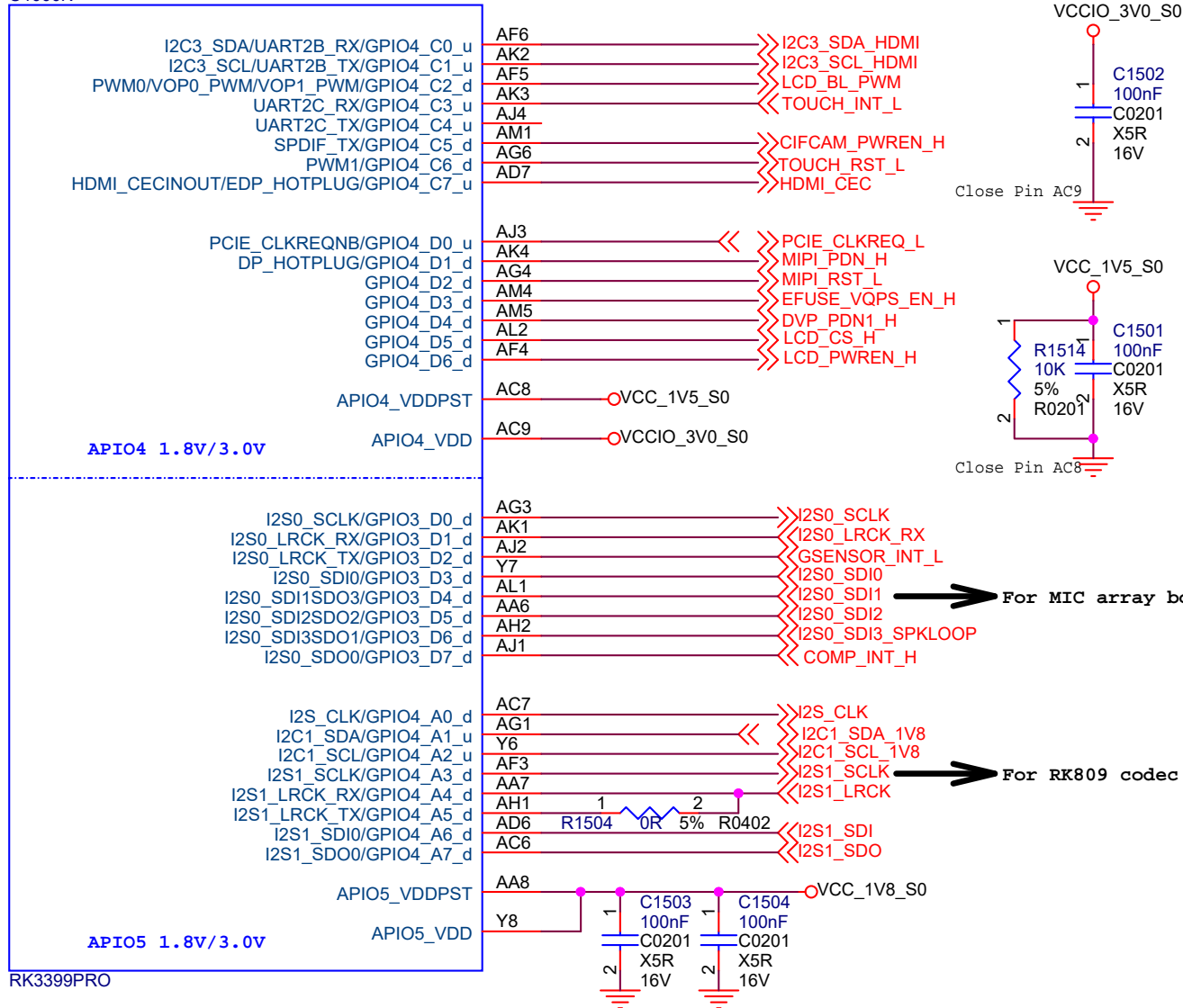
Rockchip
福州微电子

Fuzhou Rockchip Electronics

Project:	RK3399Pro LP3S178P232DD8		
File:	14.RK3399 Pro USB2.0/TYPEC/PCIe		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	14 of 90

GPIO

U1000N



APIO4 1.8V/3.0V

APIO5 1.8V/3.0V

RK3399PRO

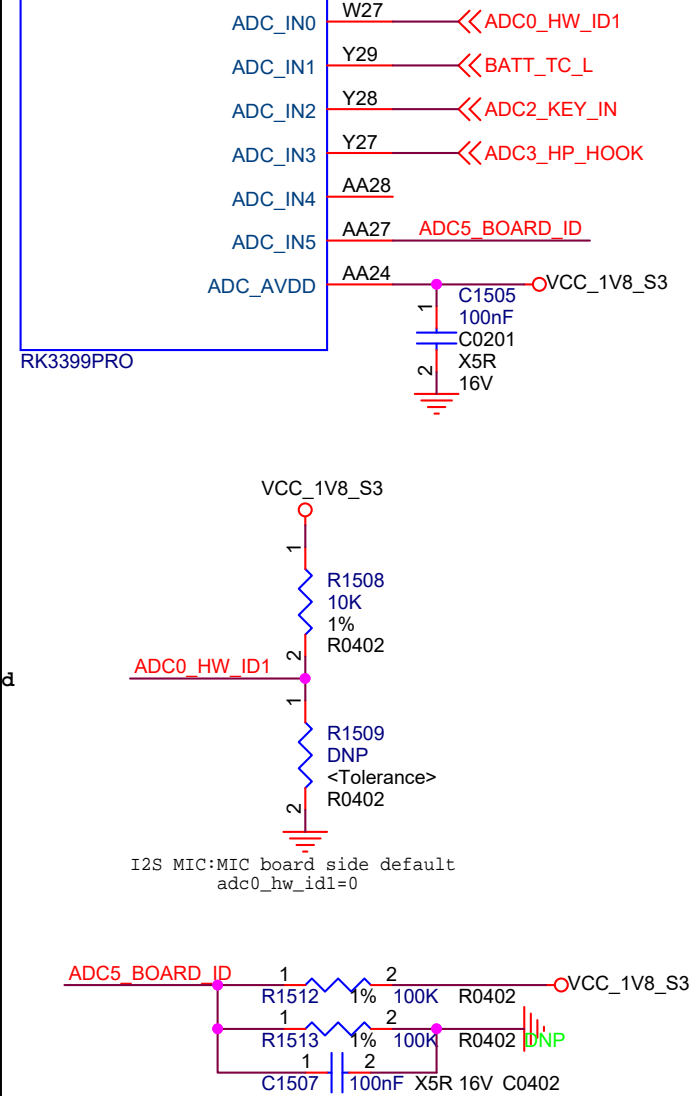
For MIC array board

For RK809 codec

U1000Q

SARADC

SARADC 1.8V only



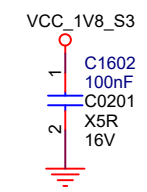
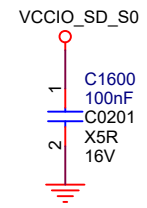
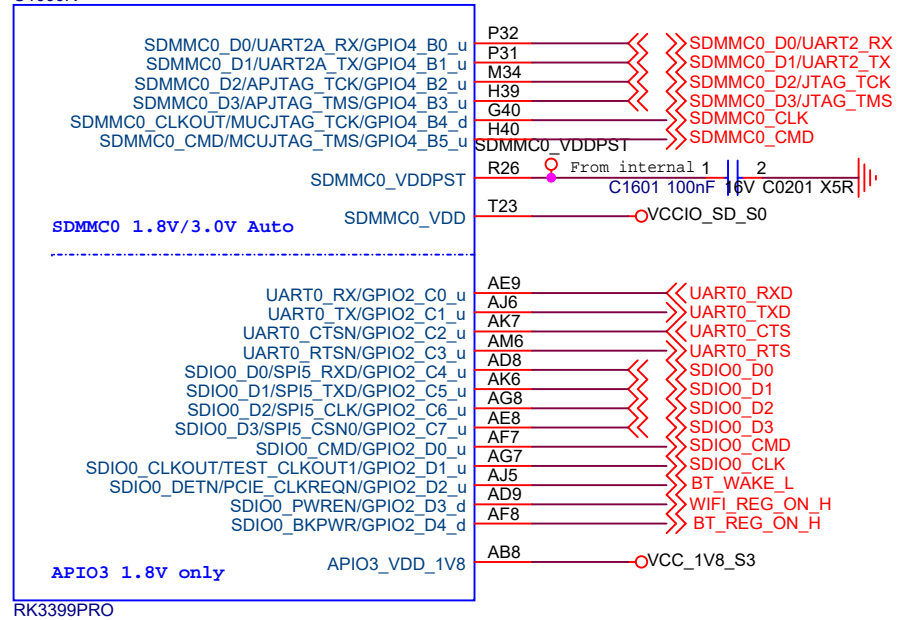
I2S MIC:MIC board side default
adc0_hw_id1=0

Vboard_id=1.8V, Version:V10;
Vboard_id=0.9V, Version:V20;
Vboard_id=0V, Version:V30;

Rackchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8		
File:	15.RK3399 Pro SARADC/GPIO		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	15 of 99

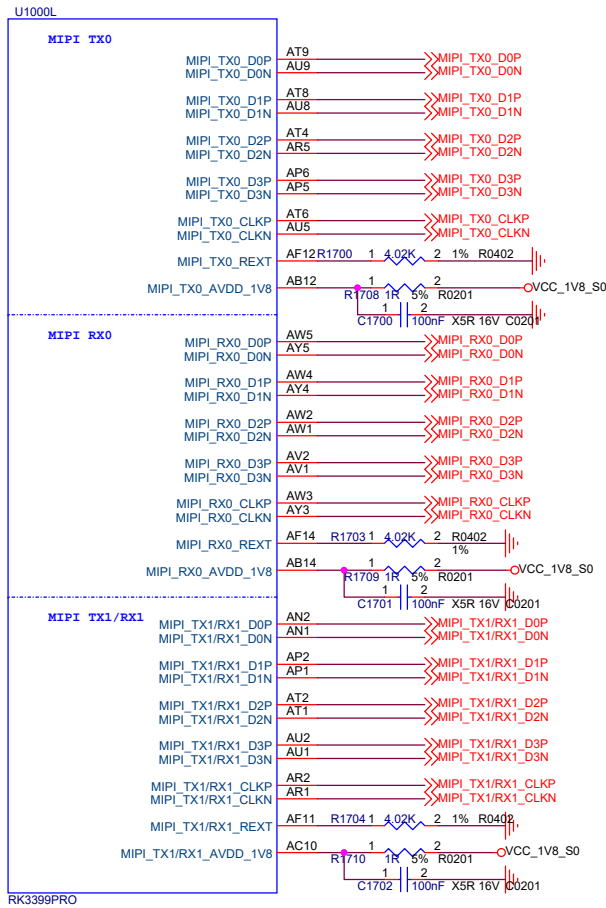
SDMMC0/SDIO0 Controller

U1000R



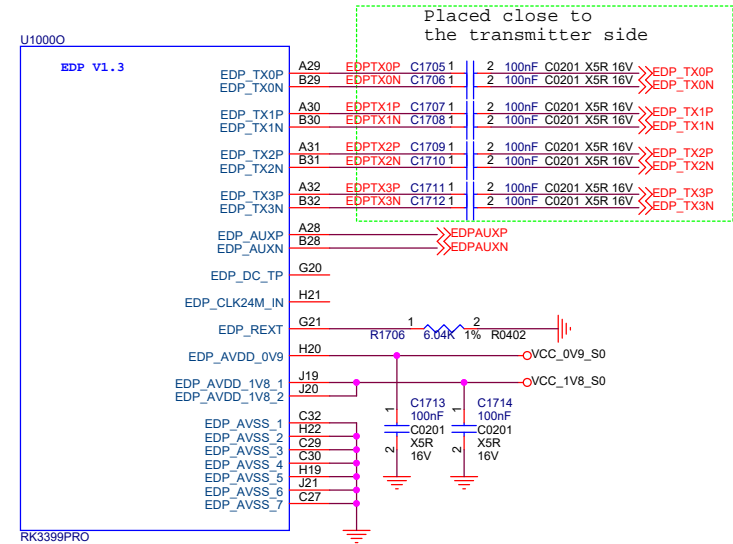
 Fuzhou Rockchip Electronics 瑞芯微电子	
Project:	RK3399Pro LP3S178P232DD8
File:	16.RK3399 Pro SDMMC0/SDMMC1
Date:	Thursday, November 15, 2018
Designed by:	Rzf
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MIPI CSI/DSI



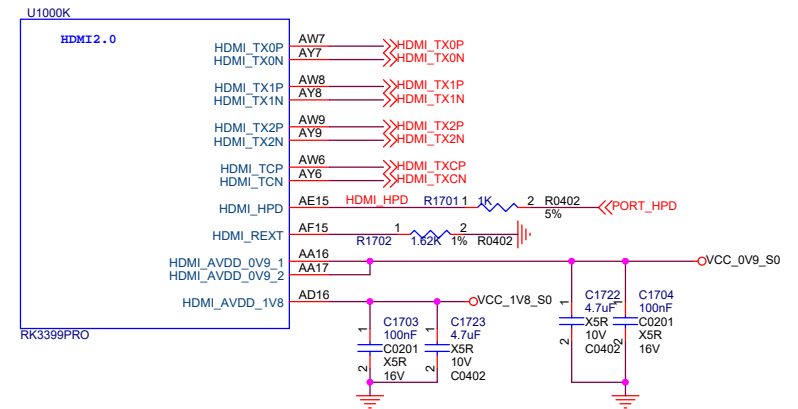
RK3399PRO

EDP



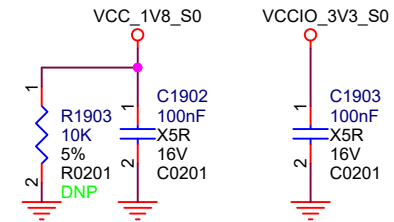
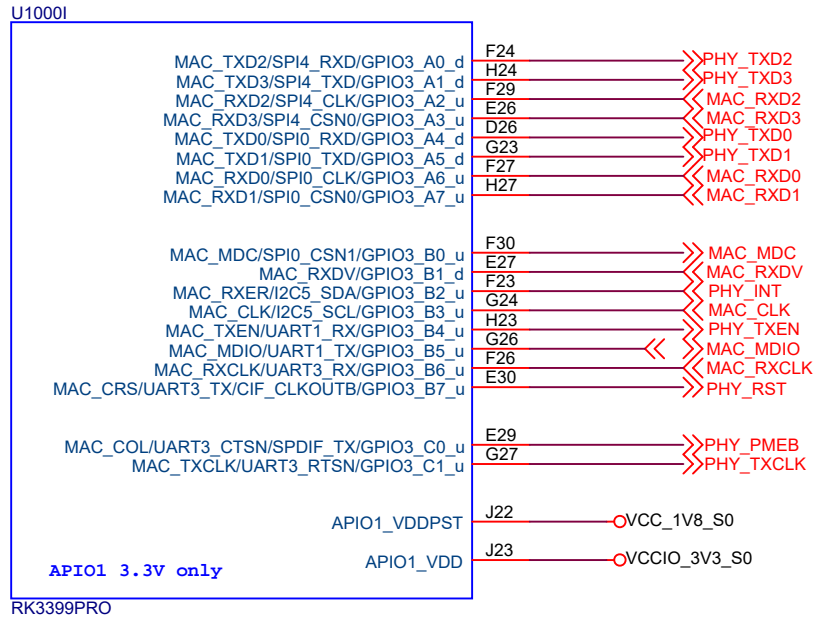
RK3399PRO

HDMI

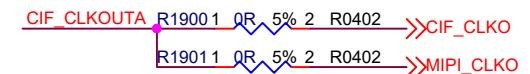
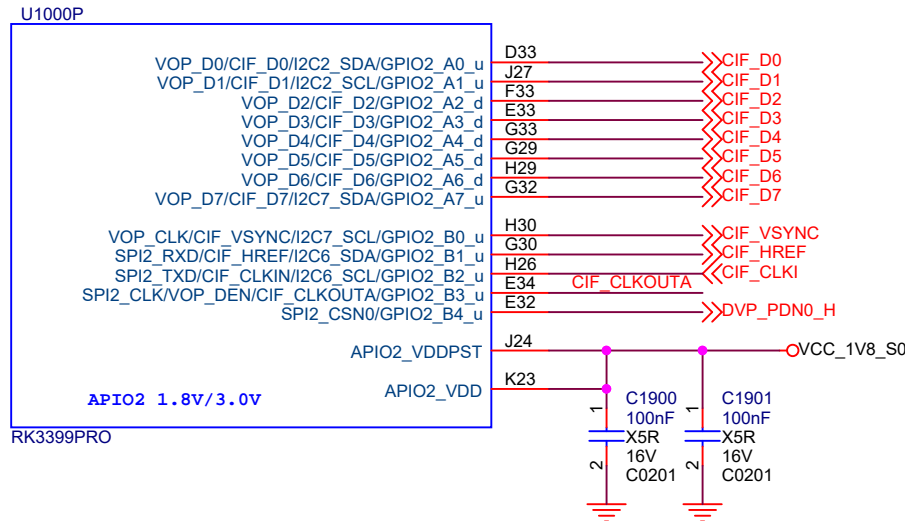


RK3399PRO

MAC

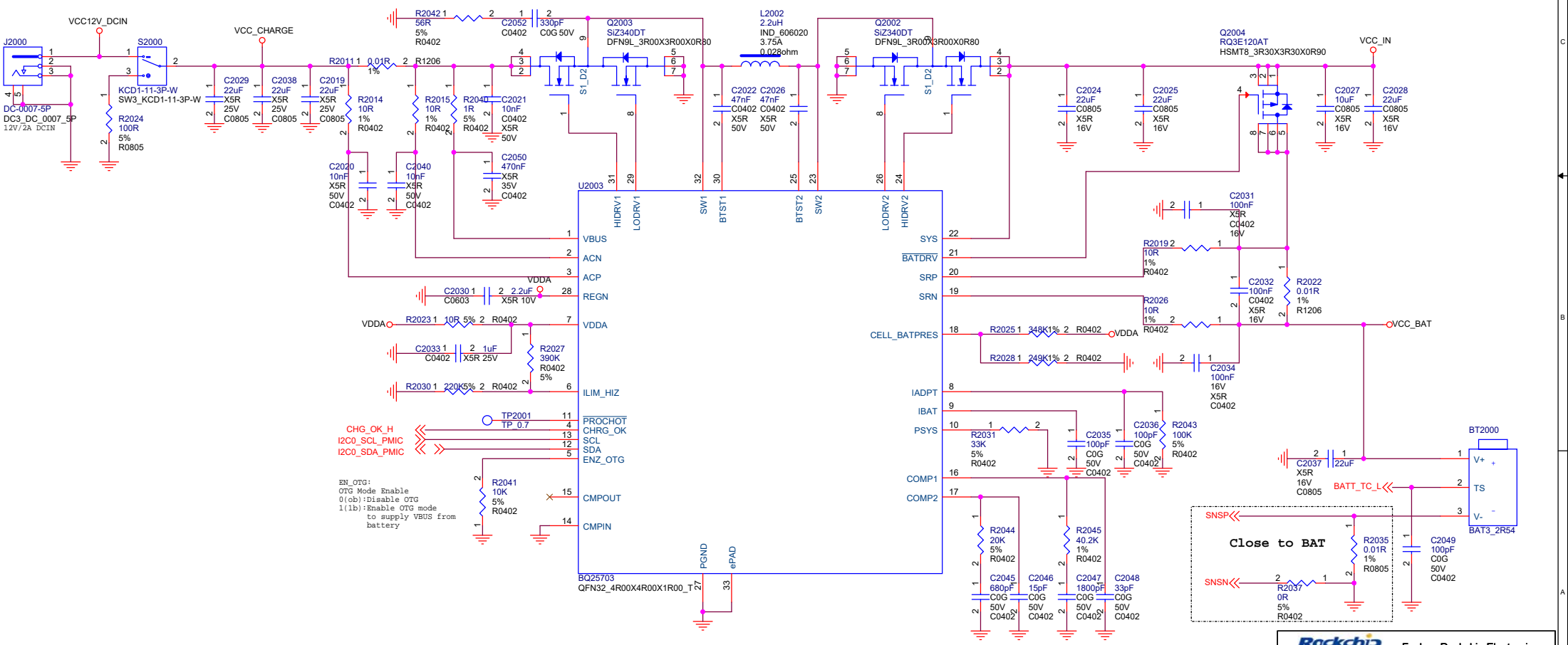
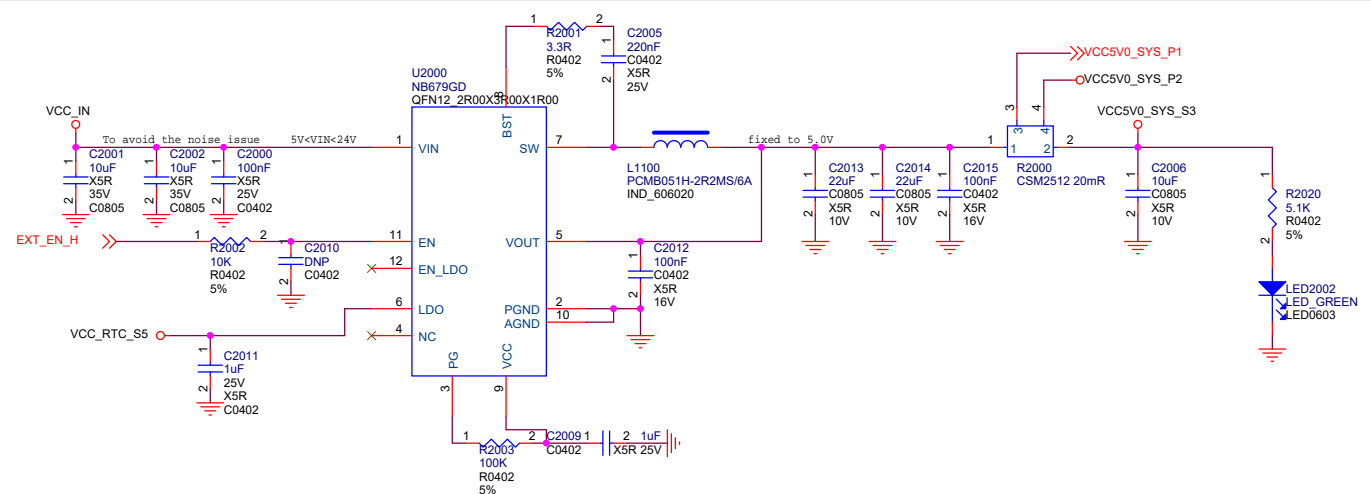


VOP/CIF



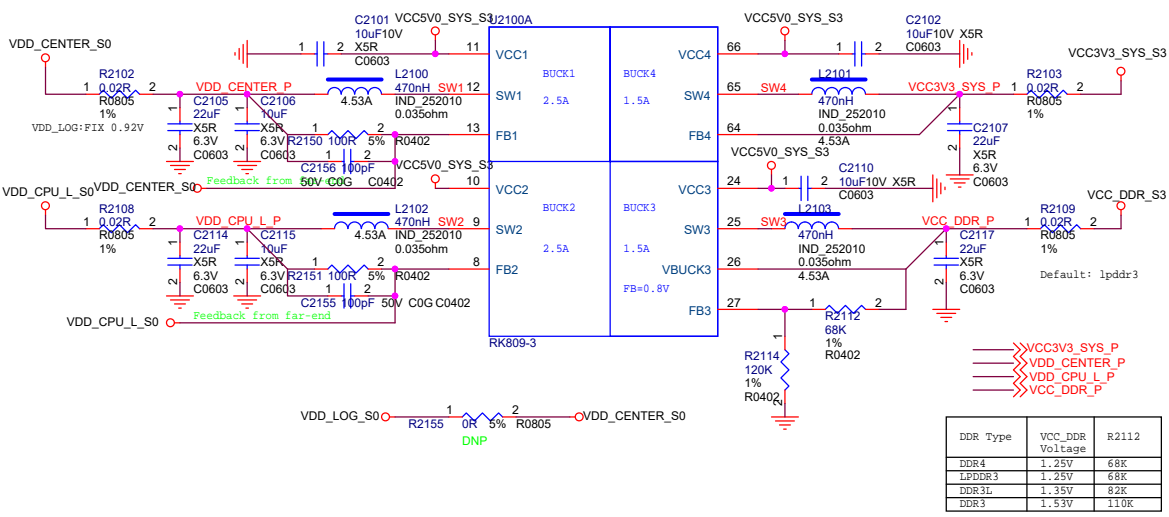
		Fuzhou Rockchip Electronics	
Project:		RK3399Pro LP3S178P232DD8	
File:		19.RK3399 Pro RGMII/VOP/CIF	
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	19 of 99

SYSTEM Power

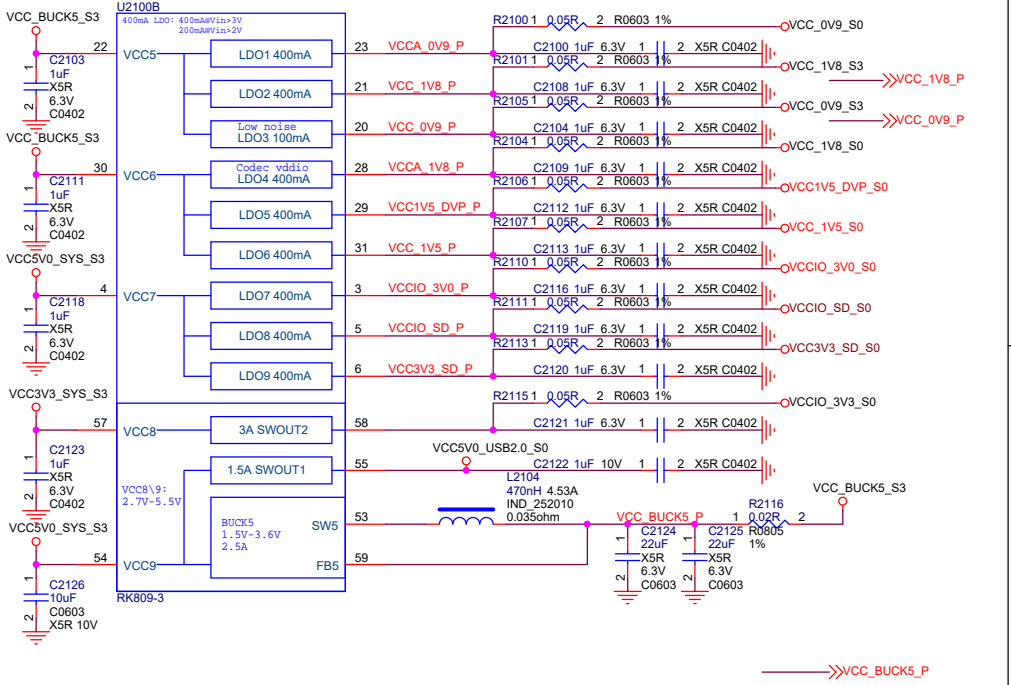


DC IN

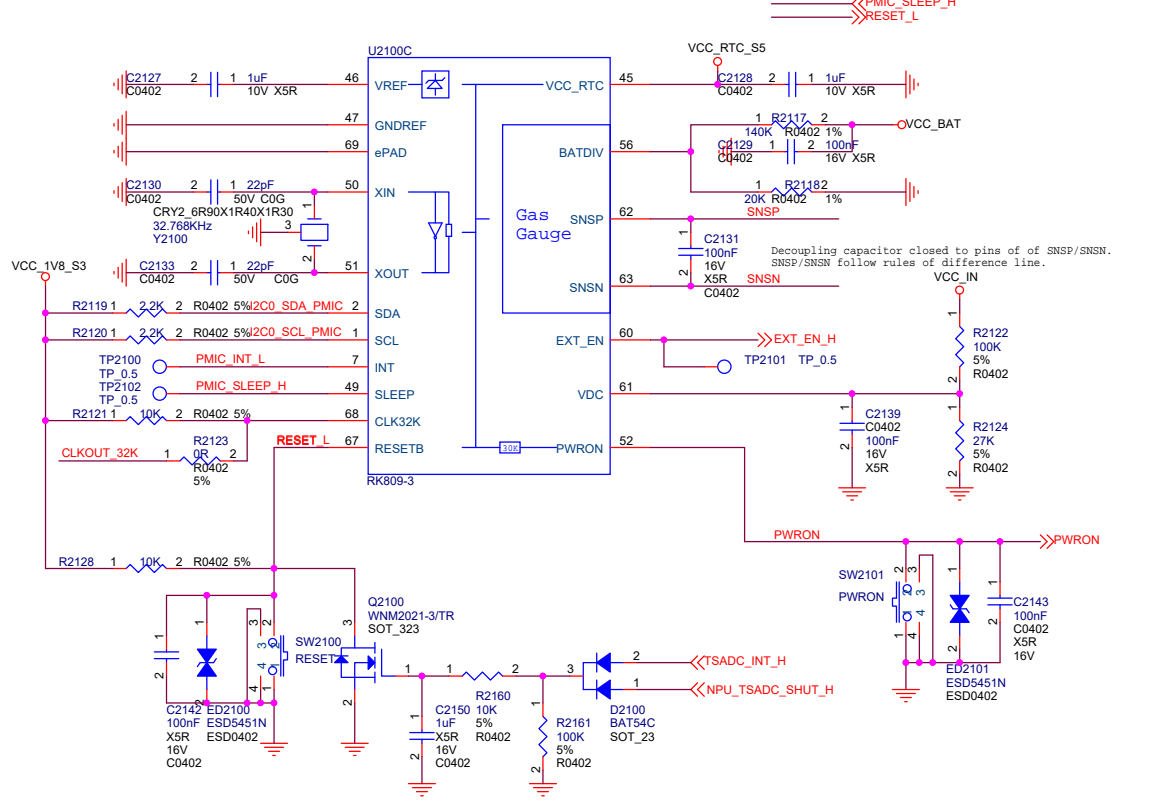
PMIC RK809-3 DCDC



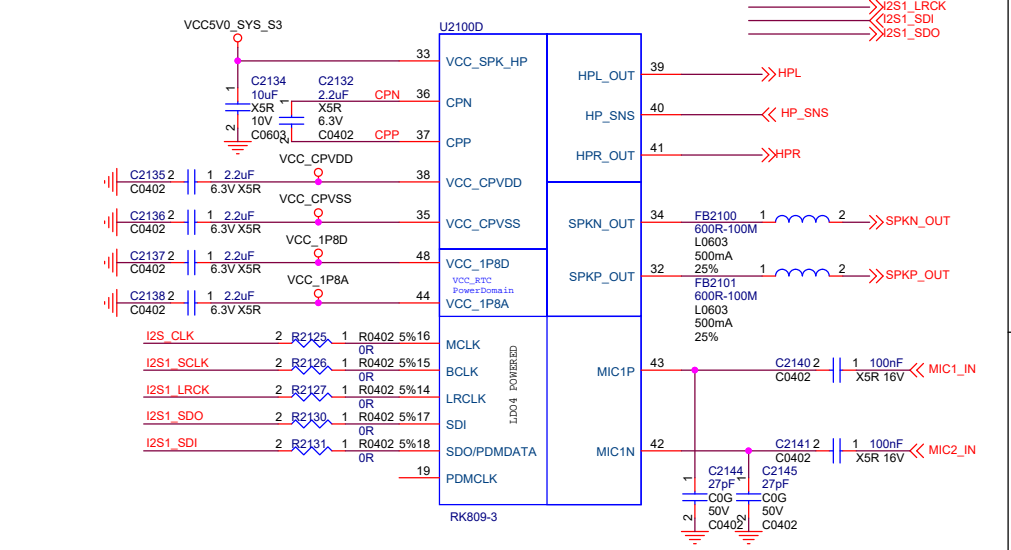
PMIC RK809-3 LDO



PMIC RK809-3 Management



PMIC RK809-3 CODEC



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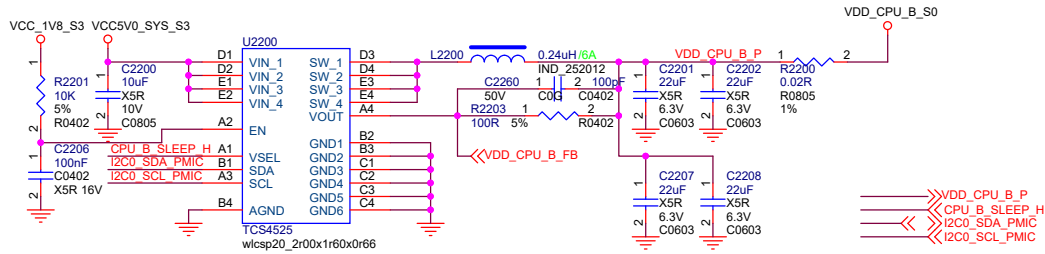
Project: RK3399Pro LP3S178P232DD8

File: 21-Power-PMIC RK809-3

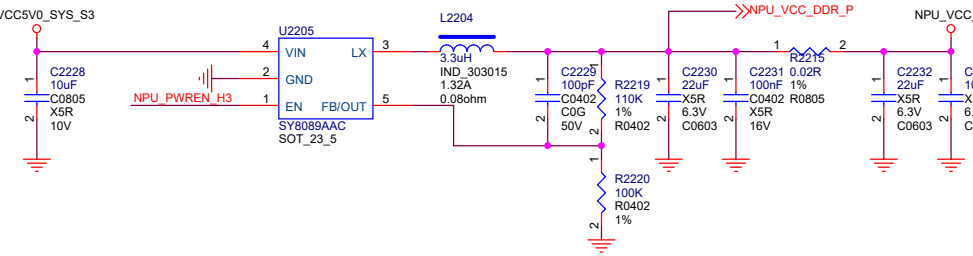
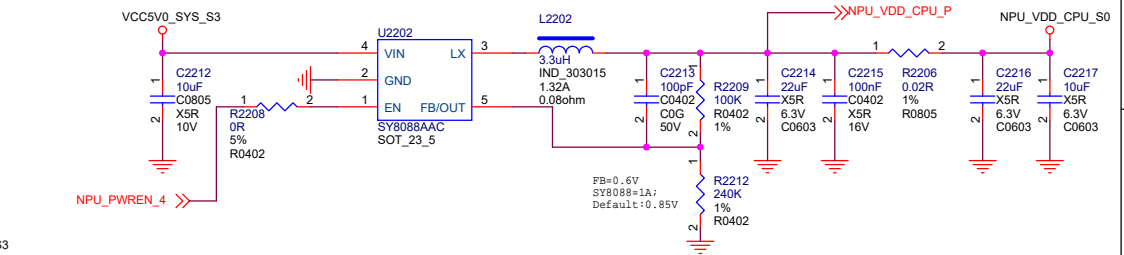
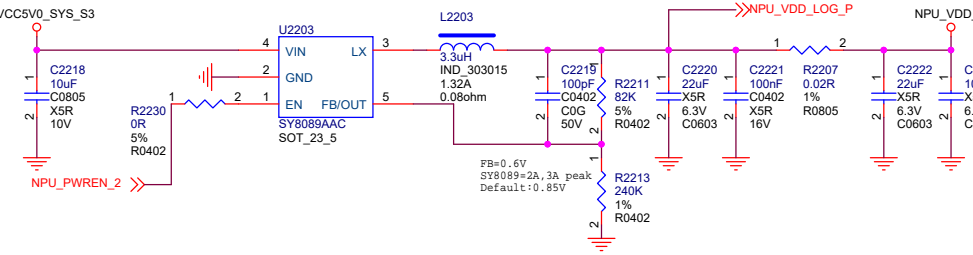
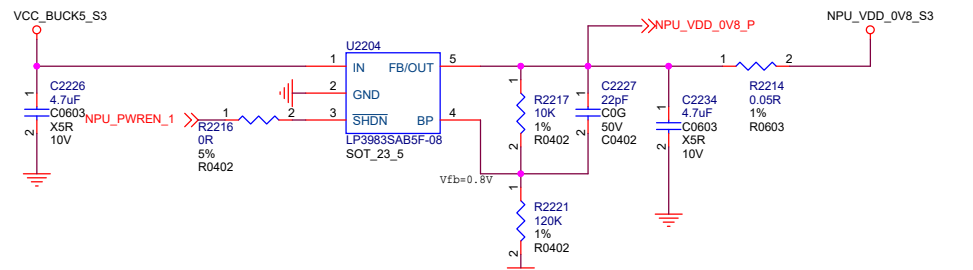
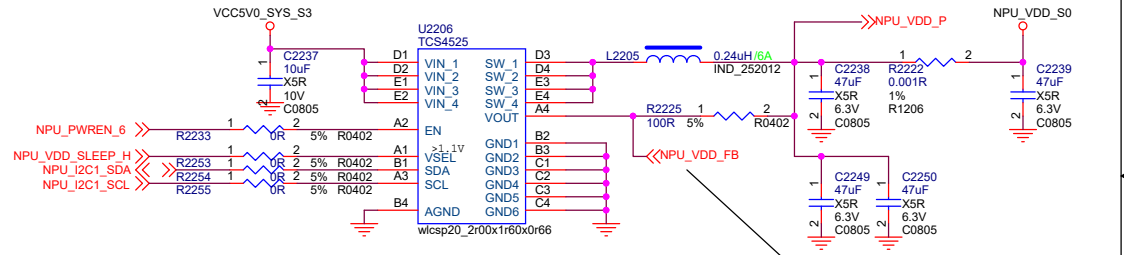
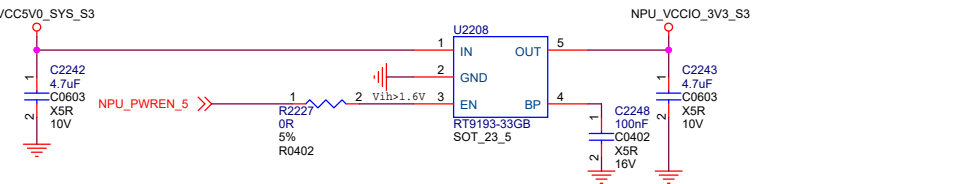
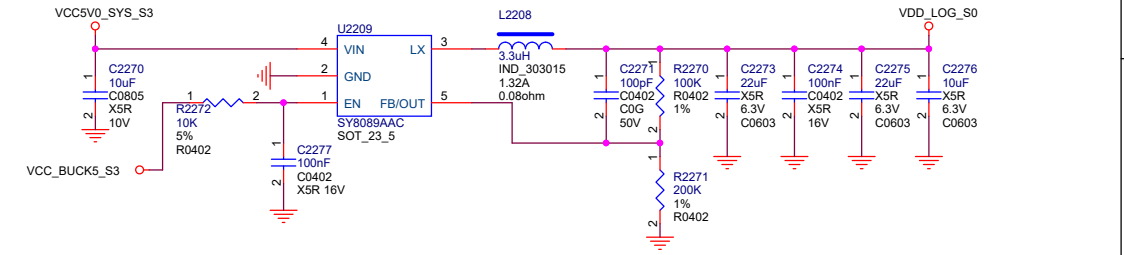
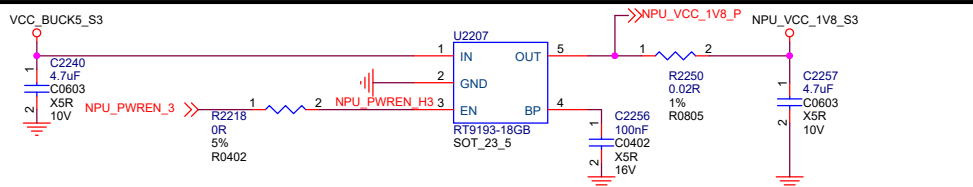
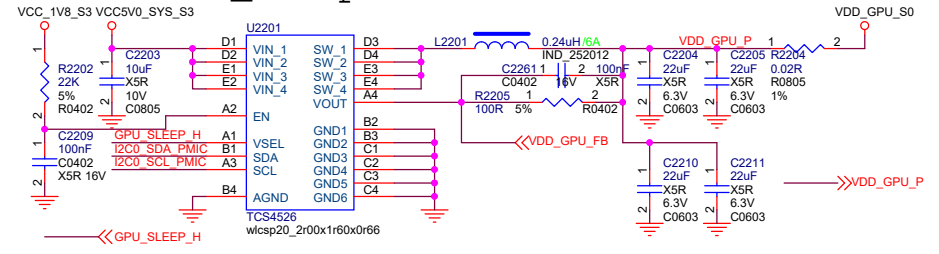
Date: Tuesday, November 20, 2018 Rev: V1.0

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VDD_CPU_B power



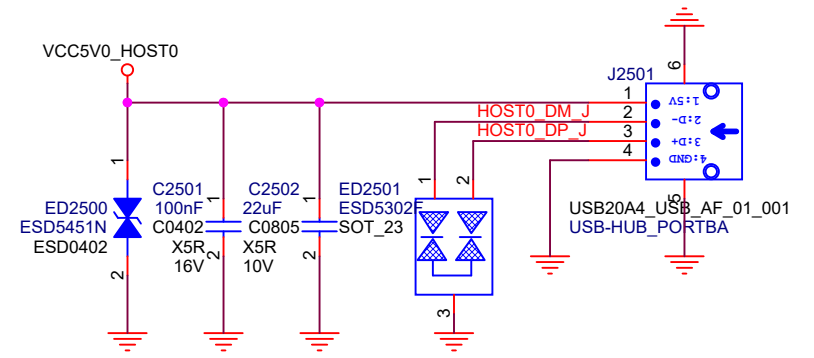
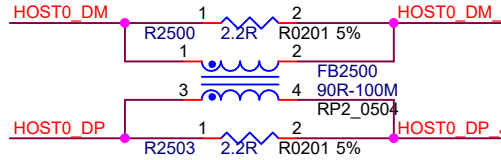
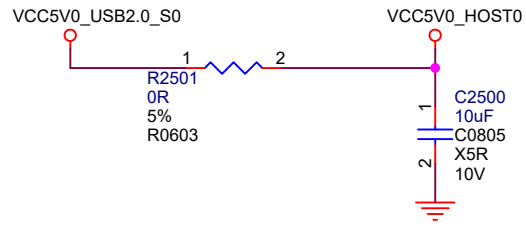
VDD_GPU power



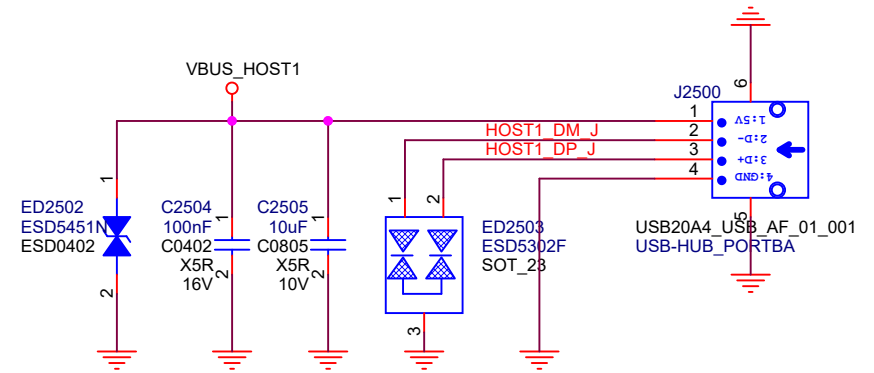
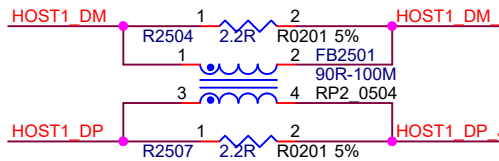
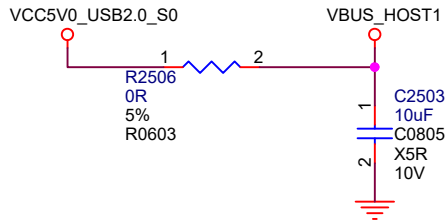
NPU Part power

Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P23DD8		
File:	22.POWER-CPU/GPU/NPU		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	22 of 99

USB2.0 HOST

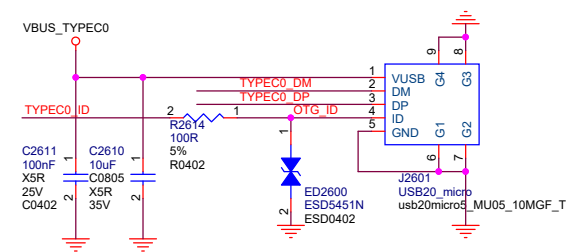
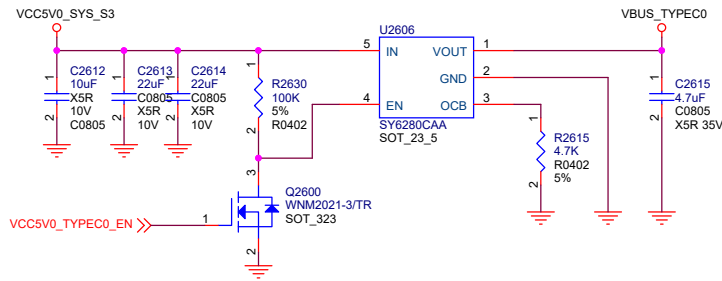
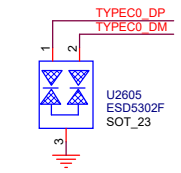
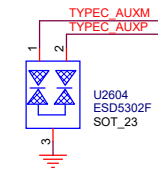
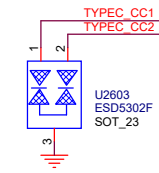
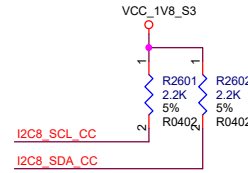
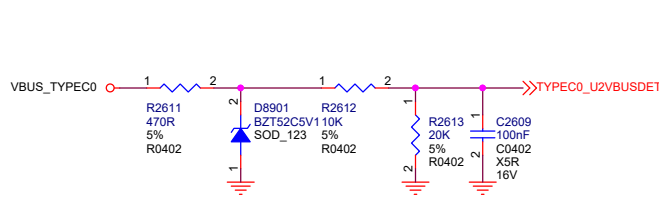
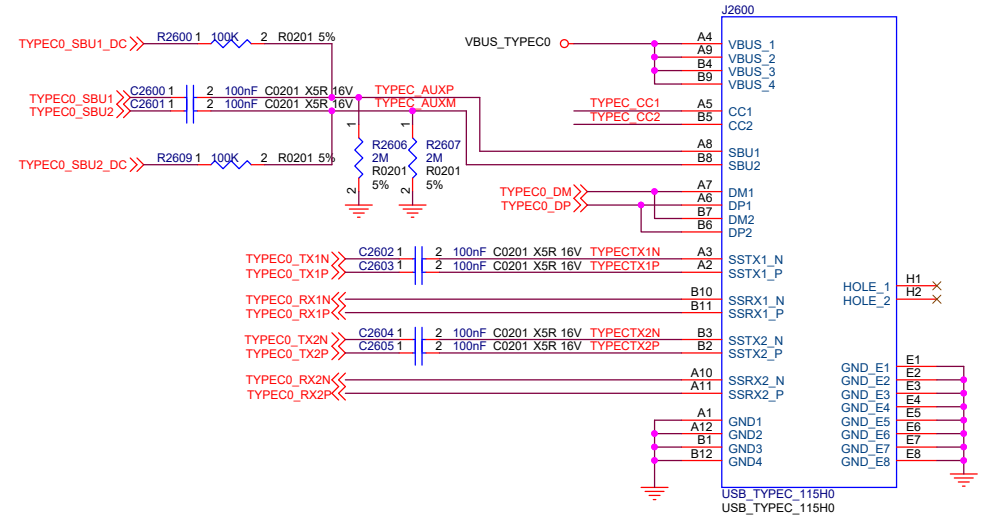
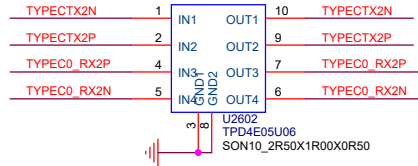
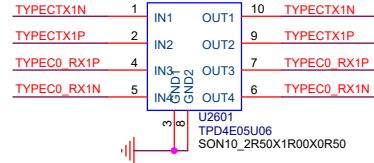
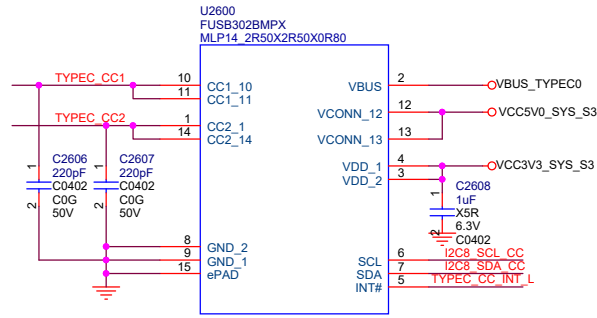


USB2.0 HOST1



TYPE-C PORT

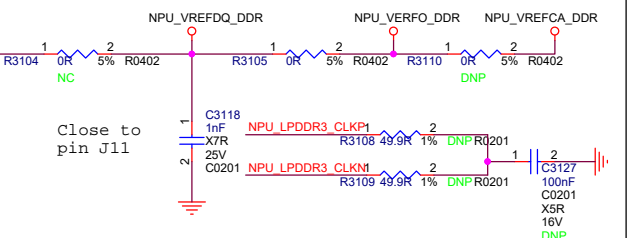
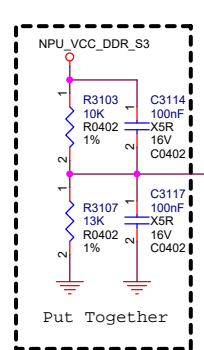
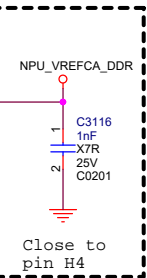
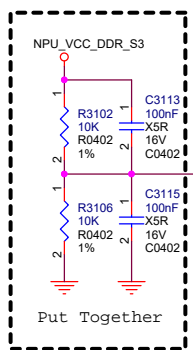
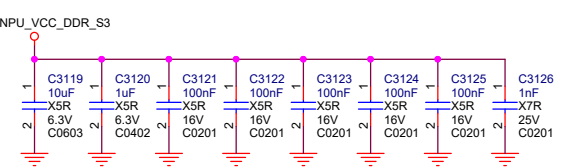
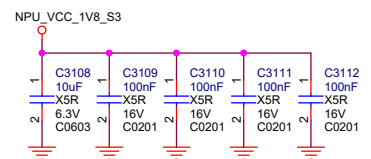
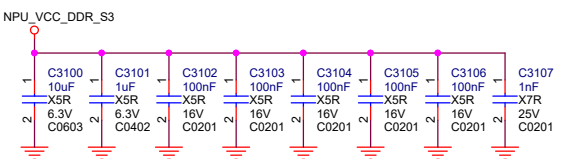
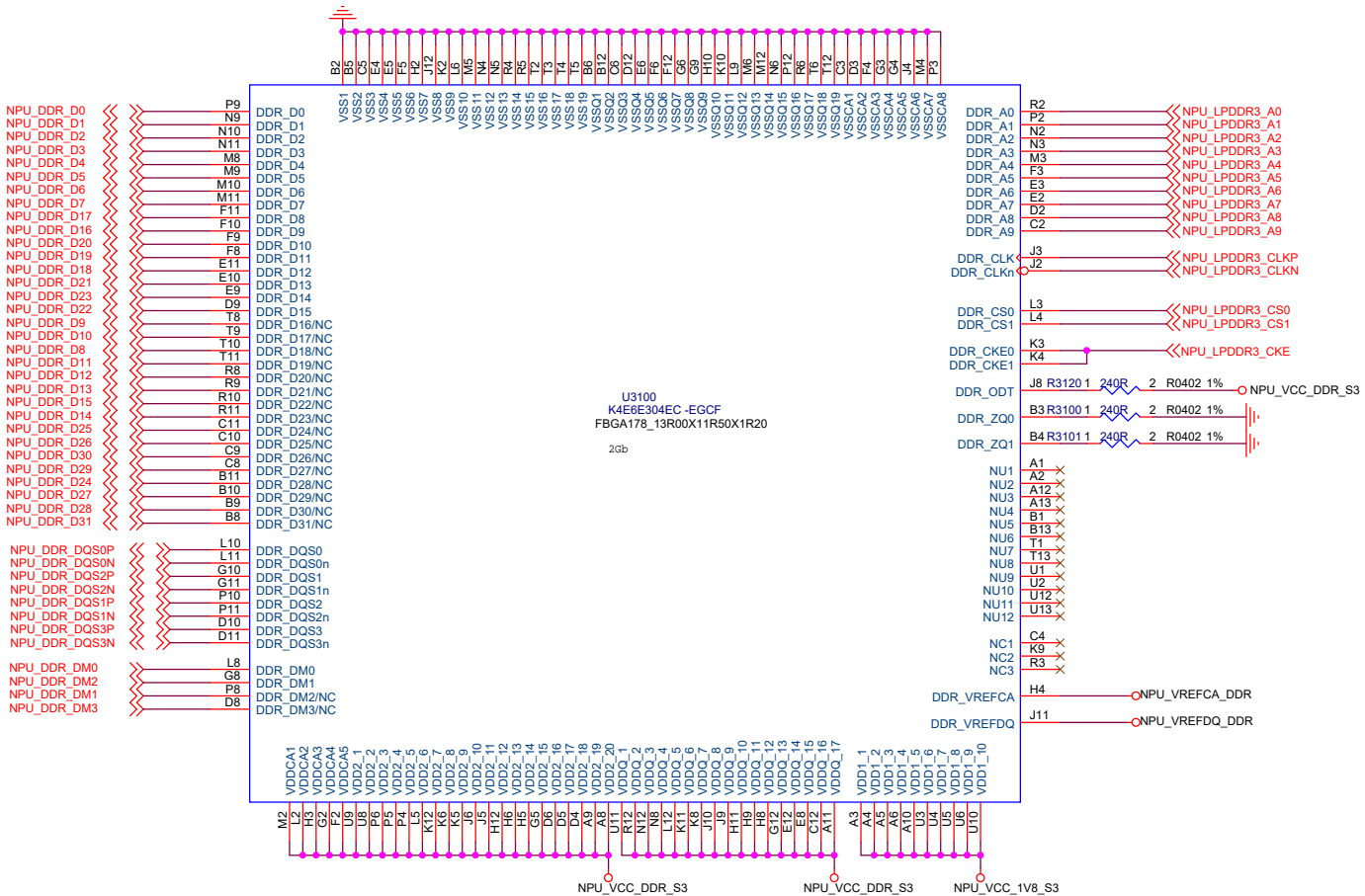
- I2C8_SCL_CC
- I2C8_SDA_CC
- TYPEC0_ID
- TYPEC0_CC_INT_L



VBUS_TYPEC

Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8		
File:	26.TYPEC Port		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	26 of 99

NPU LPDDR3 1x32bit

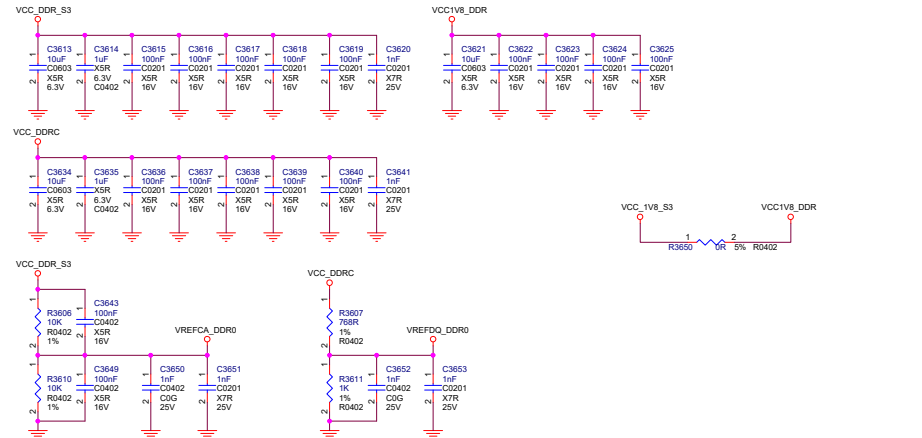
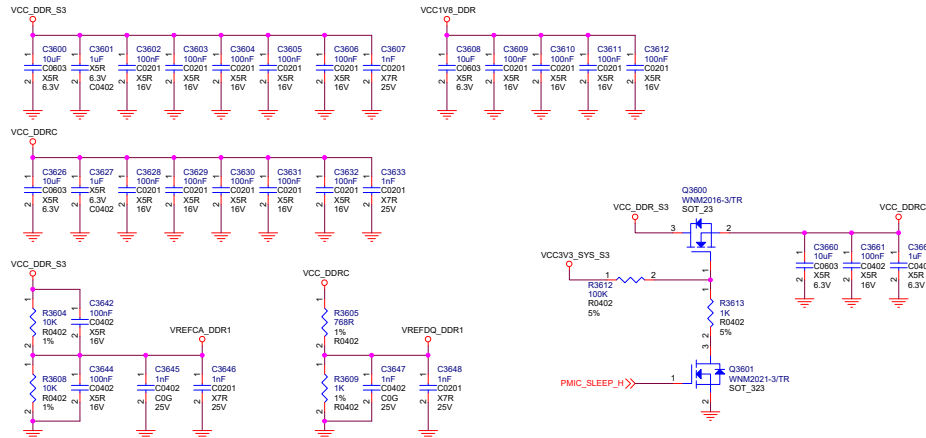
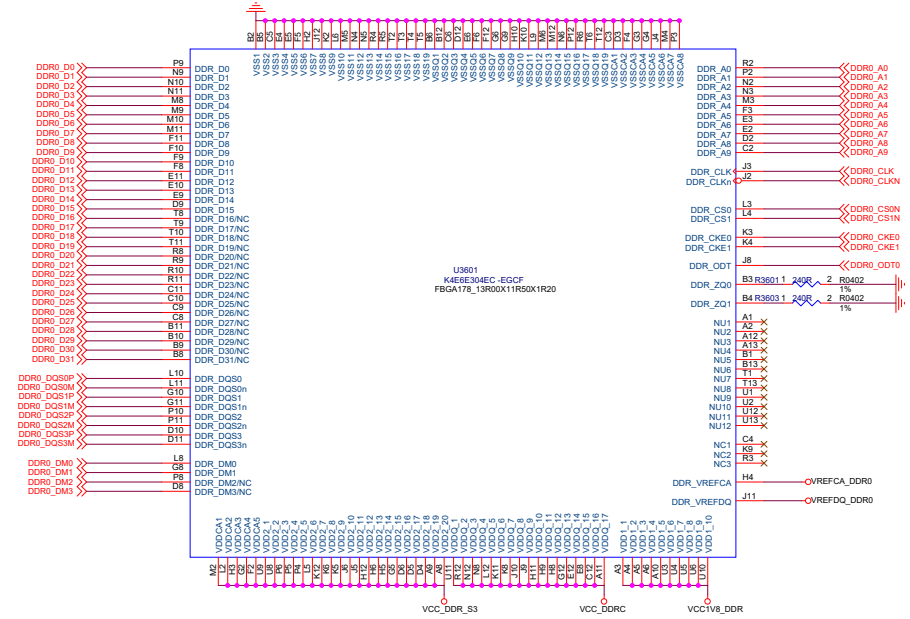
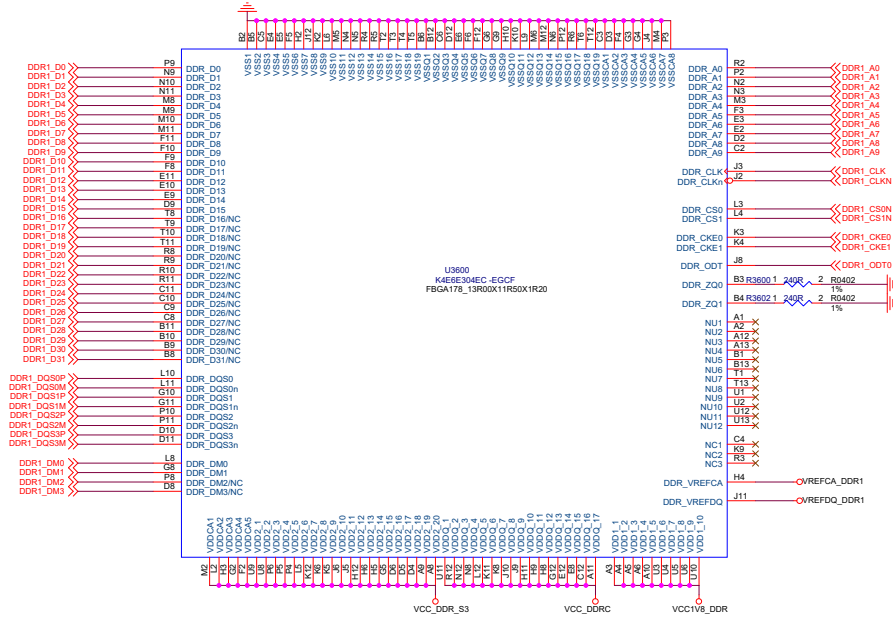


Note: All the power filter capacitors should be placed close to the power pins of LPDDR3

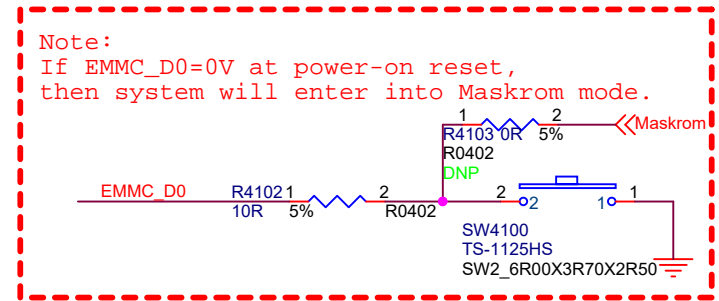
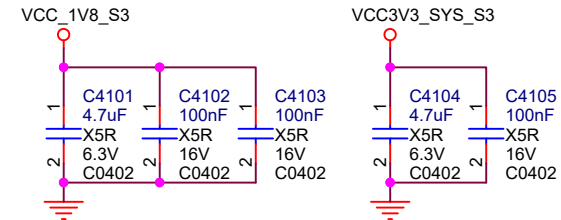
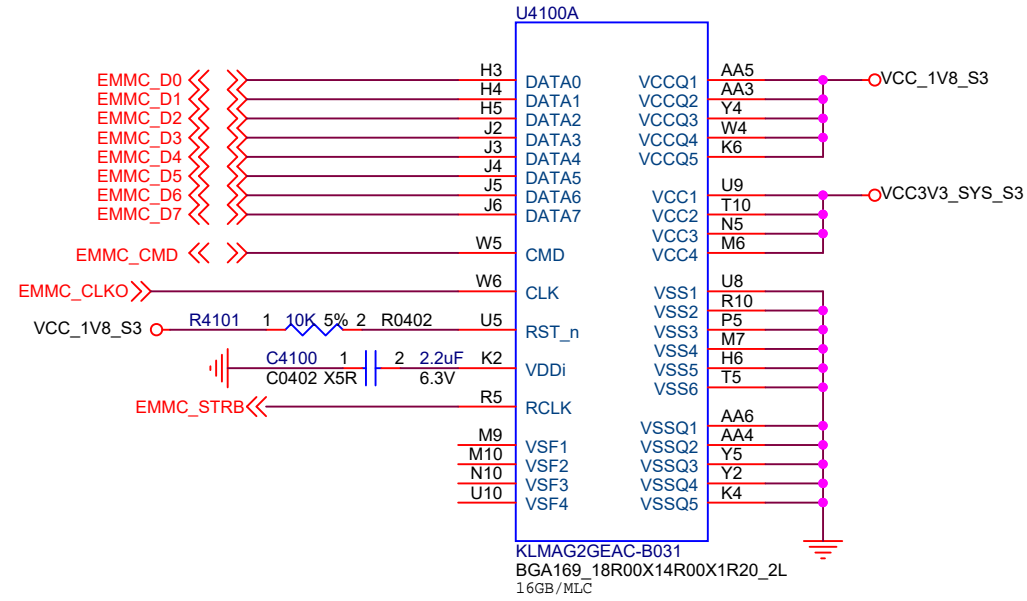
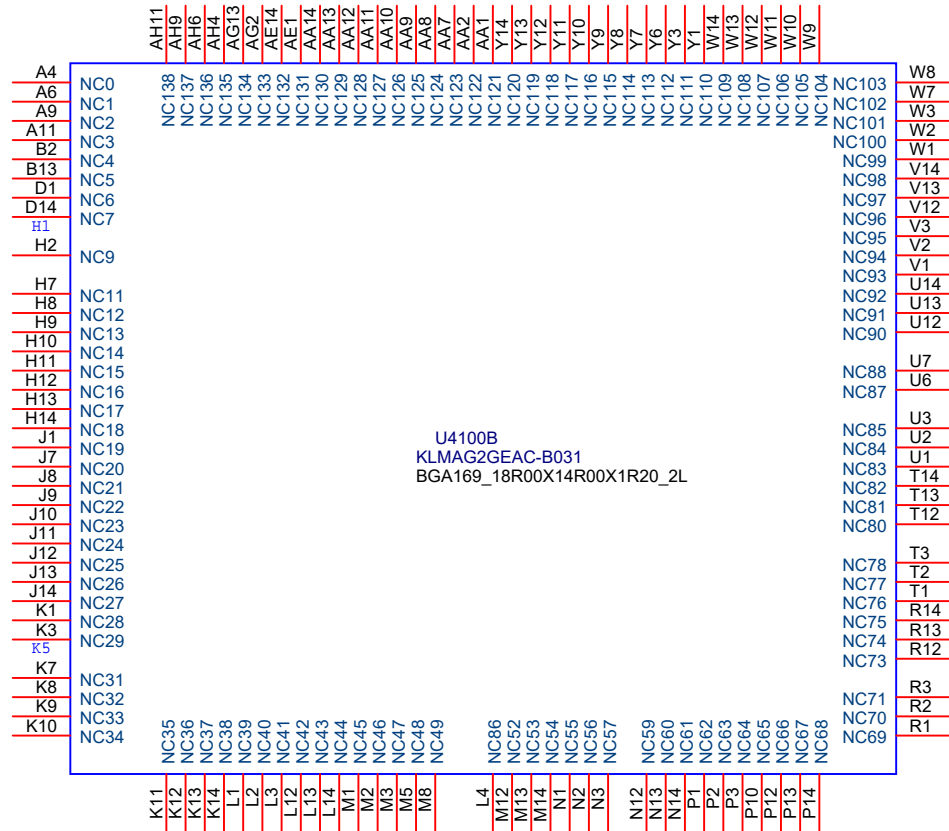
Note:
 $V_{ih} = V_{CC}$
 $V_{il} = V_{CC} * Ron / (Ron + Rodt)$
 $V_{REFDQ_DDR} = (V_{ih} + V_{il}) / 2$
 eg: $V_{CC} = 1.2V$, $Ron = 34ohm$, $Rodt = 240ohm$
 so, $V_{ih} = 1.2V$, $V_{il} = 0.149V$, $V_{REFDQ_DDR} = 0.674V$

Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8		
File:	31.NPU_RAM-LPDDR3 1x32bit		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	31 of 90

LPDDR3

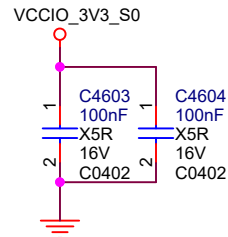
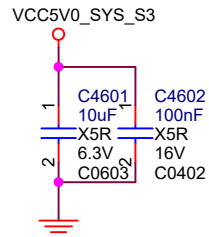
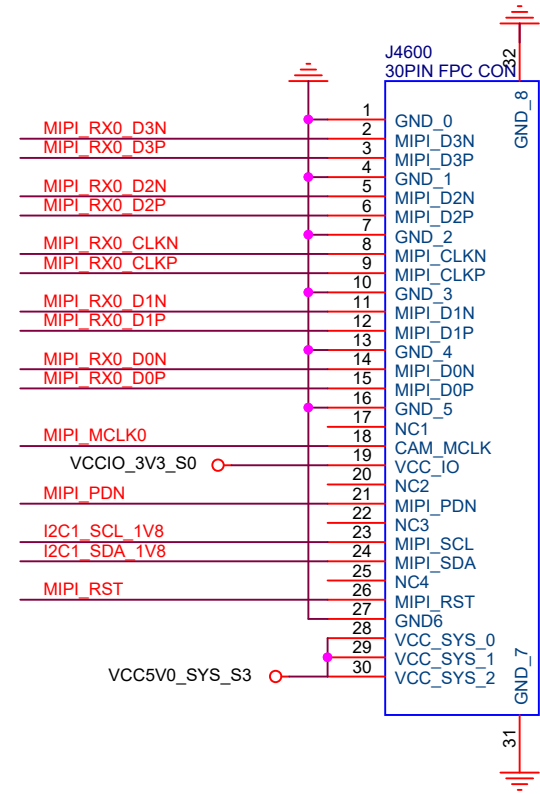
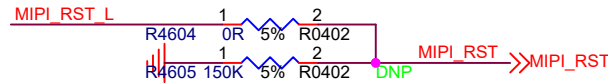
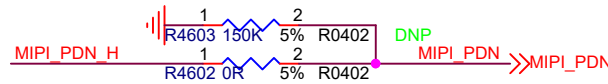
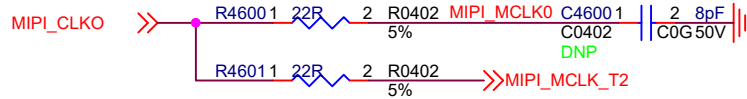
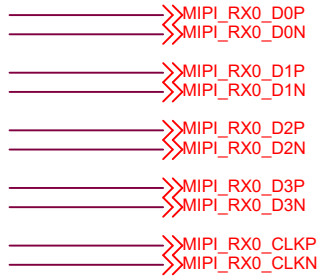


eMMC



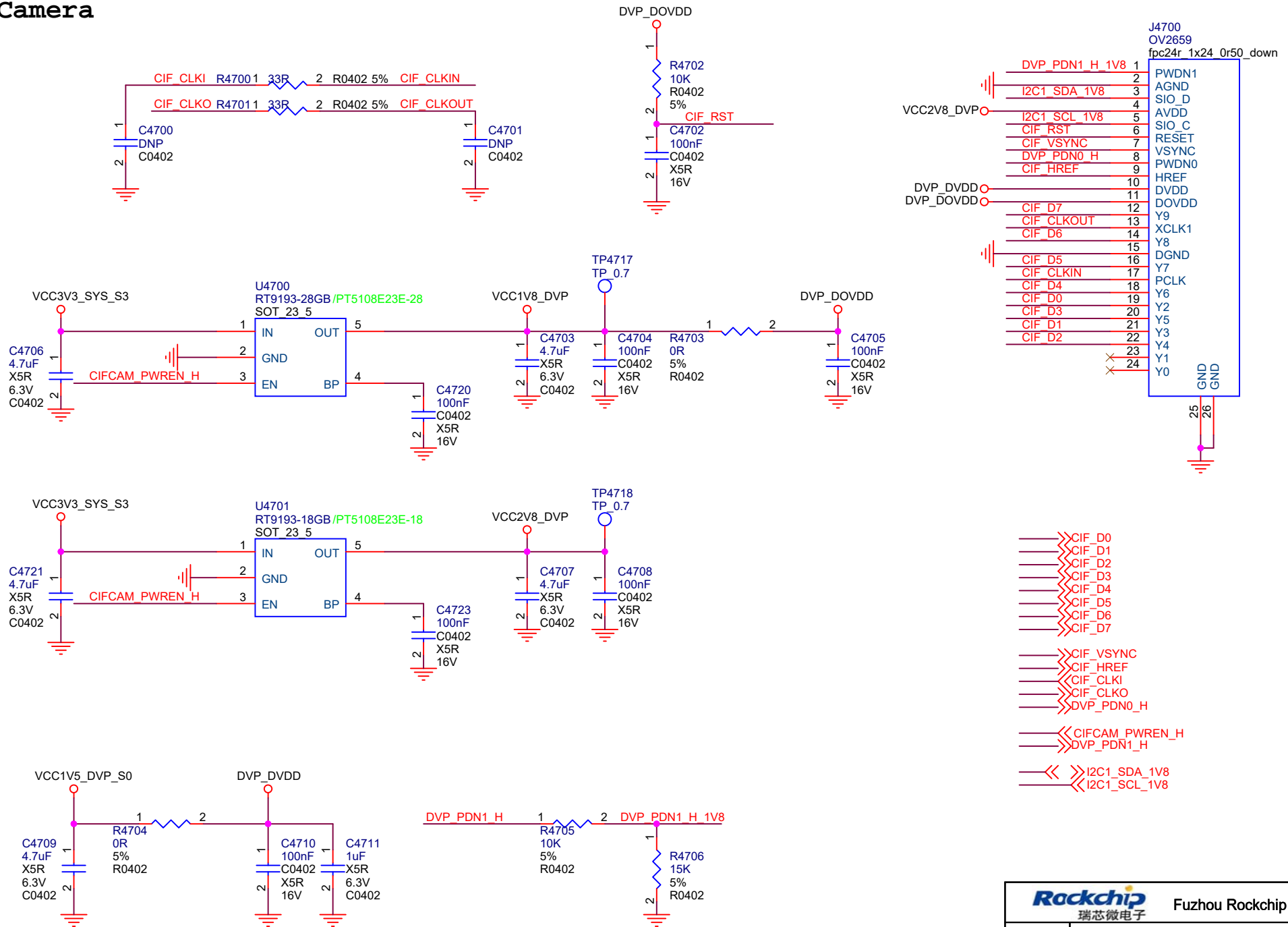
 瑞芯微电子 Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8
File:	41.EMMC
Date:	Thursday, November 15, 2018
Designed by:	Rzf
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MIPI Camera



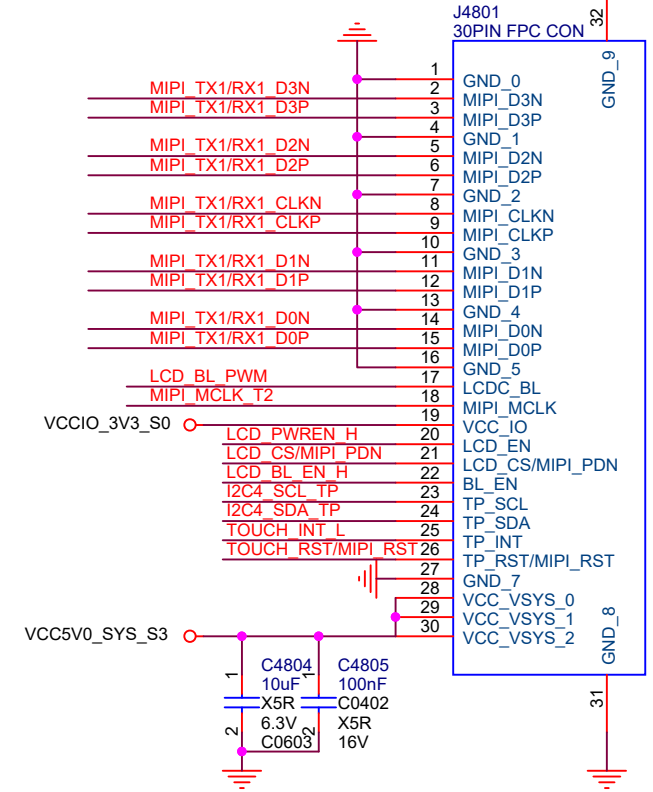
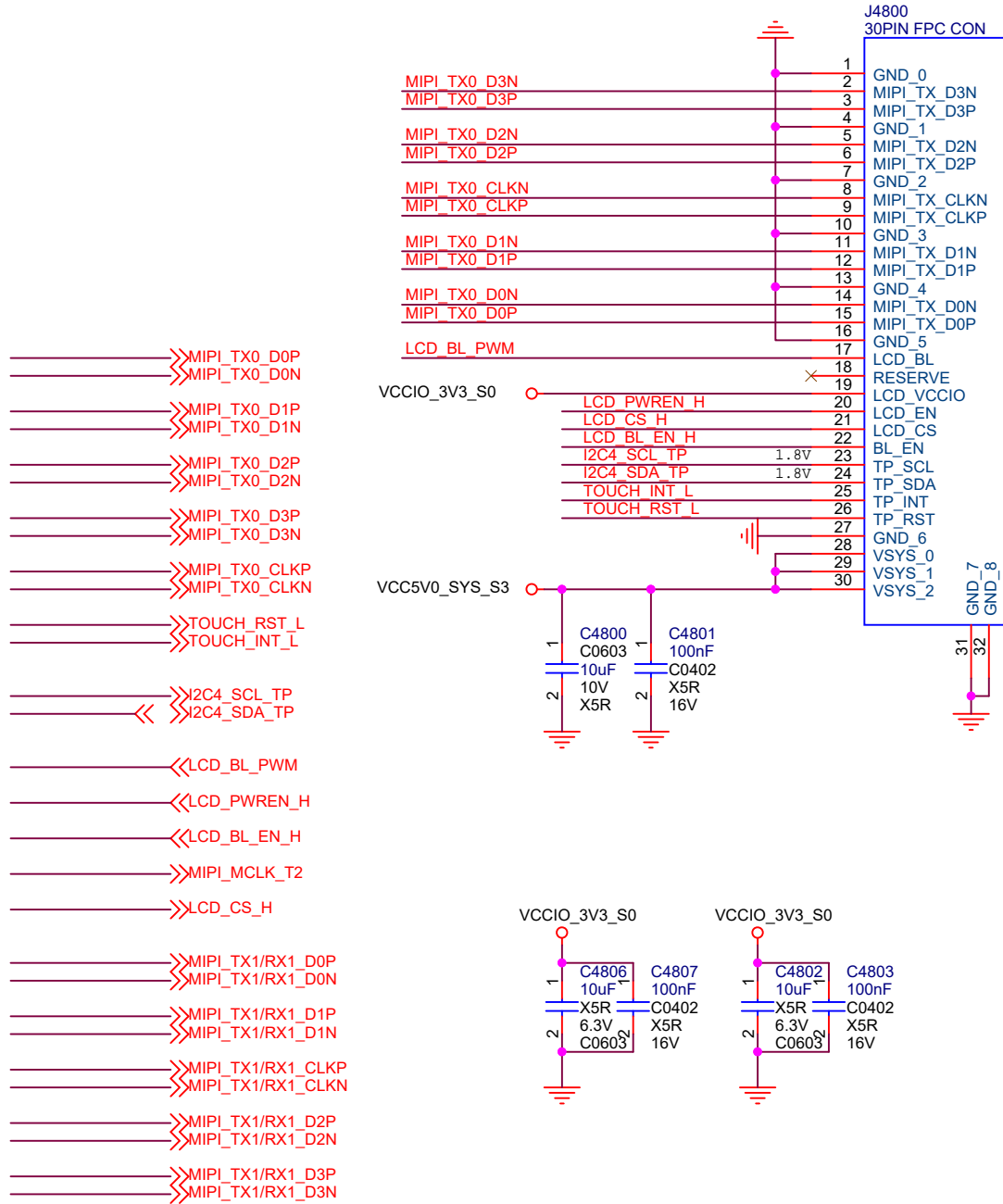
Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8		
File:	MIPI CSI		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	46 of 99

CIF Camera

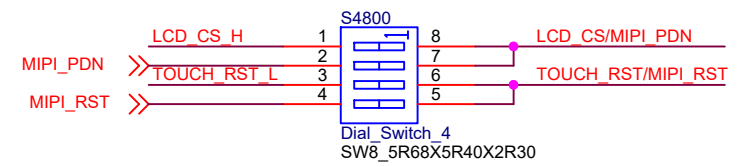


 Fuzhou Rockchip Electronics 瑞芯微电子	
Project:	RK3399Pro LP3S178P232DD8
File:	47.Camera-CIF CSI
Date:	Thursday, November 15, 2018
Designed by:	Rzf
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MIPI DSI

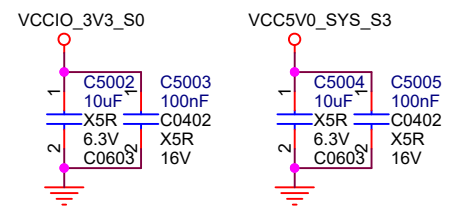
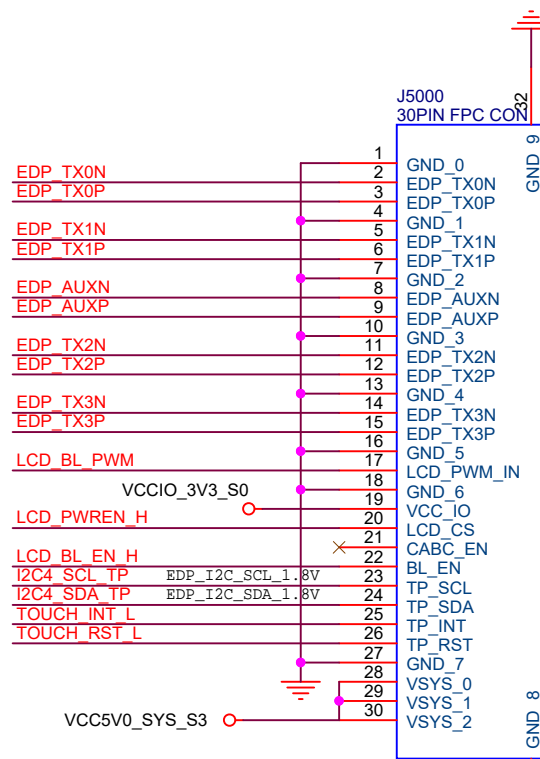
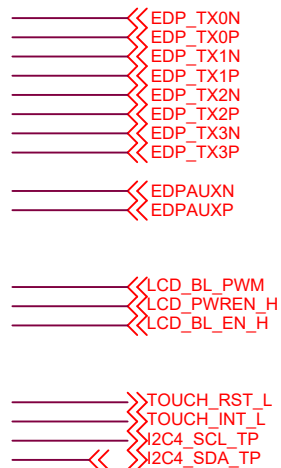
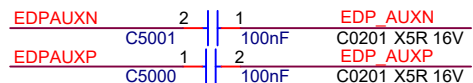


NOTE:
 J4801 insert TX device: S4800 1/8 and 3/6 switch on; others off.
 J4801 insert RX device: S4800 2/7 and 4/5 switch on; others off.



 Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8
File:	48.MIPI DSI
Date:	Thursday, November 15, 2018
Designed by:	Rzf
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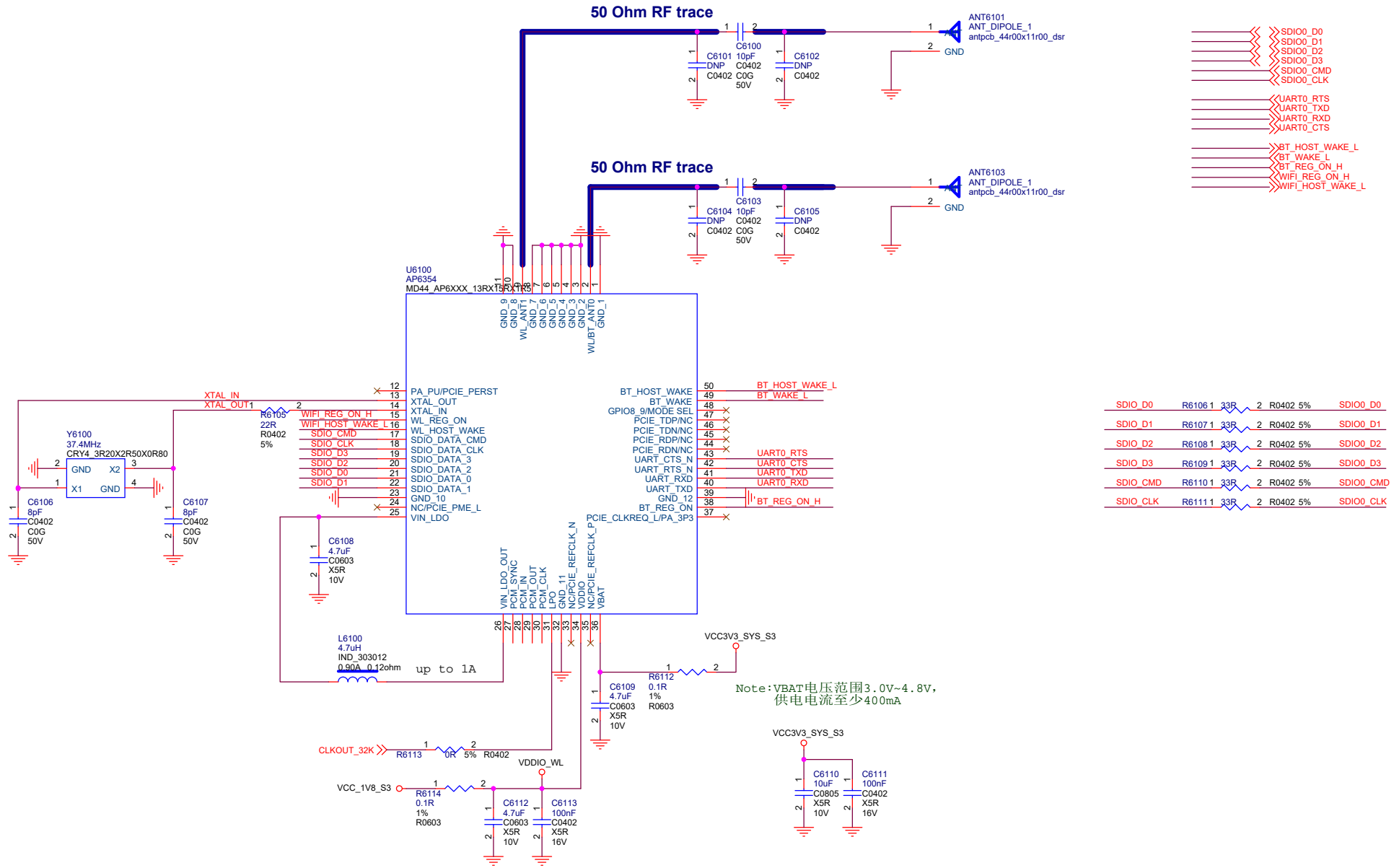
eDP PORT



Rockchip Fuzhou Rockchip Electronics
瑞芯微电子

Project:	RK3399Pro LP3S178P232DD8		
File:	50.LCM-eDP Panel		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	50 of 99

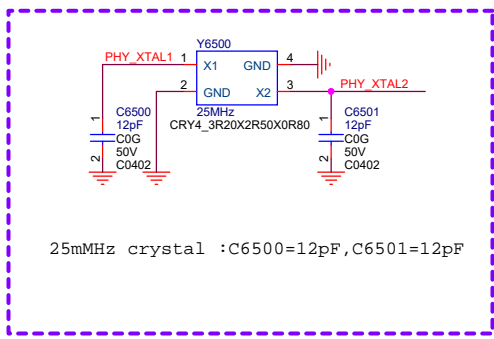
WIFI/BT MODULE



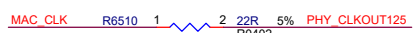
- >>SDIO0_D0
 - >>SDIO0_D1
 - >>SDIO0_D2
 - >>SDIO0_D3
 - >>SDIO0_CMD
 - >>SDIO0_CLK
 - >>UART0_RTS
 - >>UART0_TXD
 - >>UART0_RXD
 - >>UART0_CTS
 - >>BT_HOST_WAKE_L
 - >>BT_WAKE_L
 - >>BT_REG_ON_H
 - >>WIFI_REG_ON_H
 - >>WIFI_HOST_WAKE_L
-
- SDIO_D0 R6106 1 33R 2 R0402 5% SDIO0_D0
 - SDIO_D1 R6107 1 33R 2 R0402 5% SDIO0_D1
 - SDIO_D2 R6108 1 33R 2 R0402 5% SDIO0_D2
 - SDIO_D3 R6109 1 33R 2 R0402 5% SDIO0_D3
 - SDIO_CMD R6110 1 33R 2 R0402 5% SDIO0_CMD
 - SDIO_CLK R6111 1 33R 2 R0402 5% SDIO0_CLK

Note: VBAT电压范围3.0V~4.8V, 供电电流至少400mA

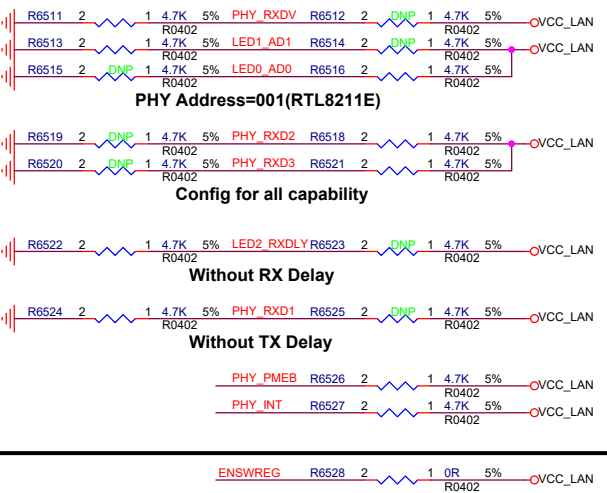
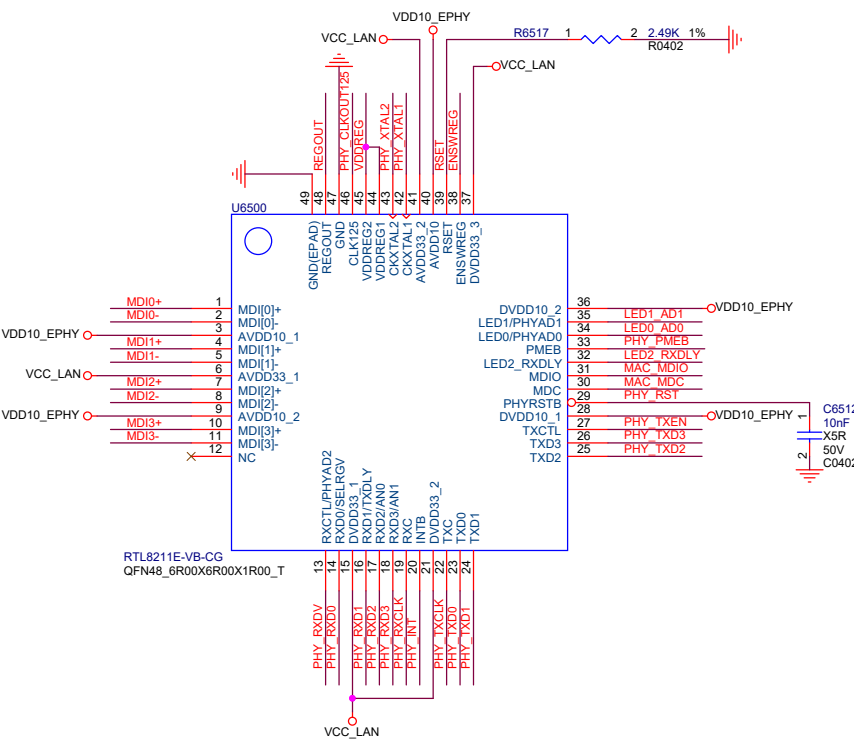
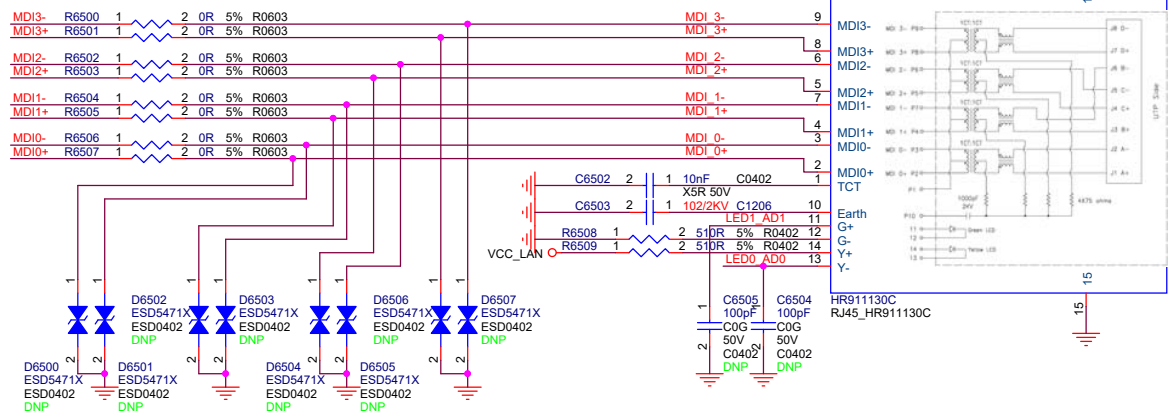
- >>PHY_TXD0
- >>PHY_TXD1
- >>PHY_TXD2
- >>PHY_TXD3
- >>PHY_TXEN
- >>PHY_TXCLK
- <<MAC_RXD0
- <<MAC_RXD1
- <<MAC_RXD2
- <<MAC_RXD3
- <<MAC_RXDV
- <<MAC_RXCLK
- <<MAC_CLK
- >>MAC_MDIO
- >>MAC_MDC
- >>PHY_RST
- >>PHY_INT
- >>PHY_PMEB



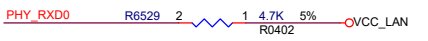
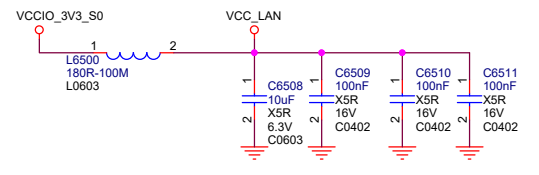
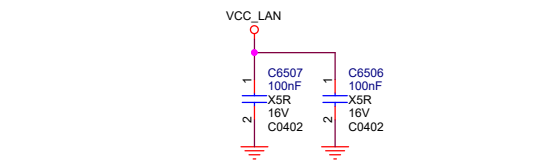
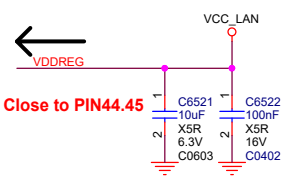
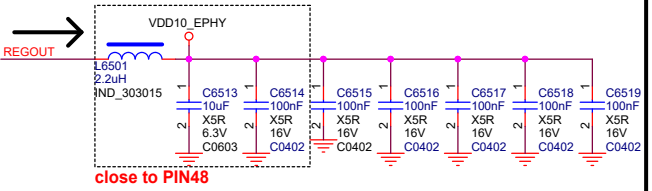
25mHz crystal :C6500=12pF,C6501=12pF



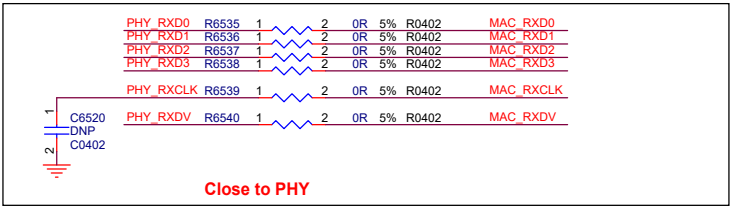
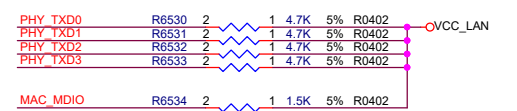
MAC <----- PHY



Connect ENSWREG to AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.



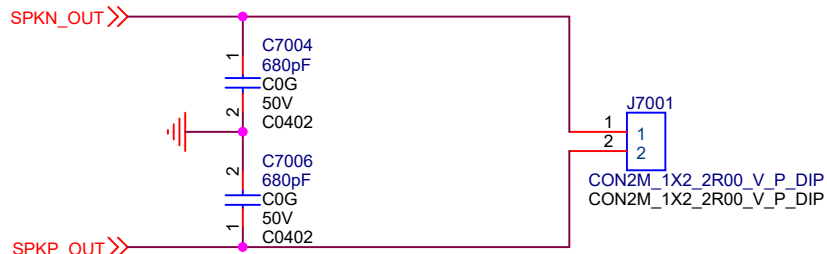
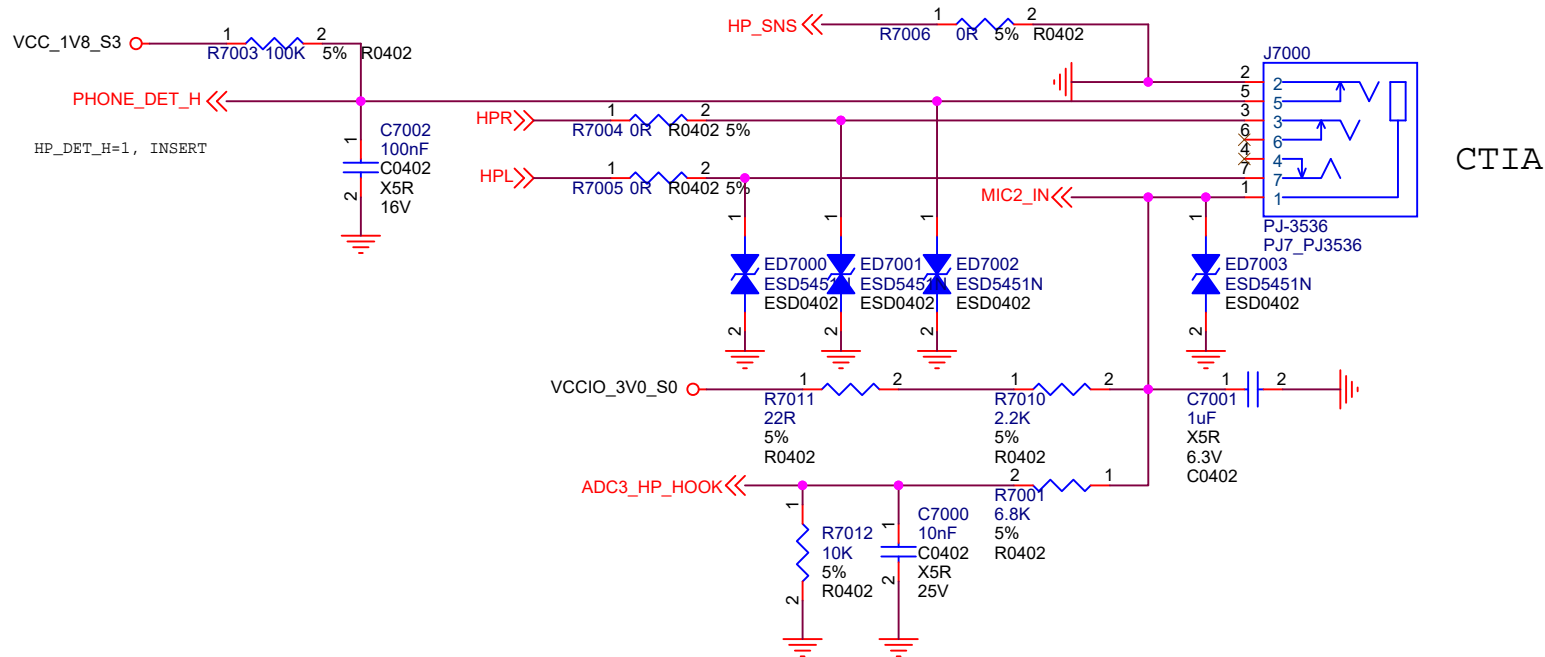
Pull down for 2.5V RGMII(RTL8211D/8211E)
Pull up for 3.3V RGMII (RTL8211D/8211E)
Pull up 1.5 /1.8V RGMII (RTL8211E-VL only)



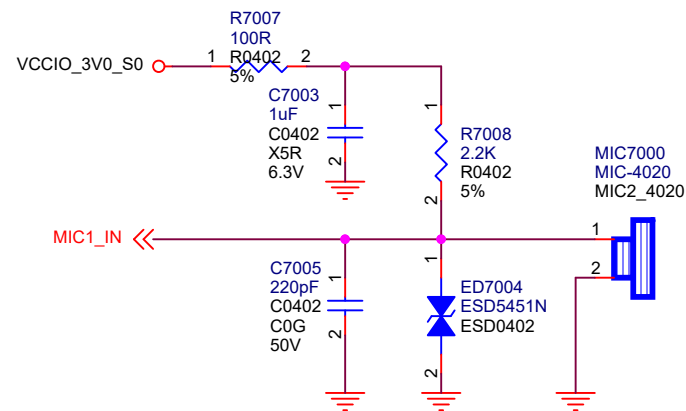
RGMII 100M

Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8		
File:	65.RGMII-10/100/1000M		
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Designed by:	Rzf	Sheet:	65 of 90

HEADPHONE



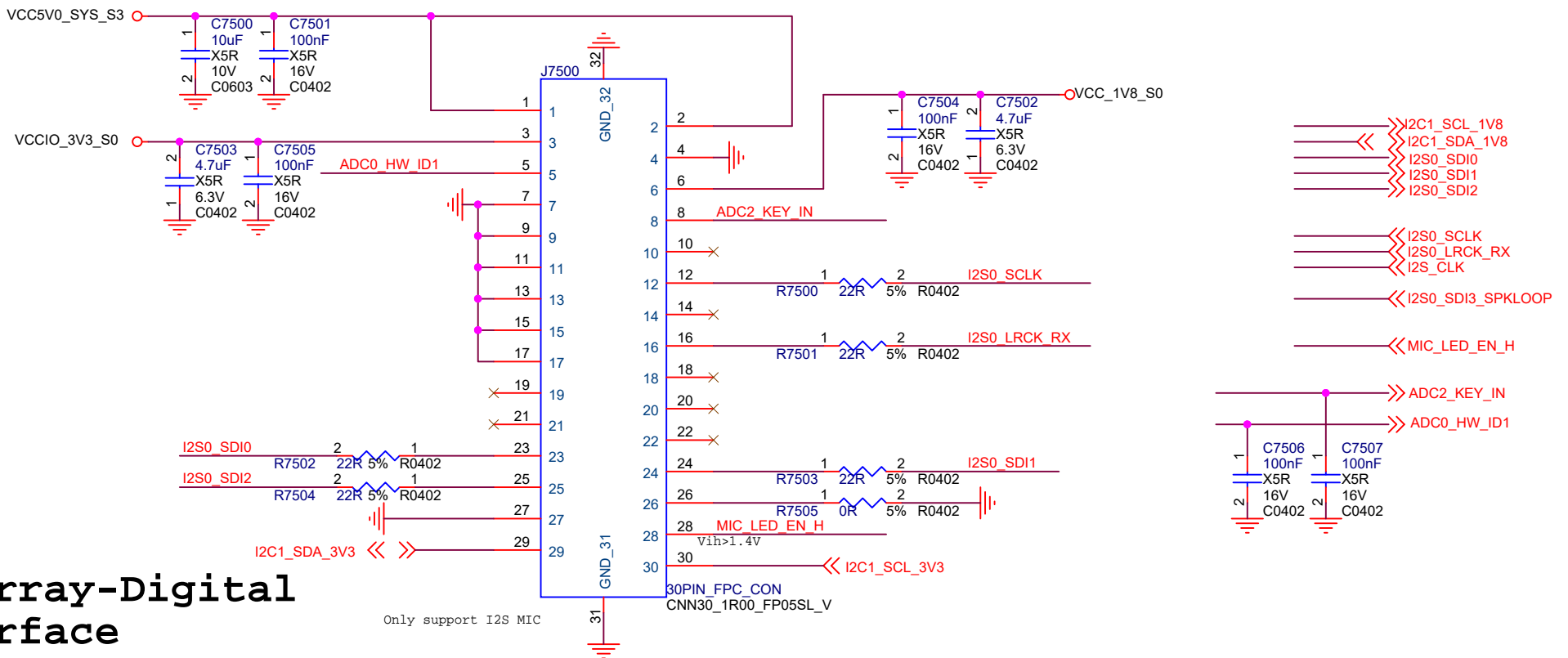
SPEAKER



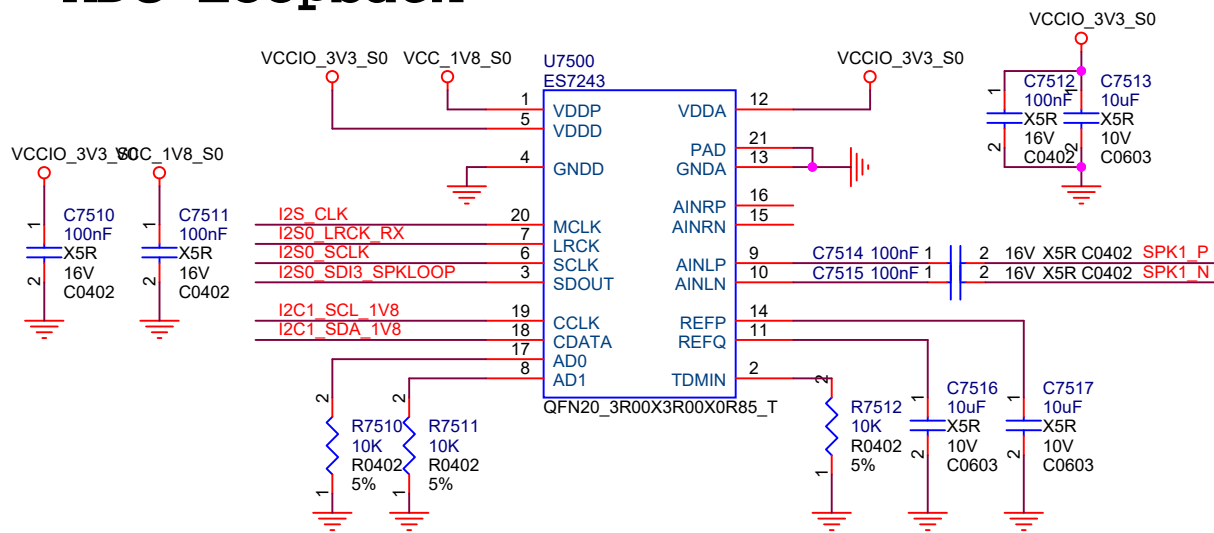
MIC

 Fuzhou Rockchip Electronics 瑞芯微电子	
Project:	RK3399Pro LP3S178P232DD8
File:	70.AUDIO1
Date:	Thursday, November 15, 2018
Designed by:	Rzf
Rev:	V1.0
Sheet:	70 of 99

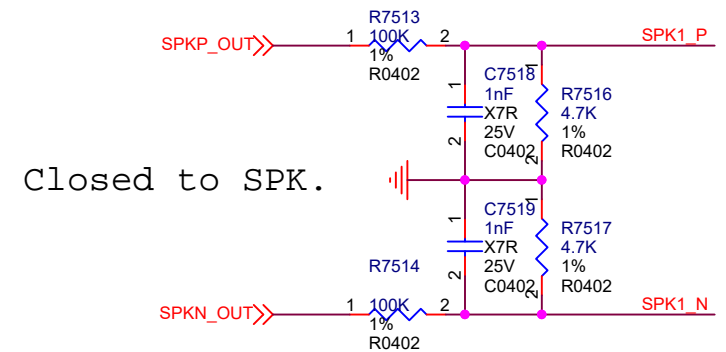
MIC Array-Digital Interface



ADC Loopback



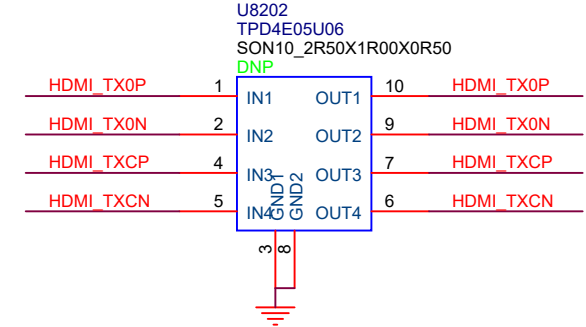
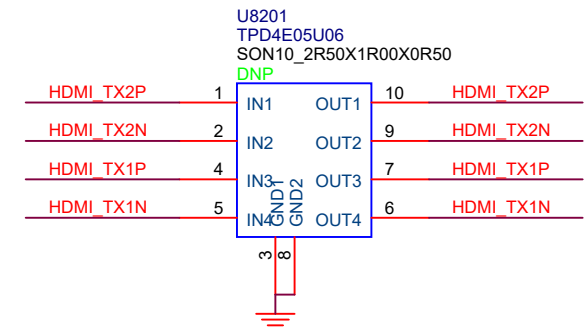
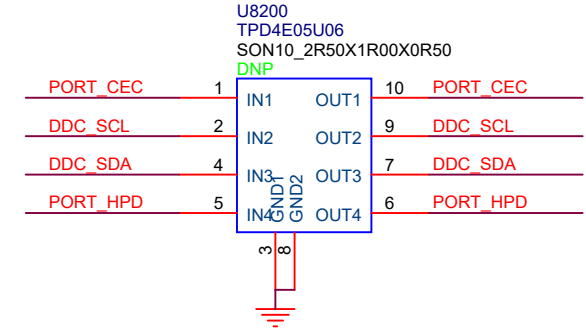
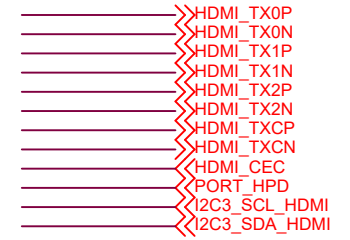
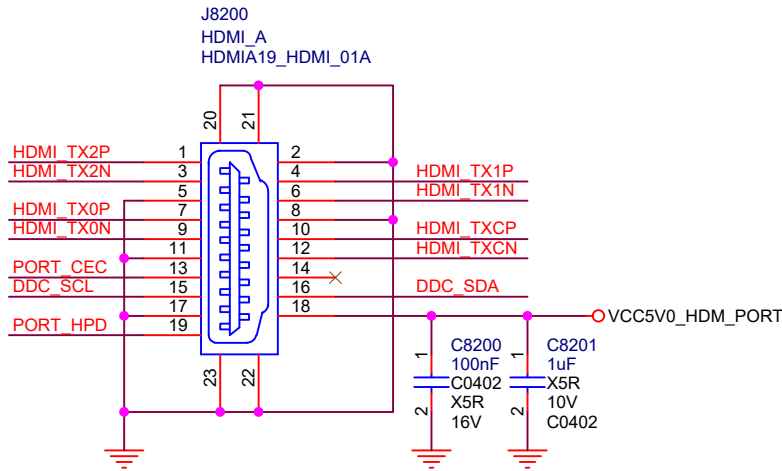
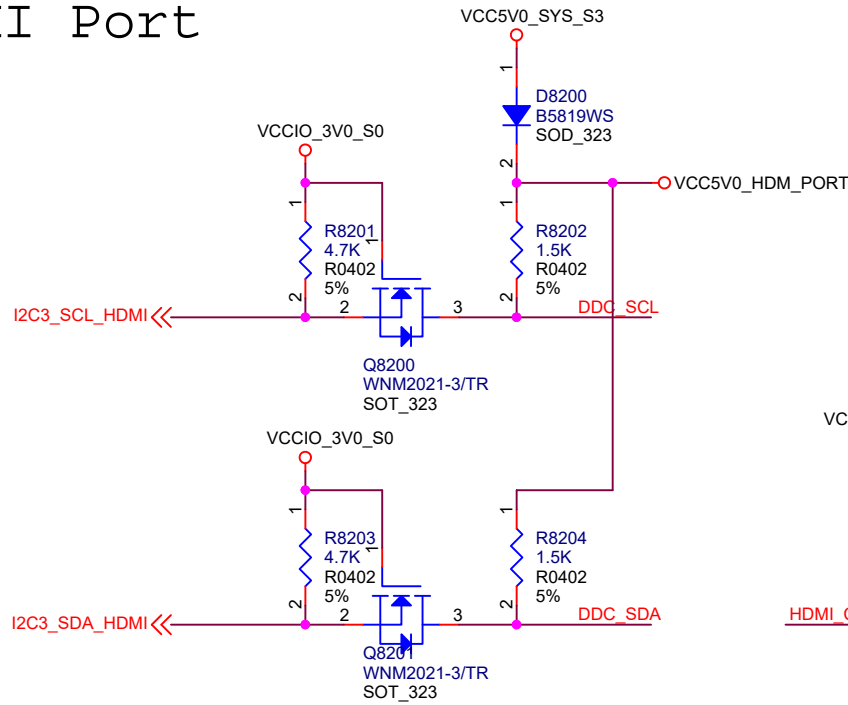
I2C Chip ID = 0x26
Place this loopback ADC close to Amplifier.




Notice the divided voltage should be suit to the ADC input parameters.

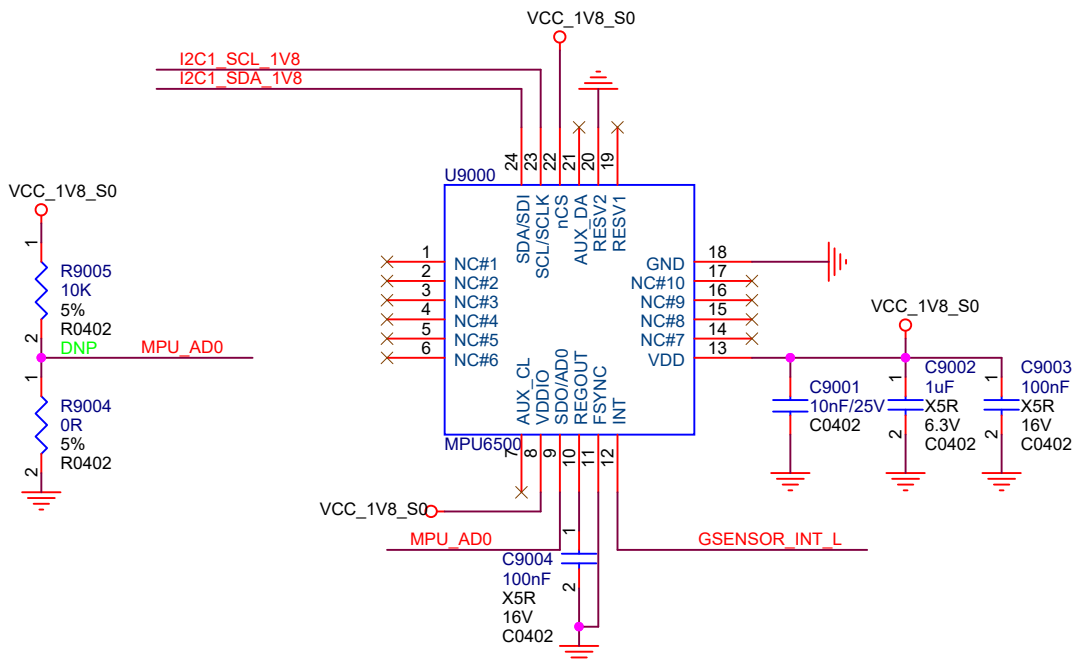
Rackchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8		
File:	75.AUDIO2-MIC Array Connector		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	75 of 99

HDMI Port



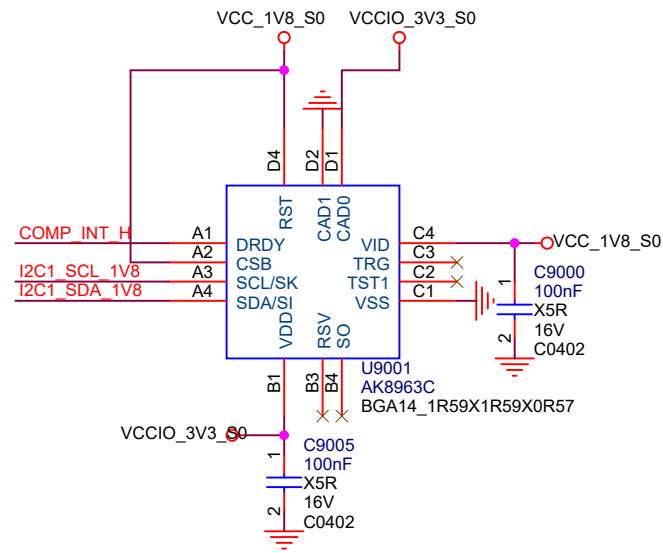
 Fuzhou Rockchip Electronics 瑞芯微电子	
Project:	RK3399Pro LP3S178P232DD8
File:	82.HDMI Port
Date:	Thursday, November 15, 2018
Designed by:	Rzf
Rev:	V1.0
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Gyroscope+G-sensor

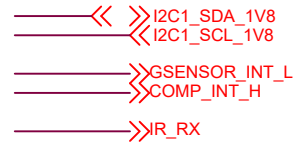
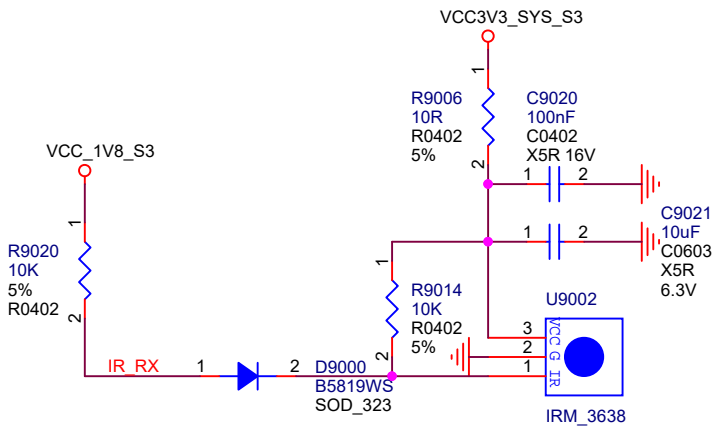



Compass

Note:
The first pin of AK8963C must be placed on the lower left corner of PCB.

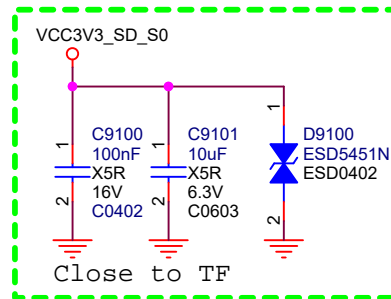
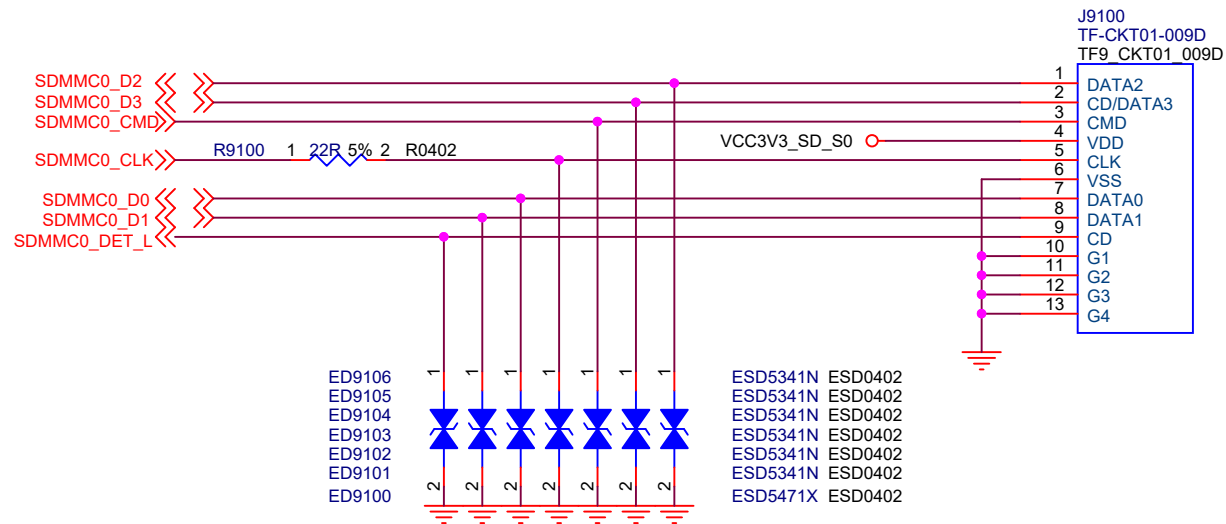


IR



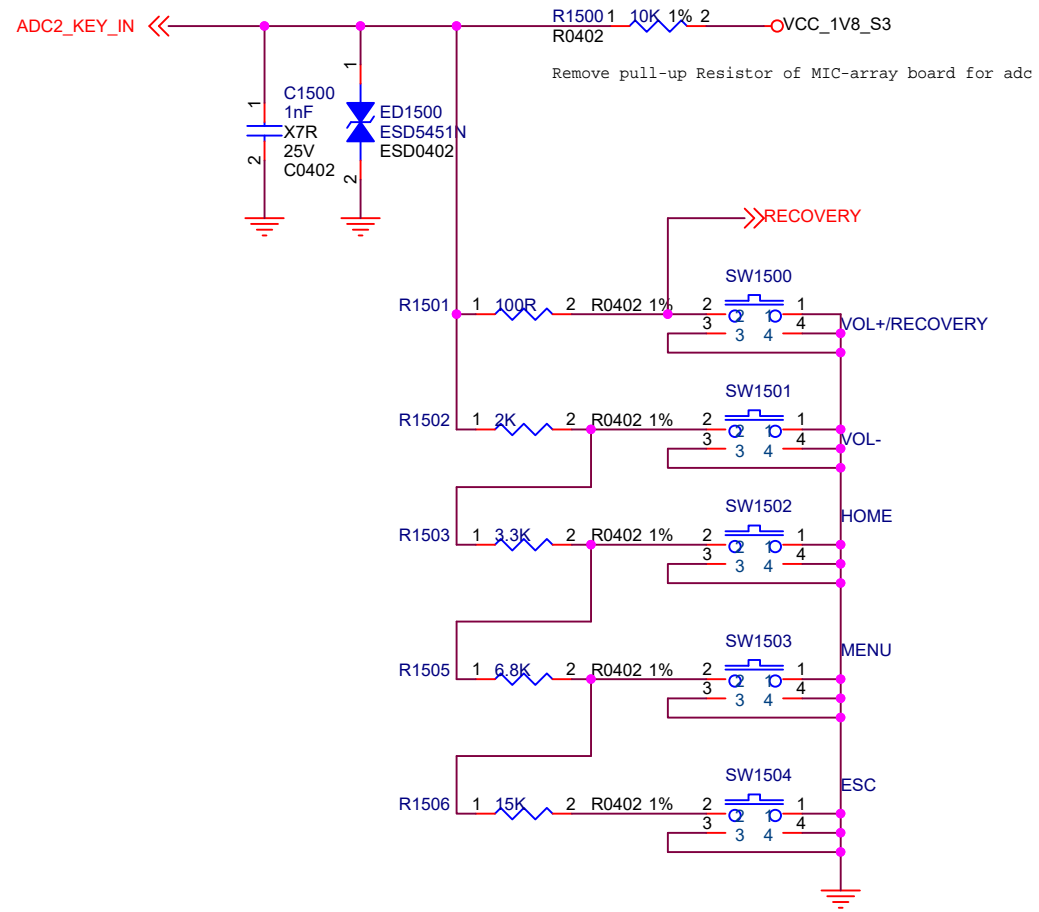
 Fuzhou Rockchip Electronics 瑞芯微电子			
Project:	RK3399Pro LP3S178P232DD8		
File:	90.Sensor		
Date:	Thursday, November 15, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	90 of 99

TF Card



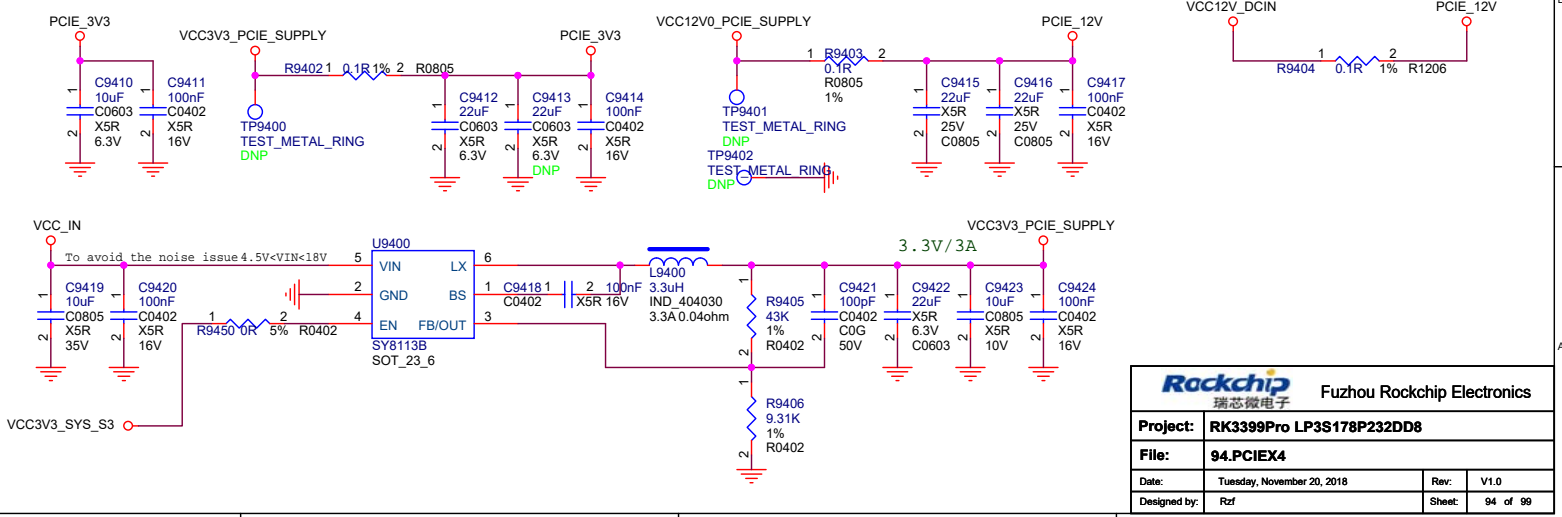
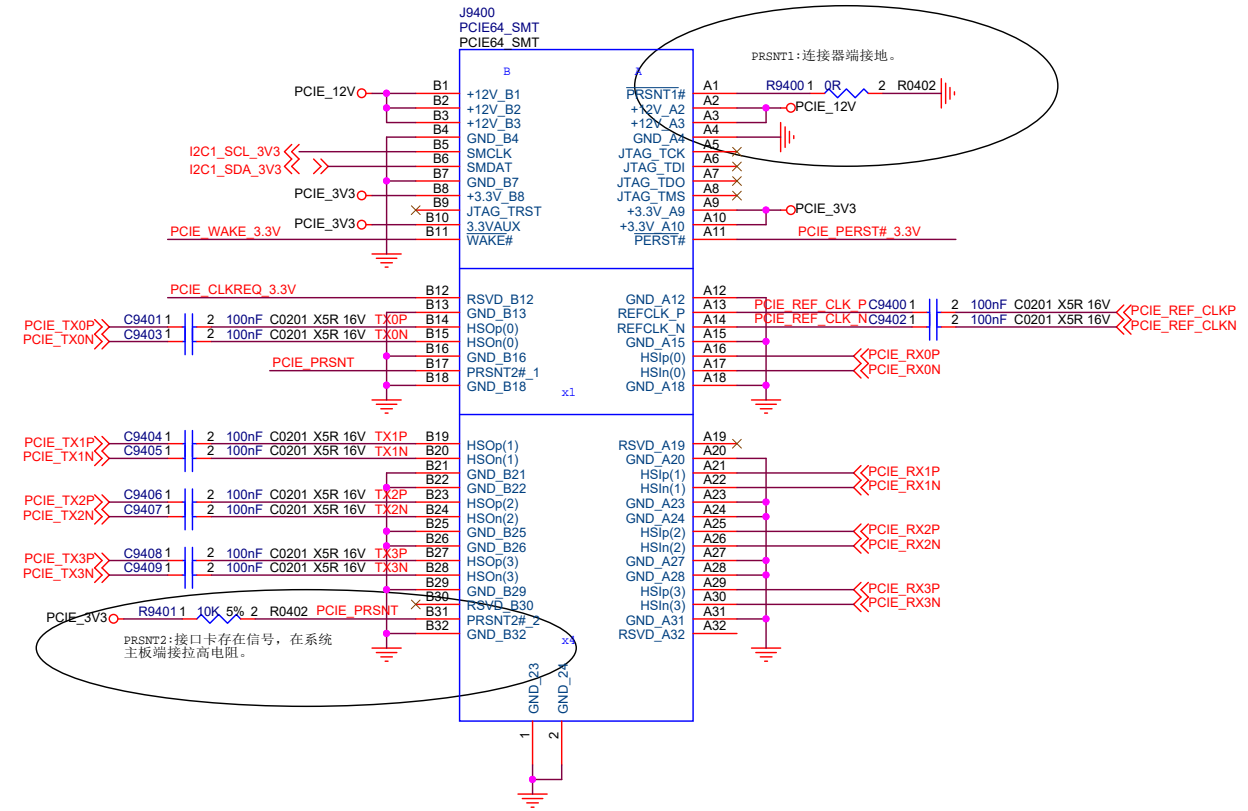
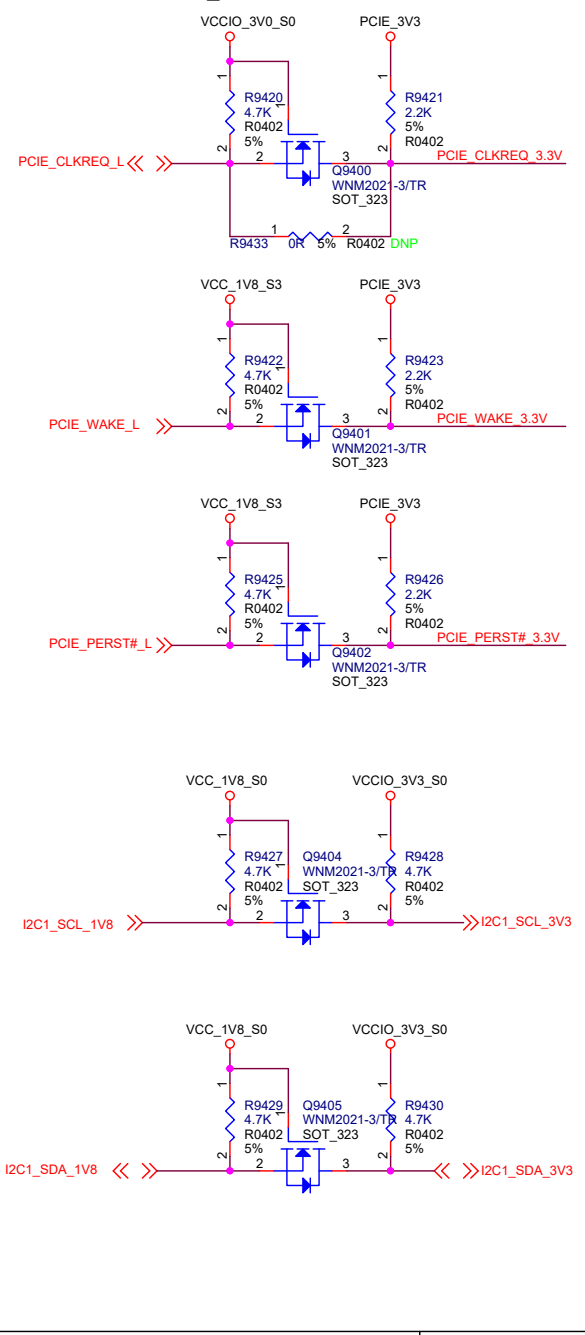
 Fuzhou Rockchip Electronics 瑞芯微电子	
Project:	RK3399Pro LP3S178P232DD8
File:	91.TF Card
Date:	Thursday, November 15, 2018
Designed by:	Rzf
Rev:	V1.0
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Key board



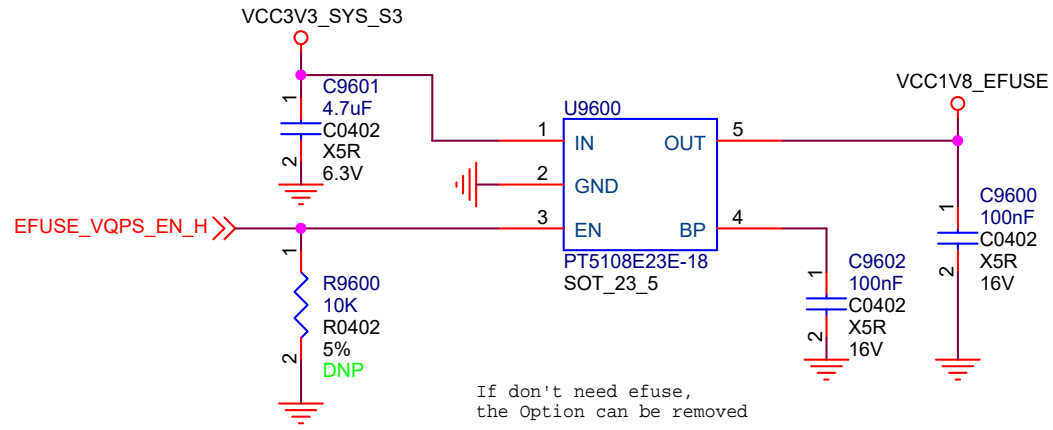
Key Name	SARADC
VOL+ /RECOVERY	10
VOL-	170
HOME	354
MENU	560
ESC	747

PCI . Express

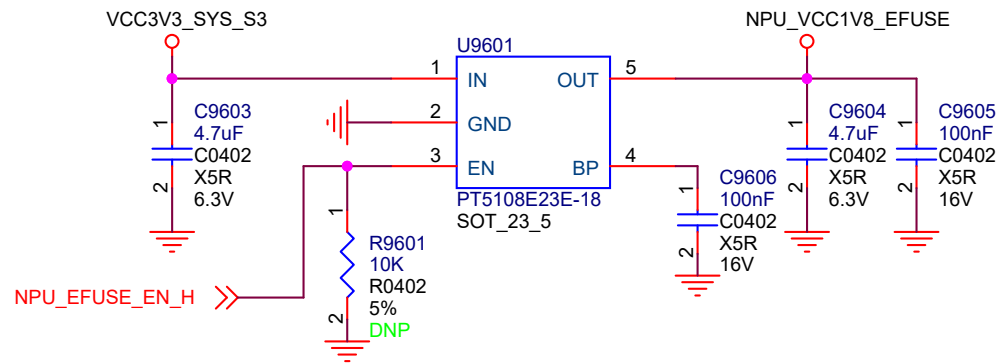


Rackchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project:	RK3399Pro LP3S178P232DD8		
File:	94.PCIE4		
Date:	Tuesday, November 20, 2018	Rev:	V1.0
Designed by:	Rzf	Sheet:	94 of 99

EFUSE POWER



NPU EFUSE POWER



Fuzhou Rockchip Electronics

Project: RK3399Pro LP3S178P232DD8

File: 96.EFUSE

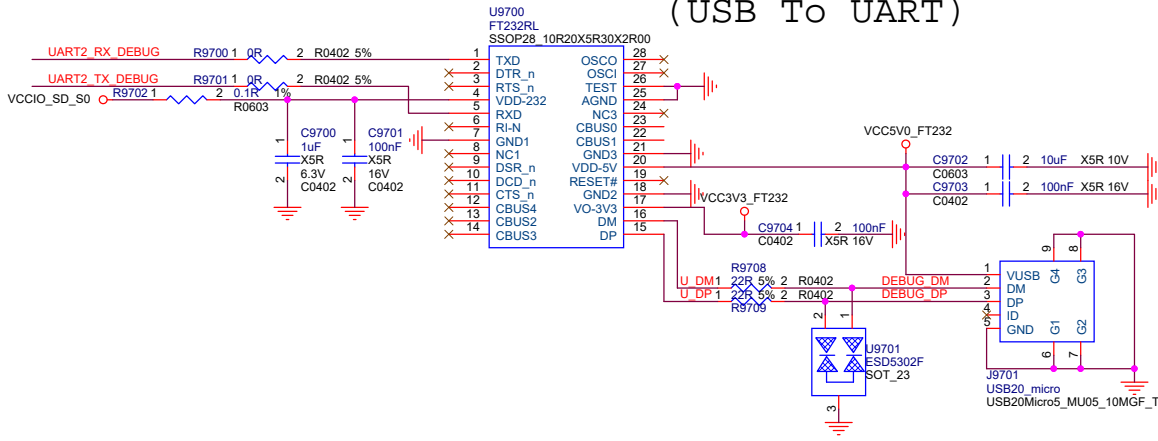
Date: Tuesday, November 20, 2018

Rev: V1.0

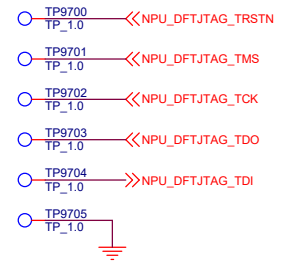
Designed by: Rzf

Sheet: 96 of 99

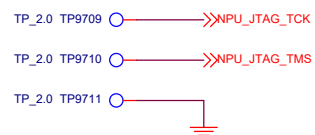
Debug UART2 (USB To UART)



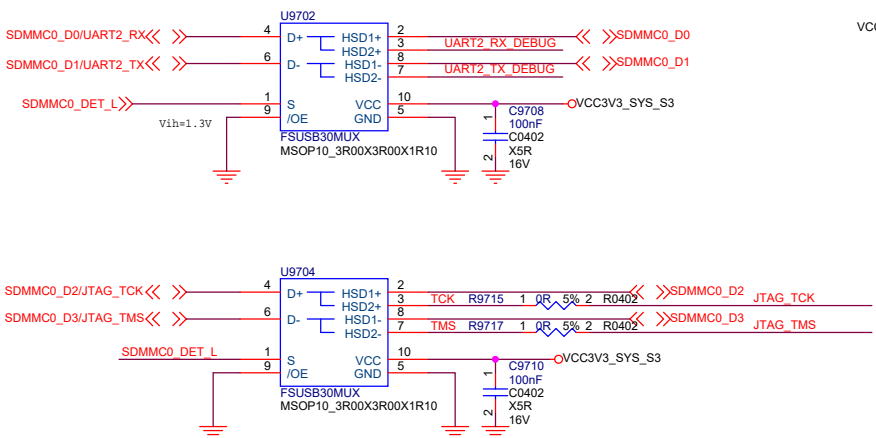
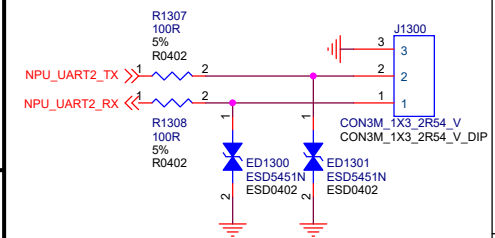
NPU DFTJTAG



NPU SWD

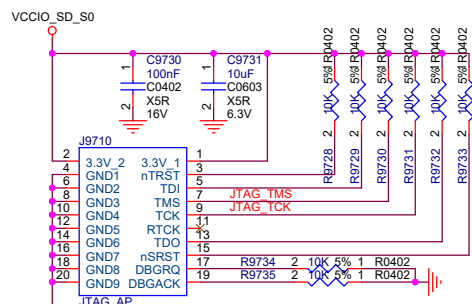


NPU UART DEBUG

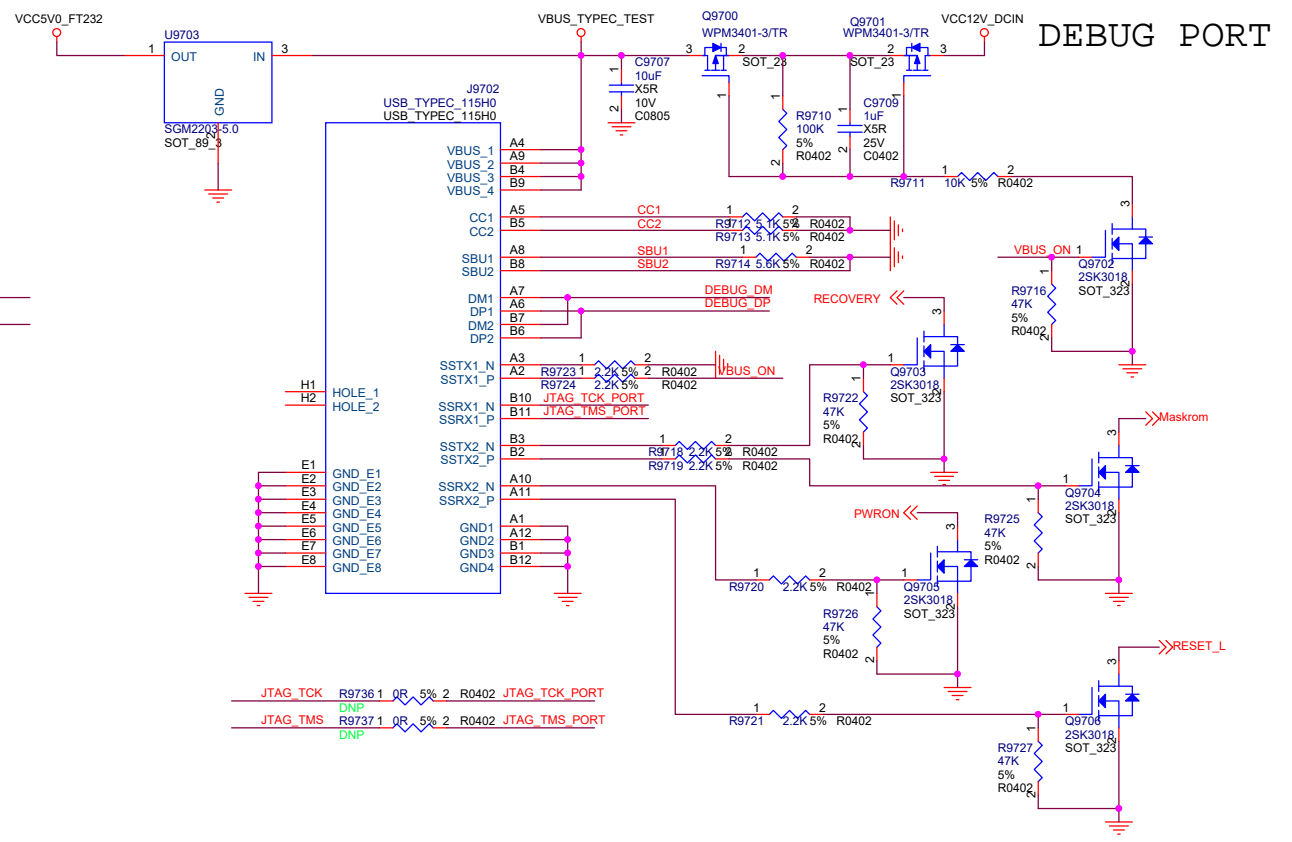


Truth Table

S	OE	Function
X	H	Disconnect
L	L	D+, D- = HSD1 _n
H	L	D+, D- = HSD2 _n



SWD



DEBUG PORT

Rockchip 福州瑞芯微电子 Fuzhou Rockchip Electronics

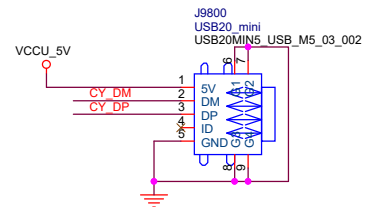
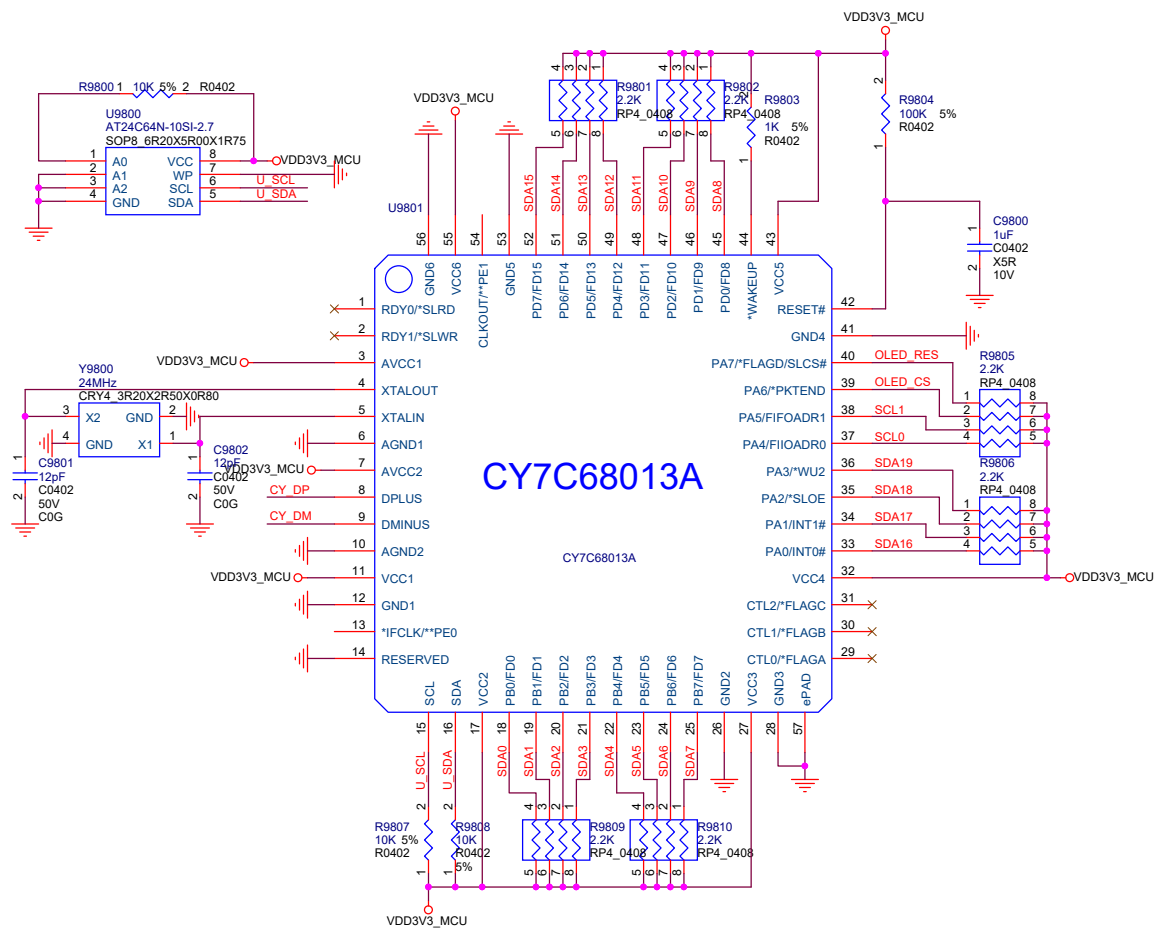
Project: RK3399Pro LP3S178P232DD8

File: 97.DEBUG

Date: Thursday, November 15, 2018 **Rev:** V1.0

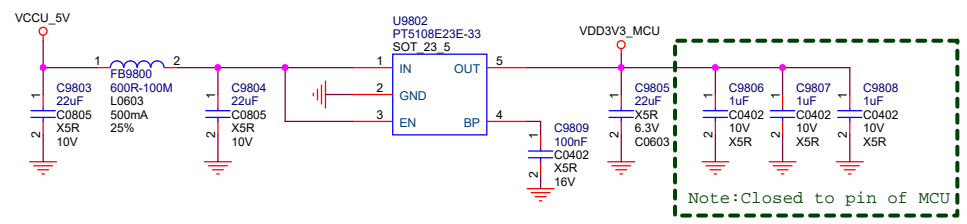
Designed by: Rzf **Sheet:** 97 of 99

Current Detection MCU



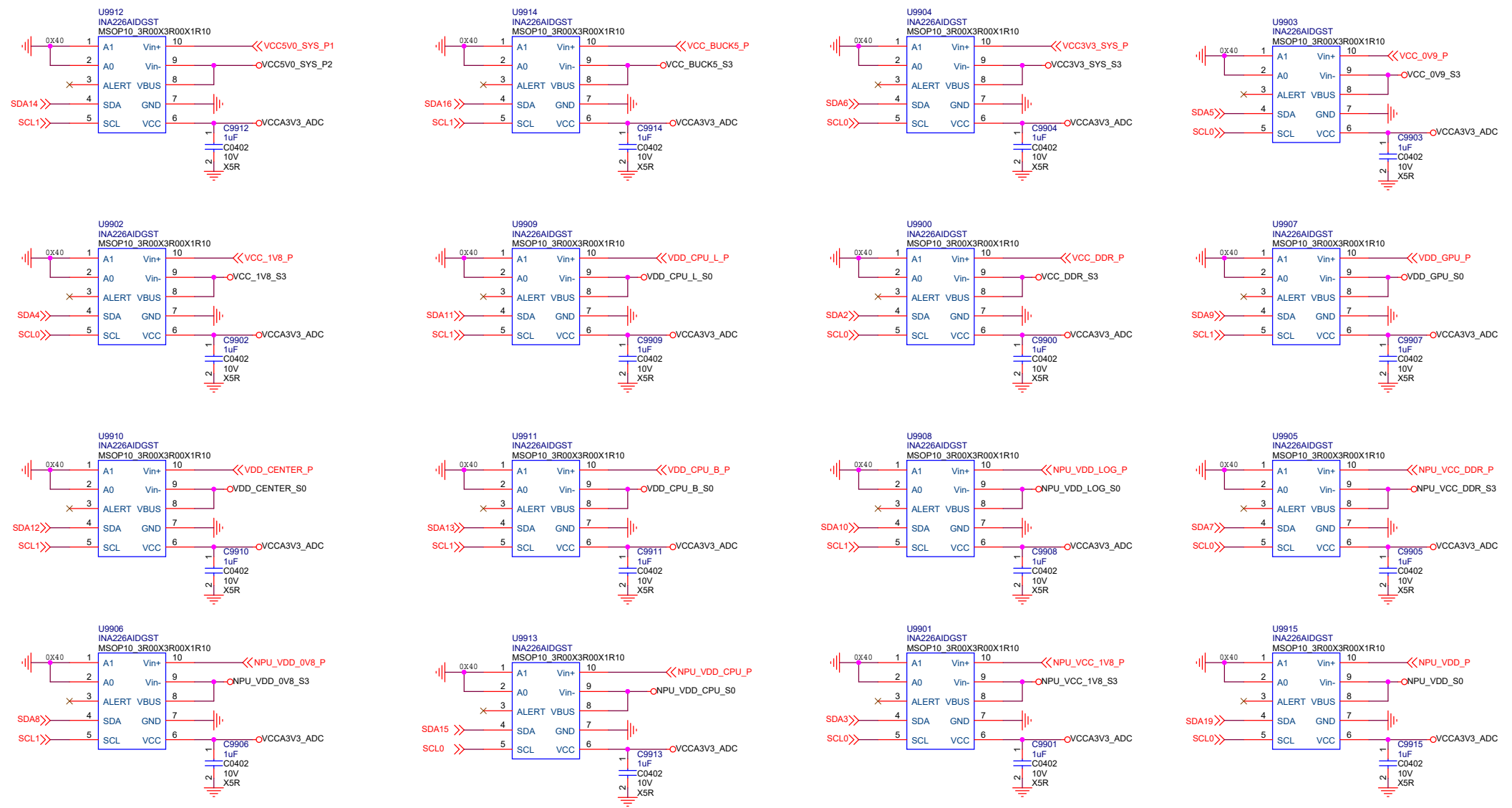
USB Port

Power

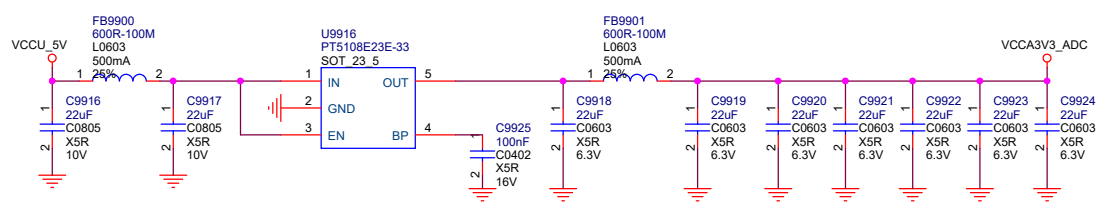


Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project: RK3399Pro LP3S178P232DD8			
File: 98.Power Test_MCU			
Date: Thursday, November 15, 2018		Rev: V1.0	
Designed by: Rzf		Sheet: 98 of 99	

ADC Array



ADC Power



Rockchip 瑞芯微电子		Fuzhou Rockchip Electronics	
Project: RK3399Pro LP3S178P232DD8			
File: 99.Power Test_INA226			
Date: Thursday, November 15, 2018		Rev: V1.0	
Designed by: Rzf		Sheet: 99 of 99	