# RK3399Pro Hardware Design Guide

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# Preface

## Overview

This document mainly describes the key points of hardware design and notices for RK3399Pro processor, aiming to help Rockchip customers shorten the product design cycle, improving the product design stability and reducing the failure rate. Please refer to the requirements of this guide to do the hardware design, and suggest to use the relevant core templates released by Rockchip. If need to modify due to specific reasons, please strictly follow the design rule of high-speed-digital-circuit and Rockchip Schematic&PCB checklist requirements.

## Chip Type

The corresponding chip type is RK3399Pro in this document.

## Intended Audience

This document is mainly suitable for below:

- Product hardware development engineers
- Field application engineers
- Test engineers

# Revision History

The revision history accumulates instructions for each update of the document and the latest version contains updates of all previous versions.

| Version | Author | Revision Date | Revision Description | Remark |
|---|---|---|---|---|
| V1.0 | Linus.Lin | 2019.03.20 | The initial version release | |
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# Acronym

Acronym includes the abbreviations of commonly used phrases in this document:

| | | |
|---|---|---|
| DDR | Double Data Rate | 双倍速率同步动态随机存储器 |
| DP | DisplayPort | 显示接口 |
| eDP | Embedded DisplayPort | 嵌入式数码音视讯传输接口 |
| eMMC | Embedded Multi Media Card | 内嵌式多媒体存储卡 |
| GPU | Graphics Processing Unit | 图形处理器 |
| HDMI | High Definition Multimedia Interface | 高清晰度多媒体接口 |
| $I^2C$ | Inter-Integrated Circuit | 内部整合电路(两线式串行通讯总线) |
| JTAG | Joint Test Action Group | 联合测试行为组织定义的一种国际标准测试协议（IEEE 1149.1兼容） |
| LDO | Low Drop Out Linear Regulator | 低压差线性稳压器 |
| MAC | Media Access Control | 以太网媒体接入控制器 |
| MIPI | Mobile Industry Processor Interface | 移动产业处理器接口 |
| NPU | Neural-network Process Units | 神经元网络处理器 |
| PMIC | Power Management IC | 电源管理芯片 |
| PMU | Power Management Unit | 电源管理单元 |
| Rockchip | Rockchip Electronics Co., Ltd. | 瑞芯微电子股份有限公司 |
| SD Card | Secure Digital Memory Card | 安全数码卡 |
| SDIO | Secure Digital Input and Output Card | 安全数字输入输出卡 |
| SDMMC | Secure Digital Multi Media Card | 安全数字多媒体存储卡 |
| SPDIF | Sony/Philips Digital Interface Format | SONY、PHILIPS数字音频接口 |
| SPI | Serial Peripheral Interface | 串行外设接口 |
| TF Card | Micro SD Card(Trans-flash Card) | 外置记忆卡 |
| Type-C | | USB3.0定义的一种接口标准 |
| USB | Universal Serial Bus | 通用串行总线 |
| VR | Virtual Reality | 虚拟现实 |
| | | |

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# 1 Introduction

## 1.1 Overview

RK3399Pro is a low power, high performance processor. Based on Big.Little architecture, it integrates dual-core Cortex-A72 and quad-core Cortex-A53 with separate NEON coprocessor.

Equipped with one powerful neural network process unit (NPU), RK3399Pro has strong AI computing ability and rich interfaces, and also has the advantages to support current mainstream deep learning frameworks (such as caffe, TensorFlow, etc.), support mainstream platforms in the market , easy to add customized layer and support INT16/FP16 and so on.

This chipset can be widely used for computing, personal mobile internet devices and other smart device applications such as industrial tablet, smart commercial display, smart pay, new retail, human face recognition and so on.

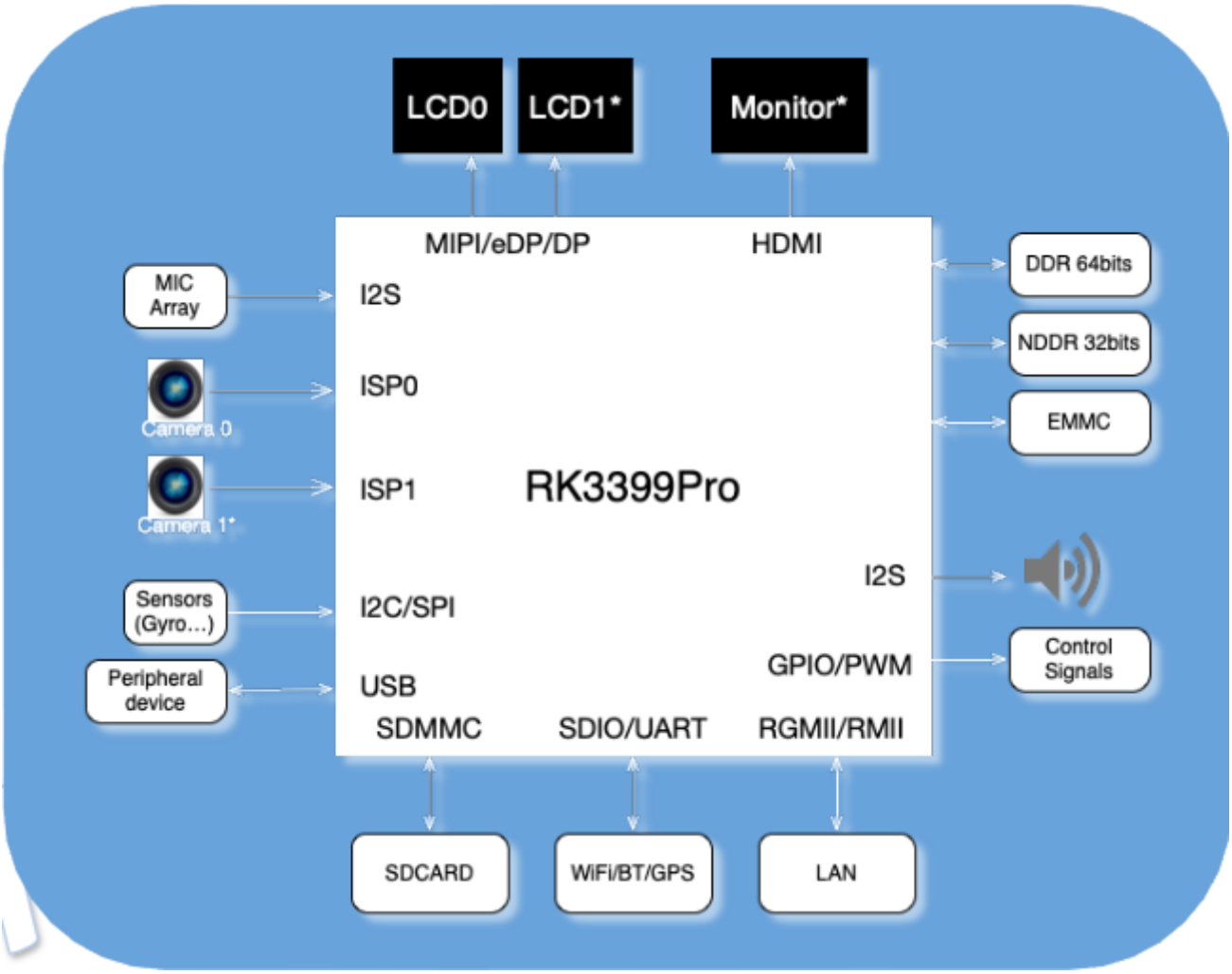



Figure 1–1 RK3399Pro side AI device solution application

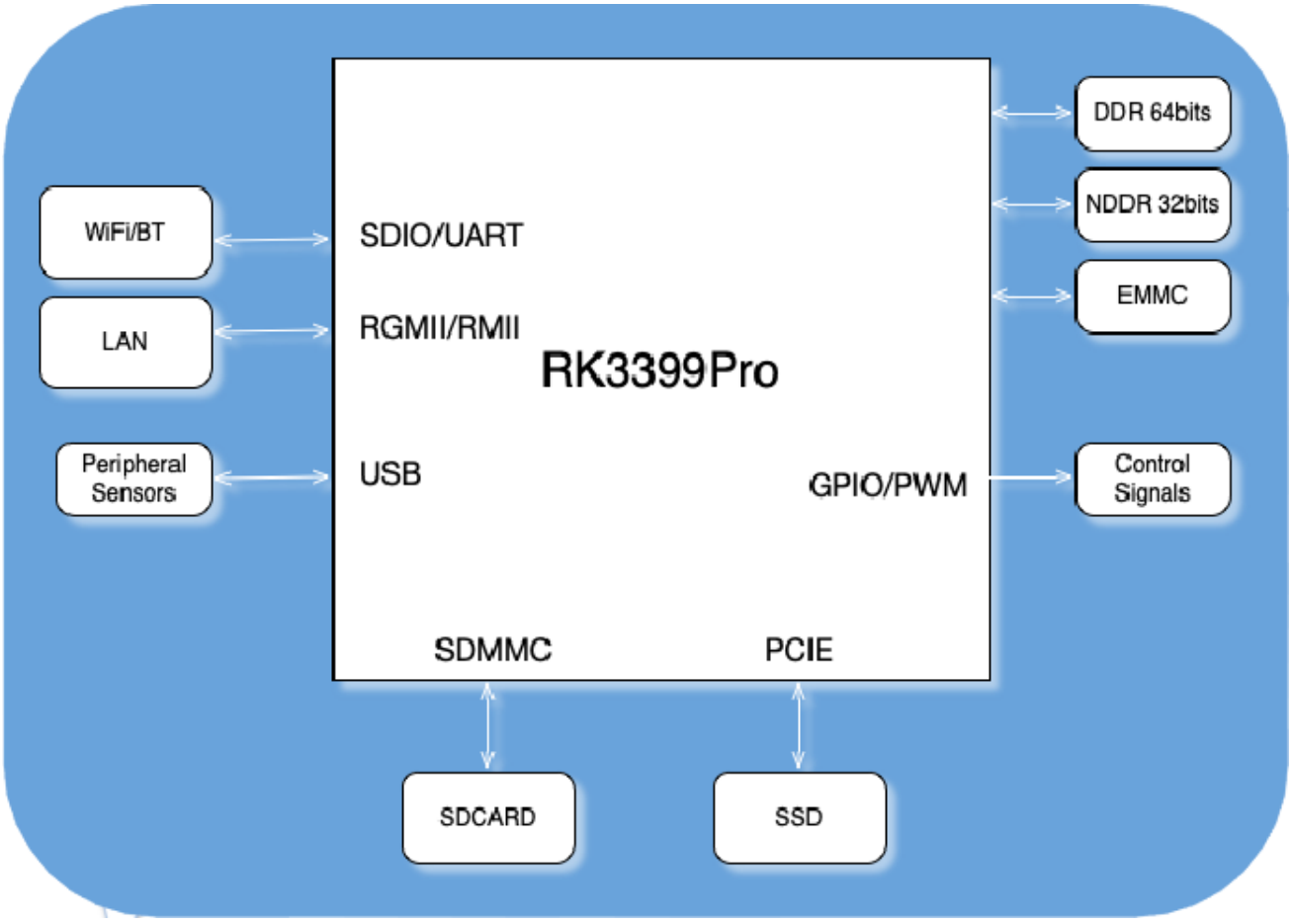



Figure 1–2 RK3399Pro side AI gateway/server solution application

RK3399Pro embedded CPU and NPU have standalone power supply, interface and logic units, so they can work separately. CPU is responsible for system operation and application, when need to do massive parallel computing, such as in deep learning scenario, NPU will join. They connect to communicate and exchange the computing data via USB interface.

Because CPU and NPU are mutually independent, RK3399Pro design recommendation is divided into two parts: CPU and NPU. Please refer to the corresponding chapters for design.

## 1.2 Block Diagram

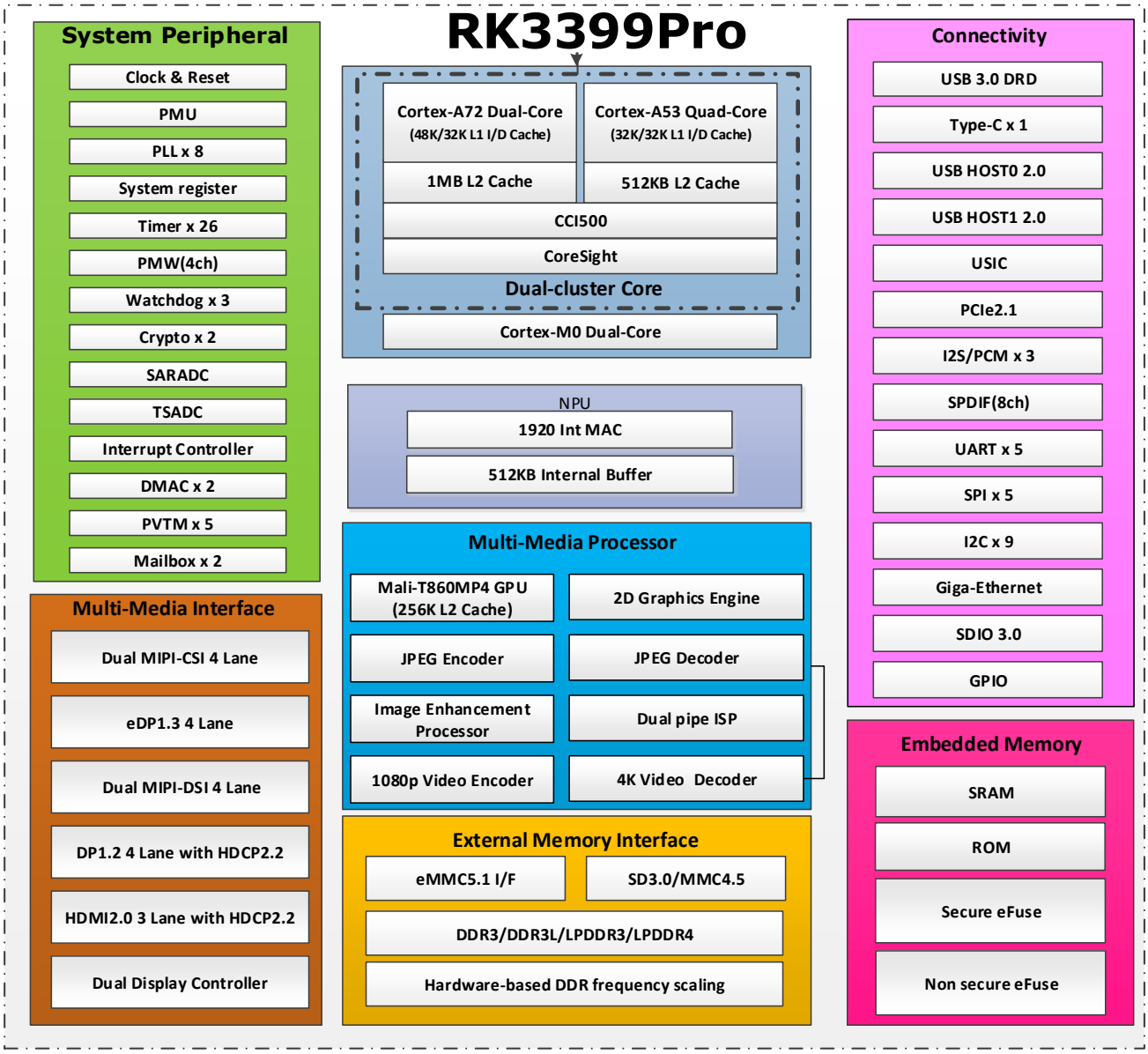



Figure 1–3 RK3399Pro Block Diagram

## 1.3 Application Block Diagram

### 1.3.1 AI BOX Application

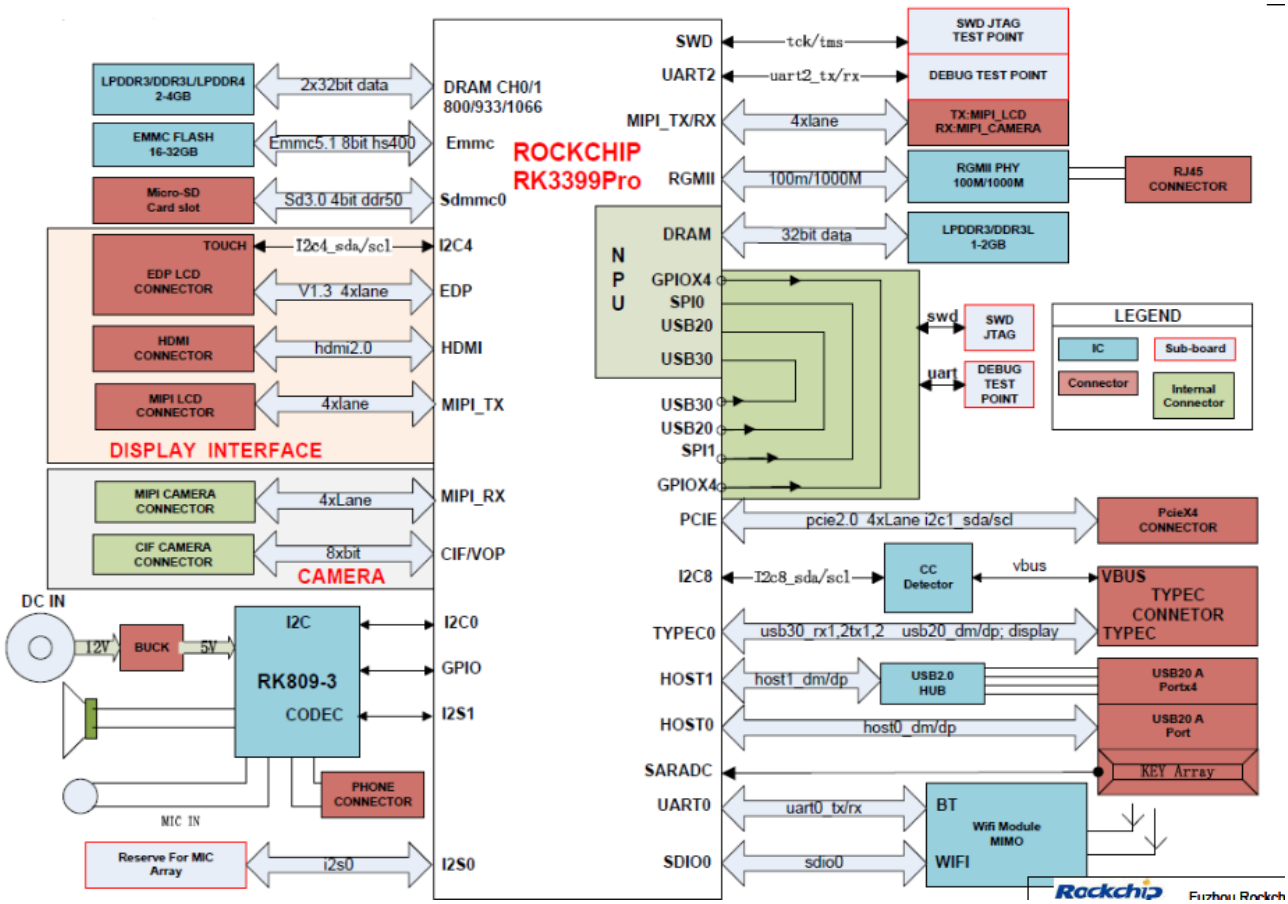



Figure 1–4 RK3399Pro AI BOX Application Block Diagram

Figure 1-4 is the application block diagram of RK3399Pro AI BOX solution. For more details please refer to the reference design schematic released by Rockchip.

# 2 CPU Schematic Design Recommendation

## 2.1 CPU Minimum System Design

### 2.1.1 CPU Clock Circuit

RK3399Pro CPU internal oscillator circuit and external 24MHz crystal constitute the internal oscillator clock source, as Figure 2-1 shows:

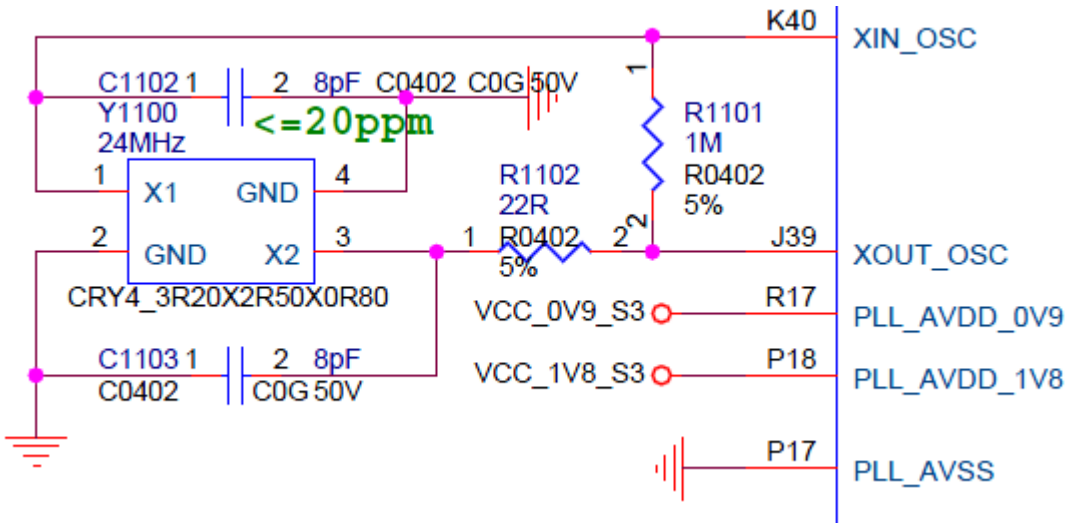



Figure 2–1 RK3399Pro CPU crystal implementation

**Note**

*The value of crystal load capacitance should be selected according to the load capacitance value of crystal. 8pF is the capacitance value of crystal used by Rockchip which may not be commonly used.*

The system clock can also be generated by digital clock source. The 0.9V compatible clock source is connected to the XIN_OSC pin.In this mode of operation, the XOUT_OSC pin is left unconnected and should not be used to source any external components:

Table 2–1 RK3399Pro CPU 24MHz digital clock source

| Parameter | Spec. | | | Description |
|---|---|---|---|---|
| | Min. | Max. | Unit | |
| Frequency | 24.000000 | | MHz | |
| Frequency Tolerance | +/-20 | | ppm | Frequency tolerance |
| Clock amplitude | 0.9 | | V | Peak-to-Peak value |
| Operating Temperature | -20 | 70 | ℃ | |
| ESR | / | 40 | Ohm | |

The internal oscillator clock source will be switched to the external 32.768 KHz clock source to reduce the system power consumption when RK3399Pro CPU is in standby mode. The signal can be acquired from PMIC or external RTC clock source. The clock input is shown as below:

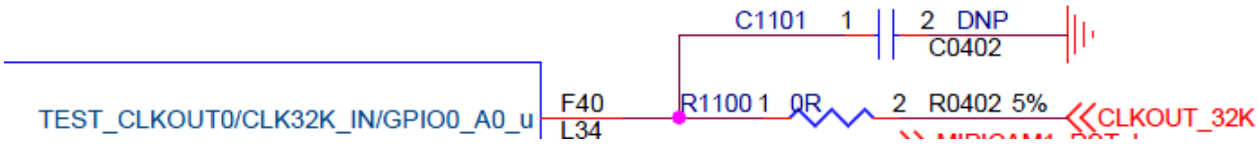



Figure 2–2 RK3399Pro CPU standby mode clock input

The 32.768KHz RTC clock parameters are shown as below table:

Table 2–2 RK3399Pro CPU 32.768KHz clock requirement

| Parameter | Spec. | | | Description |
|---|---|---|---|---|
| | Min. | Max. | Unit | |
| Frequency | 32.768000 | | kHz | |
| Frequency Tolerance | +/-30 | | ppm | Frequency tolerance |
| Clock amplitude | 1.8 | | V | Peak-to-Peak value |
| Operating temperature | -20 | 70 | ℃ | |
| Duty ratio | 50 | | % | |

### 2.1.2 CPU Reset Circuit

RK3399Pro CPU internally integrates POR (Power on Reset) circuit, low active, and the minimum pulse width time is 100 cycles of 24MHz clock (at least 4us), to ensure SoC operation stably and normally. The reset signal connects 100nF capacitor to eliminate the jitter to avoid the reset triggered mistakenly. Please place the capacitor close to the chip pin for layout.

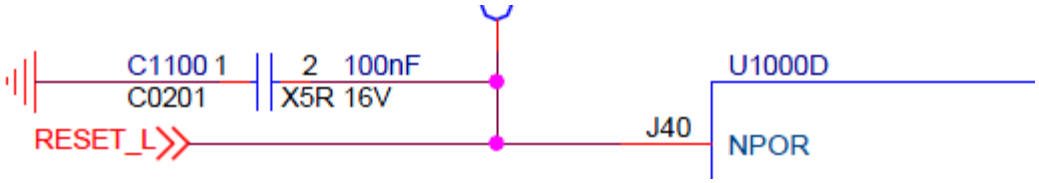



Figure 2–3 RK3399Pro Reset Input

### 2.1.3 CPU system boot sequence

RK3399Pro CPU support boot from SPI/eMMC/SDMMC, and boot priority from high to low as below:

- SPI FALSH
- eMMC FLASH
- SDMMC CARD

### 2.1.4 CPU system initialization configuration signal

RK3399Pro CPU has two important signals which need to be configured before power-on. They are the IO supply configuration pin of PMUIO2 power domain and JTAG/SDMMC function control pin.

RK3399Pro CPU PMUIO2 power domain's IO supply needs to be configured, because it belongs to PMU power domain and the signal will be used during system boots up. When system boots up, it must specify the default level mode through the hardware configuration, otherwise it cannot work normally. The pin is shown as below:

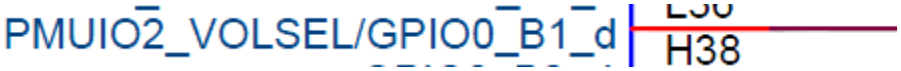



Figure 2–4 RK3399Pro PMUIO2 power domain level configuration pin

RK3399Pro CPU reuses JTAG function and SDMMC function together to reduce IO, and use

SDMMC0_DET pin to switch the output function, so it also needs to be configured before power-on, otherwise UART/JTAG without output will influence the debugging in boots up stage, while SDMMC without output will influence SDMMC boot function. The pin is shown as below:


Figure 2–5 RK3399Pro SDMMC0/JTAG reused control pin

The two pins configurations are shown in below table:

Table 2–3 RK3399Pro system initialization configuration signal description

| Name | Internl pull up/down | Description |
|---|---|---|
| PMUIO2_VOLSEL | pull down | PMUIO2 power domain IO supply configuration pin, effective only during power-on:<br>0: PMUIO2 power domain level mode is 1.8V(default).<br>1: PMUIO2 power domain level mode is 3.0V. |
| SDMMC0_DET | pull up | JTAG pin resued control pin:<br>0: recognized as sd card insertion, SDMMC/JTAG/UART pin reused as SDMMC output.<br>1: recognized as SD card not insertion, SDMMC/JTAG/UART pin reused as JTAG/UART output (default). |

### 2.1.5 CPU JTAG Debug Circuit

RK3399Pro CPU JTAG interface is compliant with IEEE1149.1 standard. PC can connect with DSTREAM emulator by SWD mode (Two-line mode) to debug A53/A72 core within the SoC. Or connect with J-link/U-link/Realview-ICE/DSTREAM emulator to debug M0 core within the SoC.

Before connecting the emulator, need to pull SDMMC0_DET pin high, otherwise it can not enter JTAG debugging mode.The JTAG interface description is shown as below table:

Table 2–4 RK3399Pro JTAG Debug interface signal

| Name | Description |
|---|---|
| APJTAG_TCK | AP JTAG clock inout, recommend to pull down |
| APJTAG_TMS | AP JTAG mode select input, recommend to pull up |
| MCUJTAG_TCK | MCU JTAG clock inout, recommend to pull down |
| MCUJTAG_TMS | MCU JTAG mode select input, recommend to pull up |
| PMCUJTAG_TCK | PMCU JTAG clock inout, recommend to pull down |
| PMCUJTAG_TMS | PMCU JTAG mode select input, recommend to pull up |

### 2.1.6 CPU DDR Circuit

- **2.1.6.1 Controller Introduction**

RK3399Pro CPU DDR controller interface supports JEDEC SDRAM standard, and has feature following:

- Support DDR3/DDR3L/LPDDR3/LPDDR4 etc. standards;
- Provide two 32bit DDR controller interfaces, each controller interface separately provides 2 chip select, 2 ODT, 2 CKE, supports data bus bit width 32bit/16bit configurable, and supports address bus up to 16 bit.
- Support DDR up to 4GB.
- Support low power consumption mode such as Power Down, Self Refresh and so on.

- **2.1.6.2 DDR topological structure and connection method**

Take LPDDR3 as an example, RK3399Pro CPU SDRAM topological structure is shown as

below:

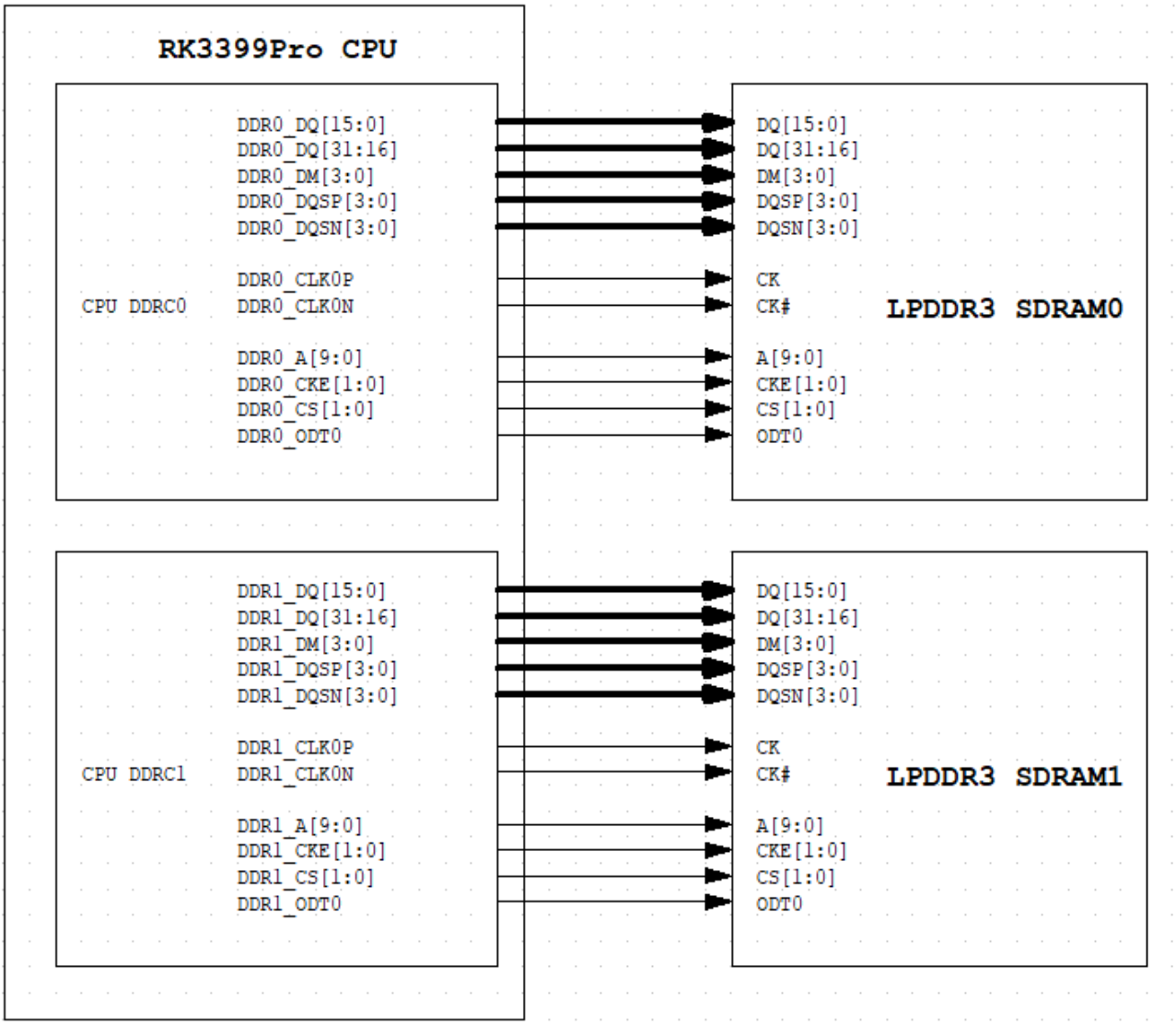



Figure 2–6 RK3399Pro LPDDR3 topological structure

- **2.1.6.3 DDR power up sequence requirement**

RK3399Pro CPU DDR controller has 3 groups of power supply:

- DDR_VDD: Supply power for Core of DDR controller, interface I/O and Buffer
- DDR_CLK_VDD: Clock power of DDR controller. It should be consistent with VCC_DDR level. Recommend to split from VCC_DDR and route separately.
- DDRPLL_AVDD_0V9: analog PLL power of DDR controller. Recommend to be supplied by LDO separately to ensure a clean clock power.

SDRAM component has two groups of power supply. The power up sequence refers to JEDEC standard:

DDR3 SDRAM power up sequence is shown as below:

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

Figure 2–7 DDR SDRAM power up sequence

LPDDR3 SDRAM power up sequence is shown as below:

| After... | Applicable Conditions |
|---|---|
| Ta is reached | $V_{DD1}$ must be greater than $V_{DD2}$—200mV |
| | $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDCA}$—200mV |
| | $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDQ}$—200mV |
| | $V_{Ref}$ must always be less than all other supply voltages |

Figure 2–8 LPDDR3 SDRAM power up sequence

LPDDR4 SDRAM power up sequence is shown as below:

| After | Applicable Conditions |
|---|---|
| Ta is reached | VDD1 must be greater than VDD2 |
| | VDD2 must be greater than VDDQ - 200mV |

NOTE 1 Ta is the point when any power supply first reaches 300mV.
NOTE 2 Voltage ramp conditions in Table 4 apply between Ta and power-off (controlled or uncontrolled).
NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.
NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
NOTE 5 The voltage difference between any of Vss and Vssq pins must not excess 100mV.

Figure 2–9 LPDDR4 SDRAM power up sequence

#### • 2.1.6.4 DDR Support List

RK3399Pro DDR interfaces DDR3/LPDDR3/LPDDR4 support operating frequency up to 800MHz. Please refer to the document 《Rockchip DDR Support List》 released by Rockchip for the components available. The document can be downloaded from redmine through below link:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

### 2.1.7 CPU eMMC Circuit

#### • 2.1.7.1 eMMC Controller Introduction

RK3399Pro eMMC interface supports eMMC 5.1 and is also compatible with 4.41, 4.51, 5.0 protocol. The controller supports the features:

- Support single channel eMMC.
- Support 1-bit, 4-bit and 8-bit mode of data bus width.
- Support eMMC 5.1 protocol, support HS400 mode

### 2.1.7.2 eMMC Topological Structure and Connection Method

Table 2–5 RK3399Pro eMMC interface design

| Name | Internal pull up/down | Connection method | Description(chip side) |
|---|---|---|---|
| eMMC_DQ[7:0] | pull up | direct connection | eMMC data output/input |
| eMMC_CLK | pull up | Series connect 22ohm resistor | eMMC clock output |
| eMMC_CMD | pull up | direct connection | eMMC command output/input |
| eMMC_STRB | pull down | Series connect 22ohm resistor | HS400 mode, eMMC strobe clock input<br>Configure internal pull down through software, no need external pull down resistor. |

### 2.1.7.3 eMMC power up sequence requirement

RK3399Pro eMMC controller has two groups of power supply:

- VCC0V9_EMMC:Core power of eMMC controller
- VCC1V8_EMMC:I/O power of eMMC controller

The power up sequence of RK3399Pro eMMC controller power refers to below:

- VCC0V9_EMMC and VCC1V8_EMMC can be power-on at the same time, however, recommend to power-up low level power first for the power ESD structure, that is, VCC0V9_EMMC should be power-on earlier than VCC1V8_EMMC.

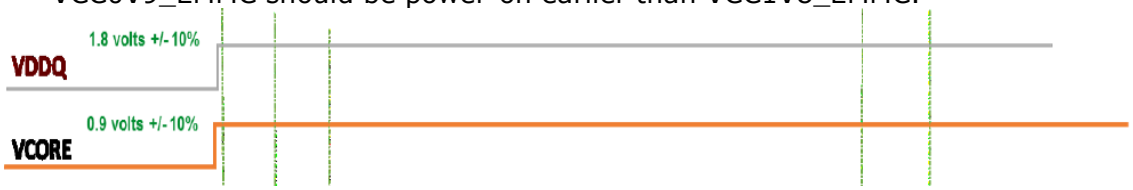



Figure 2–10 RK3399Pro eMMC controller power up sequence

eMMC component has two groups of power supply. The power up sequence refers to JEDEC standard:

- VCC and VCCQ has no required sequence in power-on
- VCC and VCCQ must be powered up before RK3399Pro CMD command is sent out, and the power supply must work stably.
- RK3399Pro can power VCC off to reduce the power consumption in sleep mode;
- VCC power must be powered up and work stably before the component is wakened from sleep mode.

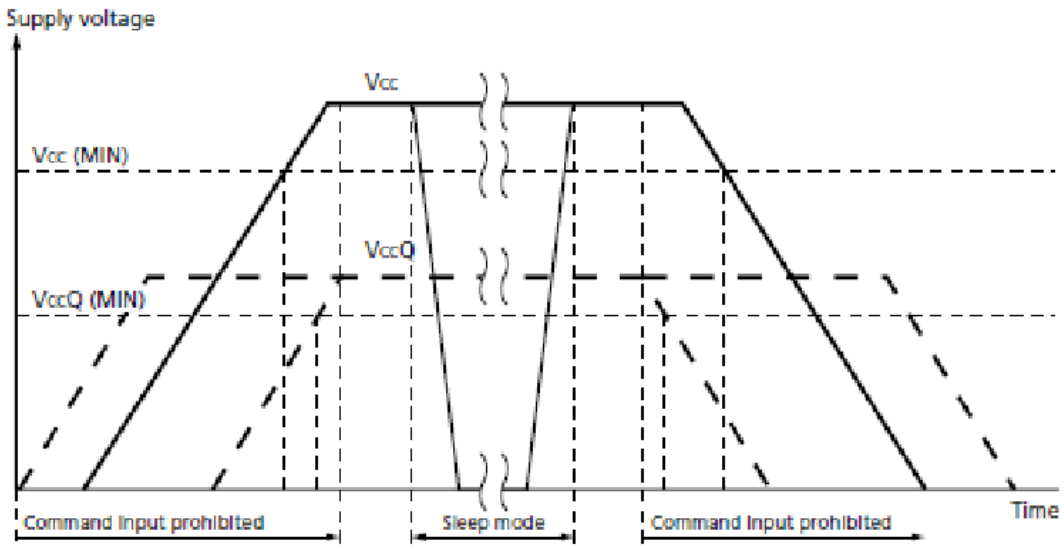



Figure 2–11 eMMC component power up/down sequence

- **2.1.7.4 eMMC Support List**

RK3399Pro eMMC support list please refer to 《RK eMMCSupportList》 released by Rockchip. The document can be downloaded from redmine through below link:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

### 2.1.8 CPU SPI Circuit

- **2.1.8.1 SPI Controller Introduction**

RK3399Pro CPU has 6 SPI controllers which can be used to connect SPI devices. SPI1 is used as boot. In Netbook applications, use SPI Flash to save Bios code and boots up the system. Because Spi Boot has the highest priority, if it is not Netbook application, please do not connect memory device to SPI1 controller otherwise it may cause system boot abnormality.

- **2.1.8.2 SPI Topological Structure and Connection Method**

Table 2–6 RK3399Pro SPI Interface Design

| Name | Internal pull up/down | Connection method | Description(chip side) |
|---|---|---|---|
| SPI1_TXD （MOSI） | pull up | Direct connection | SPI data output |
| SPI1_RXD （MISO） | pull up | Direct connection | SPI data input |
| SPI1_CLK | pull up | Series connect 22ohm resistor | SPI clock output |
| SPI1_CSn0 | pull up | Direct connection | SPI chip select signal |

- **2.1.8.3 SPI Power Up Sequence Requirement**

SPI controller power up sequence should follow the power up sequence requirement of

GPIO power domain.

SPI Flash component only has one power, so there is no requirement on power up sequence.

### 2.1.9 CPU GPIO Circuit

RK3399Pro CPU has 5 GPIO types:

- 1.8V only, fixed 1.8V.
- 3.3V only, fixed 3.3V.
- 1.8V/3.0V, configurable 1.8V or 3.0V.
- 1.8V/3.0V auto, able to automatically configure 1.8V or 3.0V

#### 2.1.9.1 GPIO Driving Capability

RK3399Pro CPU provides different driving capability and operating frequency ranges according to different GPIOs types.

Table 2–7 RK3399Pro GPIO driving capability

| Power domain | GPIO type | I/O frequency @1.8V | I/O frequency @3.xV | Supported driving capability type |
|---|---|---|---|---|
| PMUIO1 | 1.8V only | 150MHz | N/A | 5mA,10mA,15mA,20mA |
| APIO3 | 1.8V only | 150MHz | N/A | 5mA,10mA,15mA,20mA |
| APIO1 | 3.3V only | N/A | 125MHz | 4mA,7mA,10mA,13mA,16mA,19mA,22mA,26mA |
| PMUIO2 | 1.8V/3.0V | 150MHz | 50MHz | 3mA,6mA,9mA,12mA |
| APIO2 | 1.8V/3.0V | 150MHz | 50MHz | 3mA,6mA,9mA,12mA |
| APIO4 | 1.8V/3.0V | 150MHz | 50MHz | 3mA,6mA,9mA,12mA |
| APIO5 | 1.8V/3.0V | 150MHz | 50MHz | 3mA,6mA,9mA,12mA |
| SDMMC0 | 1.8V/3.0V auto | 150MHz | 50MHz | 4mA,6mA,8mA,10mA,12mA,14mA,16mA,18mA |

The default driving strength of the following two types GPIO is level 2:

- Function for Boot, such as spi1, sdmmc0:
  Pin F37:GPIO1_A7/SPI1_RXD/UART4_RX;
  Pin B39:GPIO1_B0/SPI1_TXD/UART4_TX;
  Pin G36:GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK;
  Pin H35:GPIO1_B2/SPI1_CSn0/PMCU_JTAG_TMS;
  Pin P32: GPIO4_B0/SDMMC0_D0/UART2A_RX;
  Pin P31: GPIO4_B1/SDMMC0_D1/UART2A_TX;
  Pin M34: GPIO4_B2/SDMMC0_D2/APJTAG_TCK;
  Pin H39: GPIO4_B3/SDMMC0_D3/APJTAG_TMS;
  Pin G40: GPIO4_B4/SDMMC0_CLKOUT/MCUJTAG_TCK;
  Pin H40: GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS;
- Function for debugging, such as jtag:
  Pin J32:GPIO1_C6/TCPD_VBUS_SOURCE0;
  Pin K32:GPIO1_C7/TCPD_VBUS_SOURCE1;
  Pin D36:GPIO1_D0/TCPD_VBUS_SOURCE2;

Except the above two types of GPIO, the driving strength of all the other type GPIO is level 1. Please adjust through software according to the actual requirements.

#### 2.1.9.2 GPIO Power

The power pin of GPIO power domain is described as below:

Table 2–8 RK3399Pro GPIO power pin description

| Power domain | GPIO type | Pin name | Description |
|---|---|---|---|
| PMUIO1 | 1.8V only | PMUIO1_VDD_1V8 | 1.8V power for this domain (group of) GPIO. |

| | | | |
|---|---|---|---|
| APIO3 | 1.8V only | APIO3_VDD_1V8 | 1.8V power for this domain (group of) GPIO. |
| APIO1 | 3.3V only | APIO1_VDD | 3.3V power for this domain (group of) GPIO. |
| | | APIO1_VDDPST | 1.8V Post drive. |
| PMUIO2 | 1.8V/3.0V | PMUIO2_VDD | 1.8V or 3.0V power for this domain (group of) GPIO. |
| | | PMUIO2_VDDPST | 1.8V or 1.5V post drive for this domain (group of) GPIO. |
| APIO2 | 1.8V/3.0V | APIO2_VDD | 1.8V or 3.0V power for this domain (group of) GPIO. |
| | | APIO2_VDDPST | 1.8V or 1.5V post drive for this domain (group of) GPIO. |
| APIO4 | 1.8V/3.0V | APIO4_VDD | 1.8V or 3.0V power for this domain (group of) GPIO. |
| | | APIO4_VDDPST | 1.8V or 1.5V post drive for this domain (group of) GPIO. |
| APIO5 | 1.8V/3.0V | APIO5_VDD | 1.8V or 3.0V power for this domain (group of) GPIO. |
| | | APIO5_VDDPST | 1.8V or 1.5V post drive for this domain (group of) GPIO. |
| SDMMC0 | 1.8V/3.0V auto | SDMMC0_VDD | 1.8V or 3.0V power for this domain (group of) GPIO. |
| | | SDMMC0_VDDPST | Internal post drive for this domain (group of) GPIO. |

For different applications, please follow the power rules as below:

- **1.8V only(PMUIO1 and APIO3 power domain)**

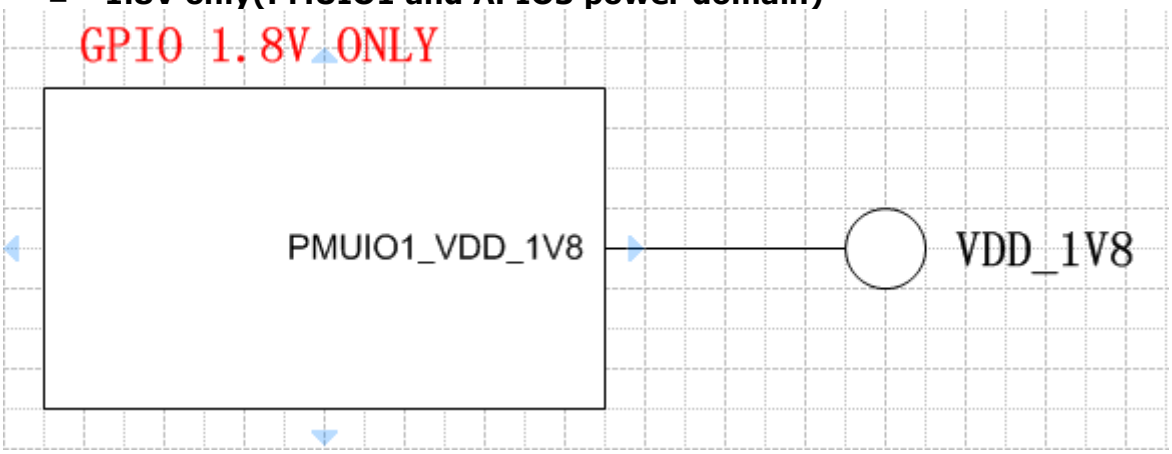



Figure 2–12 RK3399Pro GPIO 1.8V only power setting

- **3.3V only(APIO1 power domain)**

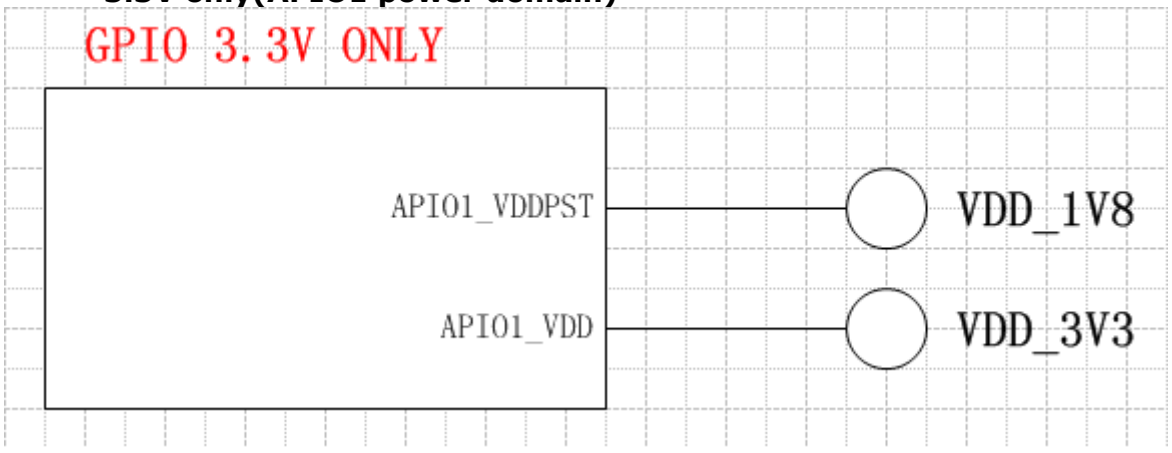



Figure 2–13 RK3399Pro GPIO 3.3V only power setting

- **1.8V/3.0V at 1.8V mode(PMUIO2, APIO2, APIO4 and APIO5 power**

domain)

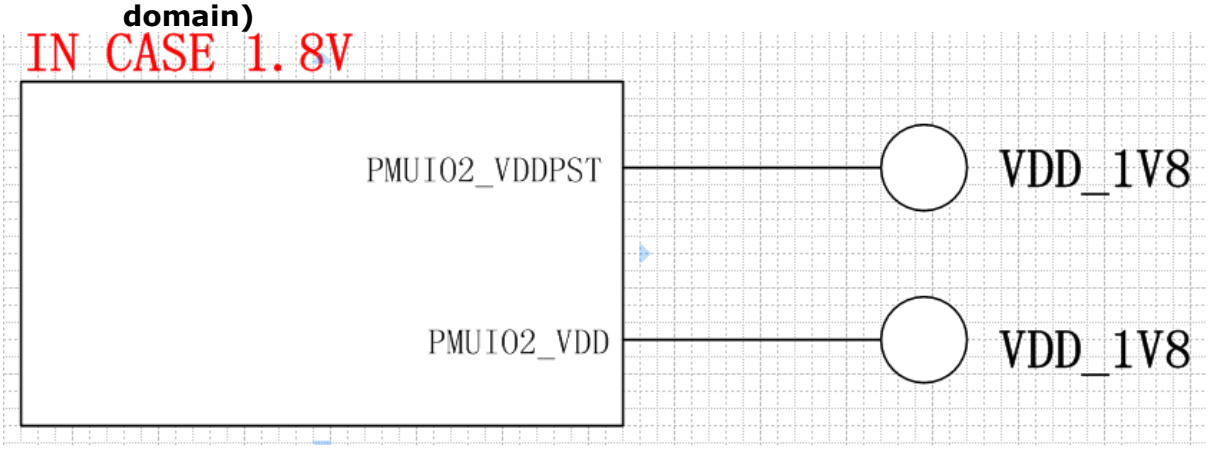



Figure 2–14 RK3399Pro GPIO 1.8V/3.0V power setting - 1.8V mode

- **1.8V/3.0V at 3.0V mode(PMUIO2, APIO2, APIO4 and APIO5 power domain)**

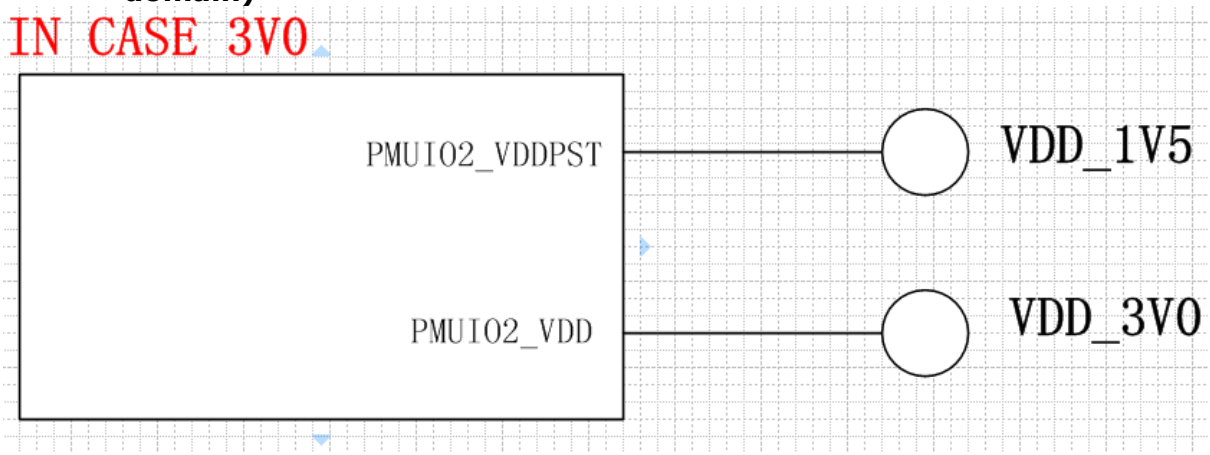



Figure 2–15 RK3399Pro GPIO 1.8V/3.0V power setting – 3.0V mode

- **1.8V/3.0V auto (SDMMC0 power domain)**

TF card side should always be supplied 3.0V, and RK3399Pro side TF card interface VDD default level is 3.0V. When the TF card is inserted, the communication between SDMMC0 data and IO signal is based on 3.0V VDD level. After communicate negotiation, if the TF card is a SD3.0, which can support USH-I high speed protocol, RK3399Pro will adjust the TF card interface VDD level to be 1.8V through adjusting the PMIC output.

RK3399Pro built-in VDDPST generation circuit is shown as below. There are a LDO and an electronic switch inside the SDMMC. When the SDMMC works in 3.0V mode, LDO works and generates a 1.5V for VDDPST, but the electronic switch doesn't work. When the SDMMC works in 1.8V mode, LDO doesn't work, and the 1.8V required for VDDPST is provided by the electronic switch of SDMMC0_VDD.

The selection between LDO and the electronic switch is controlled automatically by RK3399Pro. Hardware only needs to connect an external 1uF decoupling capacitor to SDMMC0_VDDPST.

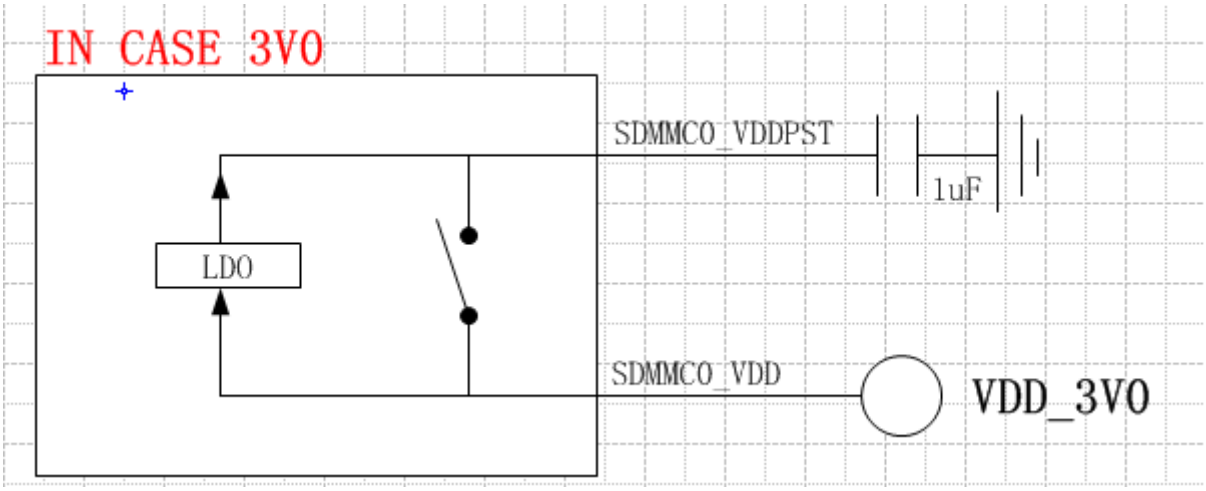



Figure 2–16 RK3399Pro GPIO 1.8V/3.0V auto power setting – 3.0V mode

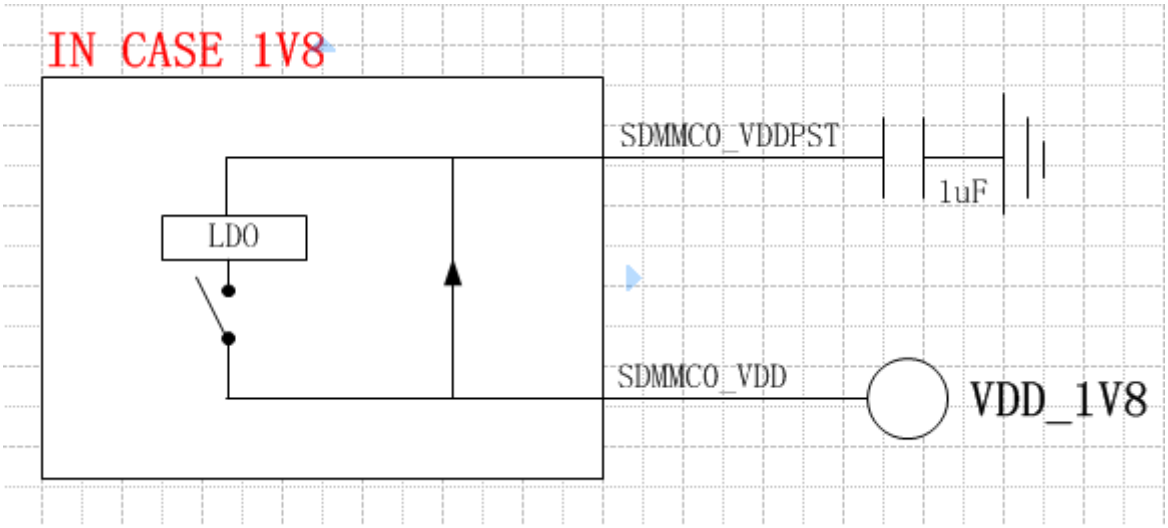



Figure 2–17 RK3399Pro GPIO 1.8V/3.0V auto power setting – 1.8V mode

# 2.2 CPU Power Design

## 2.2.1 CPU Minimum System Power Introduction

- **2.2.1.1 Power Requirement**
  - PLL:PLL_AVDD_0V9、PLL_AVDD_1V8、PMU_VDD_0V9、PMU_VDD_1V8、DDRxPLL_AVDD_0V9
  - CPU:VDD_CPU_L、VDD_CPU_B
  - GPU:VDD_GPU
  - LOGIC:VDD_LOG、VDD_CENTER
  - DDR: VCC_DDR、VCC_DDRC
  - GPIO:PMUIO1_VDD_1V8

- **2.2.1.2 Power up Sequence**

Theoretically follow the rule to power up the low voltage earlier than the high voltage in the same IP and the same voltage in one IP could be powered up at the same time. There is no sequence requirement between different IPs.

Recommended power up sequence refers to below:

VDD_LOG--->VDD_CENTER--->PLL_AVDD_0V9&PMU_VDD_0V9--->PLL_AVDD_1V8&PMU_VDD_1V8&PMUIO1_VDD_1V8--->VCC_DDR&VCC_DDRC--->VDD_GPU&VCC_CPU_B--->VCC_CPU_L

## 2.2.2 CPU Power Design Recommendation

- **2.2.2.1 Standby Circuit Solution**

RK3399Pro board level system uses the standby solution and the system consists of constant power supply area and power-off in standby area which supply power independently as shown below:

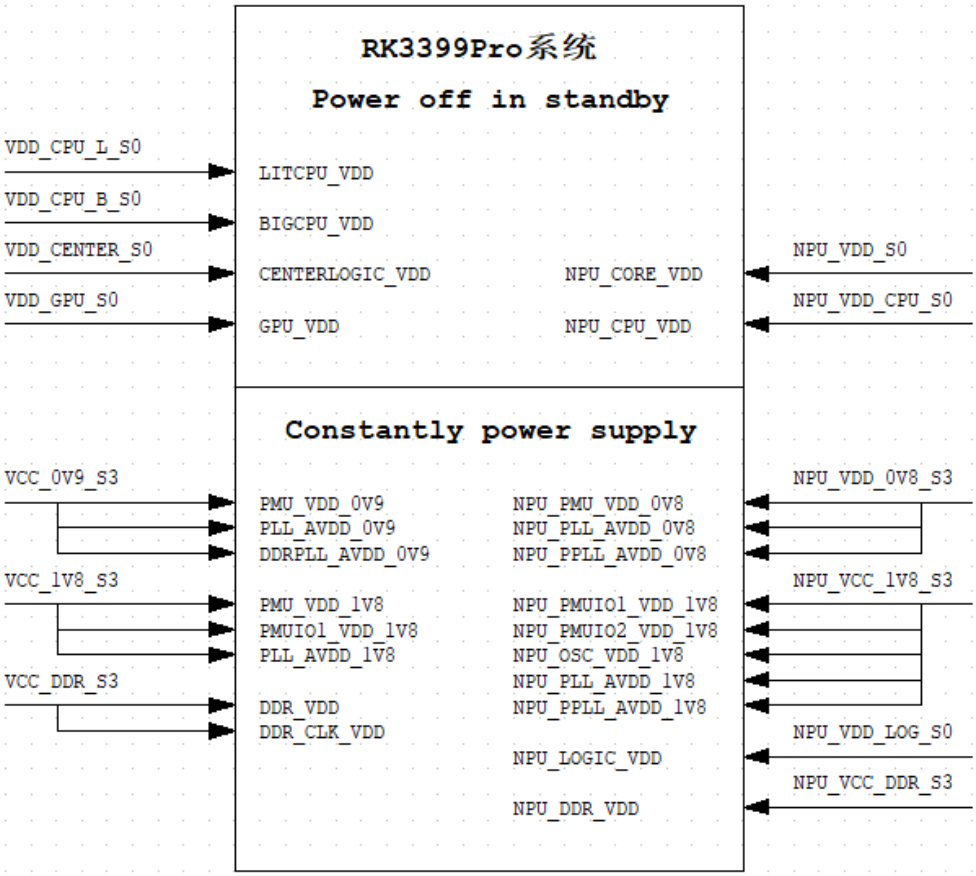



Figure 2–18 RK3399Pro Standby Circuit Solution

The power of the power-off in standby area is controlled by PMIC to turn off each independent power supply and PMIC_SLEEP_H is used to control other powers to turn off the power supply in standby mode.

The power of the constant power supply area is directly provided by the power chip and at least the following 4 groups of power must be always on in standby.

- DDR:VCC_DDR、DDR_CLK_VDD, power for DDR self-refresh
- GPIO:PMUIO1_VDD_1V8, provide IO power for PMUIO1 power domain to maintain output status and interrupt response.
- LOGIC: PMU_VDD_0V9, provide power for PLL of PMUIO1 power domain to work
- PLL:DDRPLL_AVDD_0V9, PLL_AVDD_0V9, PLL_AVDD_1V8, PMU_VDD_1V8, provide power for PLL of PMUIO1 power domain and CPU OSC to work

### 2.2.2.2 PLL Power

RK3399Pro has 10 PLL in CPU as allocated below:

Table 2–9 RK3399Pro Internal PLL Introduction

| | Quantity | Power | status in Standby |
|---|---|---|---|
| PMU/OSC | 1 | PMU_VDD_0V9、PMU_VDD_1V8 | Cannot turn off the power supply |
| DDR controller | 2 | DDR0PLL_AVDD_0V9、DDR1PLL_AVDD_0V9 | Can turn off the power supply |
| Modules inside SoC | 7 | PLL_AVDD_0V9,PLL_AVDD_1V8 | Can turn off the power supply |

Recommend to use a LDO as a separate power supply for PLL, especially when DDR operating frequency is relatively high, the stable PLL power is helpful for improving the stability. The decoupling capacitor should be placed close to the pin.

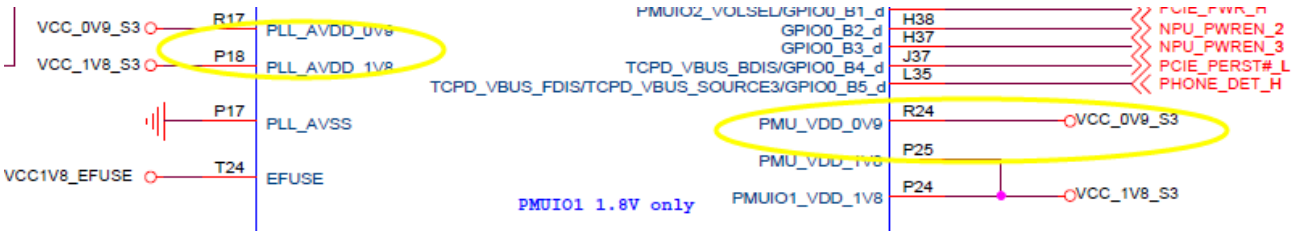



Figure 2–19 RK3399Pro PLL Power

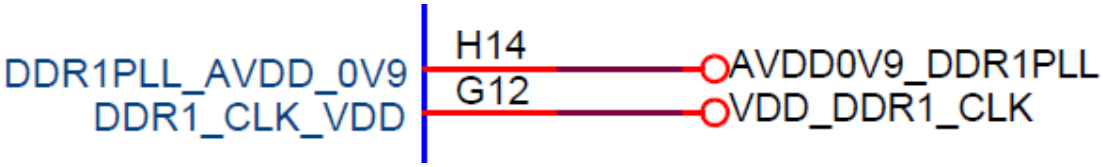



Figure 2–20 RK3399Pro DDR PLL Power

### 2.2.2.3 CPU Power

RK3399Pro uses independent power domains to supply power for CPU and CORE, VDD_CPU_B_S0 supplies power for big core A72, and VDD_CPU_L_S0 supplies power for little core A53. Both of them support DVFS (Dynamic Voltage Frequency Scaling) function. Use two separate DC-DC power supply and the peak current could be up to 4.3A/1.6A, so please do not reduce or delete the capacitors as required in RK3399Pro reference design schematic. For layout, the high- capacity capacitors should be placed on the back of RK3399Pro chip (or close to the chip) to ensure that the power ripple is controlled within 100mV to avoid the power ripple abnormality with high load. The capacitor is shown as below:

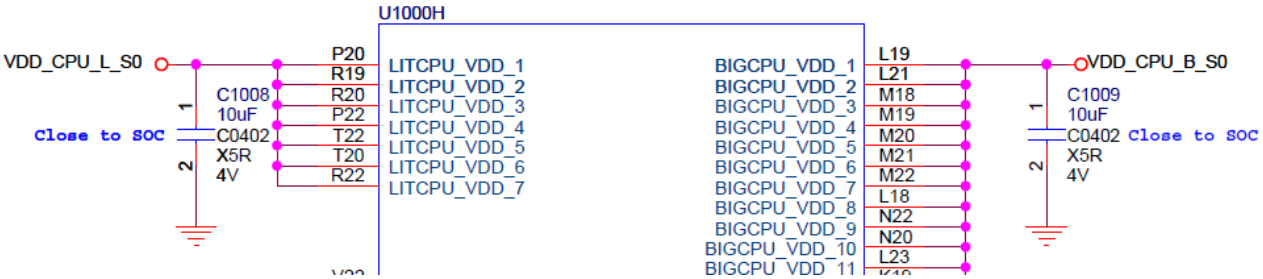



Figure 2–21 RK3399Pro VDD_CPU Power

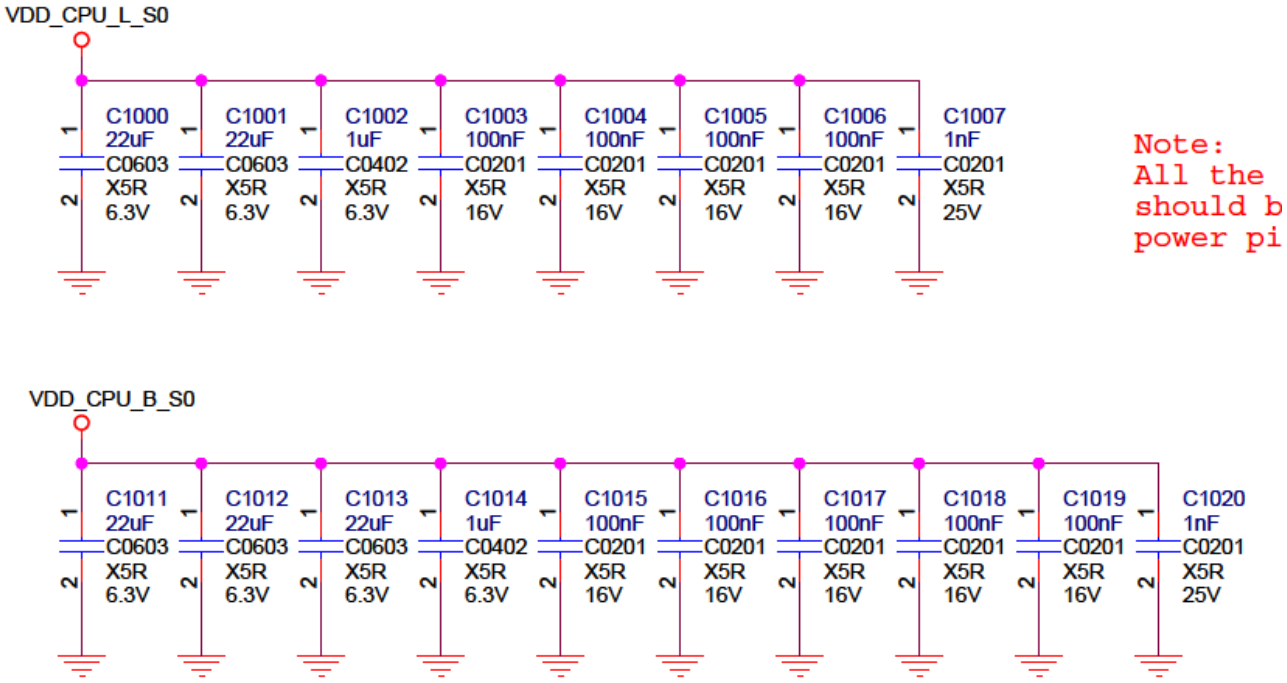



Figure 2–22 RK3399Pro VDD_CPU Power Decoupling

BIGCPU_VDD_COM is VDD_CPU_B power feedback pin of RK3399Pro, and it should be connected to FB side of DC-DC power, which can compensate the loss of PCB power traces impedance and improve the real-time of dynamic adjustment power supply.

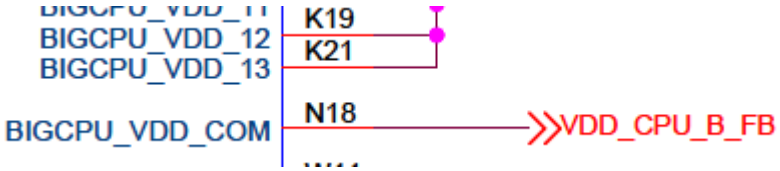



Figure 2–23 RK3399Pro VDD_CPU_COM Power Feedback

- **2.2.2.4 GPU Power**

RK3399Pro uses DC-DC to supply power separately for GPU, supports DVFS (Dynamic Voltage Frequency Scaling) function and the peak current could be up to 4A, so please do not reduce or delete the capacitors required in RK3399Pro reference design schematic. For layout, the high-capacity capacitors should be placed on the back of RK3399Pro chip (or close to the chip) to ensure that the power ripple is controlled within 100mV to avoid the power ripple abnormality with high load. The capacitor is shown as below:

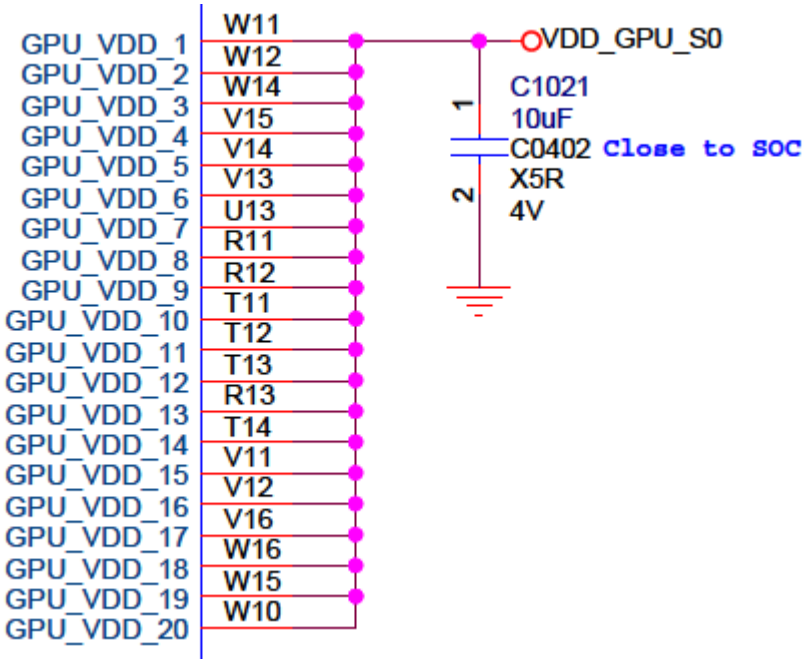



Figure 2–24 RK3399Pro VDD_GPU Power

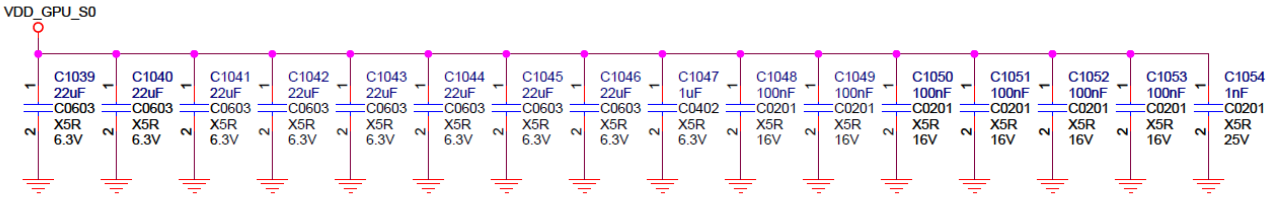



Figure 2–25 RK3399Pro VDD_GPU Power Decoupling

GPU_VDD_COM is GPU_VDD power feedback pin of RK3399Pro, and it should be connected to FB side of DC-DC power, which can compensate the loss of PCB power traces impendance and improve the real-time of dynamic adjustment power supply.

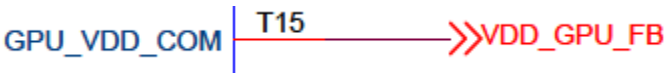



Figure 2–26 RK3399Pro VDD_GPU_COM Power Feedback

- **3.2.2.5 LOGIC Power**

The power of RK3399Pro GPU digital logic parts is supplied separately by VDD_LOGIC and VDD_CENTERLOGIC the two power domains. The power domains include the following logic sections:

| | | |
|---|---|---|
| VD_LOGIC | PD_ALIVE | CRU, PLL, GRF, TIMER, WDT, GPIO, INTR_ARB |
| | PD_PERI_LP | NOC, EFUSE, SRAM, ROM, CRYPTO, GIC, DMAC, DCF, I2S_8CH, SPDIF, UART, I2C, MAILBOX, SPI, SARADC, TSADC, Cortex-M0 |
| | PD_PERI_HP | USB2, SD/MMC, SDIO, PCIe |
| | PD_EMMC | eMMC |
| | PD_GMAC | GMAC |
| | PD_USB3 | USB3.0/2.0 |
| | PD_EDP | eDP |
| | PD_VIO | MIPI |
| | PD_ISP0 | ISP0 |
| | PD_ISP1 | ISP1 |
| | PD_VOPB | VOP_BIG |
| | PD_VOPL | VOP_LIT |
| | PD_HDCP | HDCP2.2, HDMI, DP, Gasket |
| VD_CENTER | PD_CENTER | DDRC, Memory Scheduler, DFI_MONITOR, CIC |
| | PD_VDU | RKDEC |
| | PD_VCODEC | VCODEC |
| | PD_IEP | IEP |
| | PD_RGA | RGA |

Figure 2–27 RK3399Pro Digital Logic Introduction

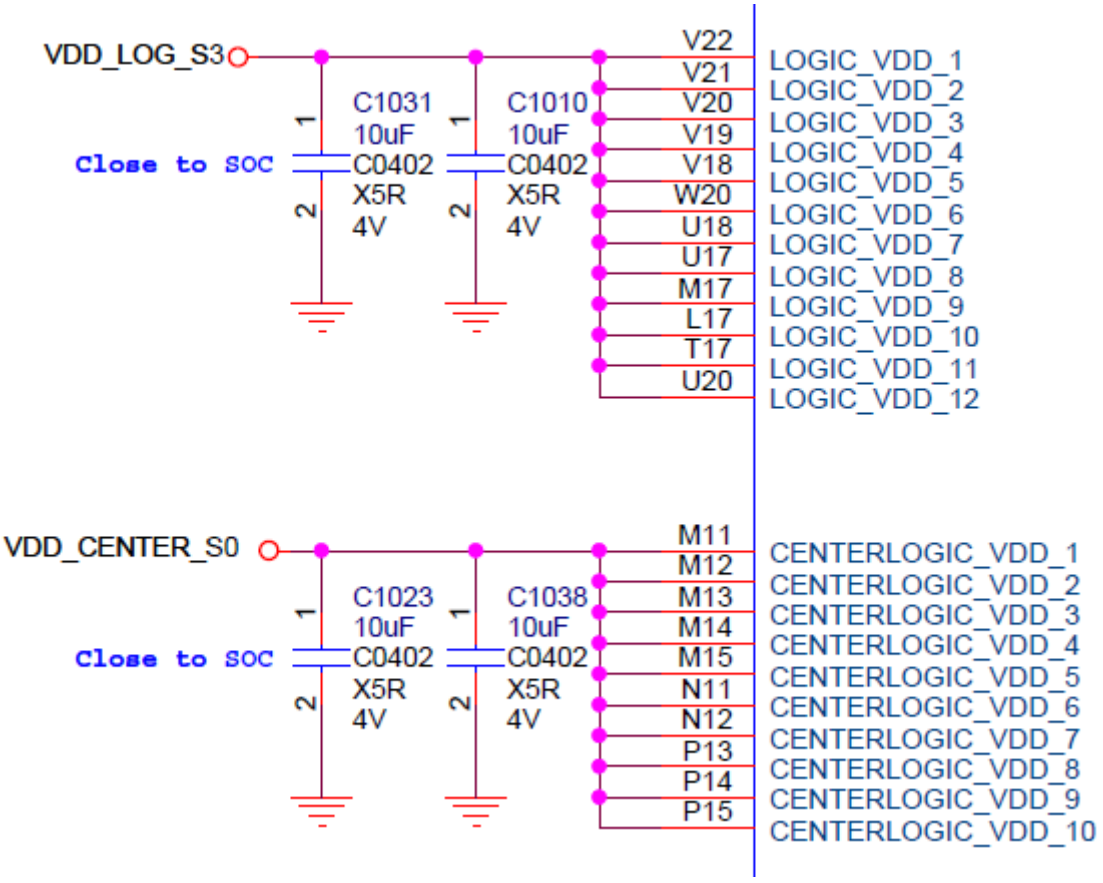



Figure 2–28 RK3399Pro Logic Power

VDD_LOG_S3 uses fixed 0.9V level, so use DC-DC to directly supply power as shown below:

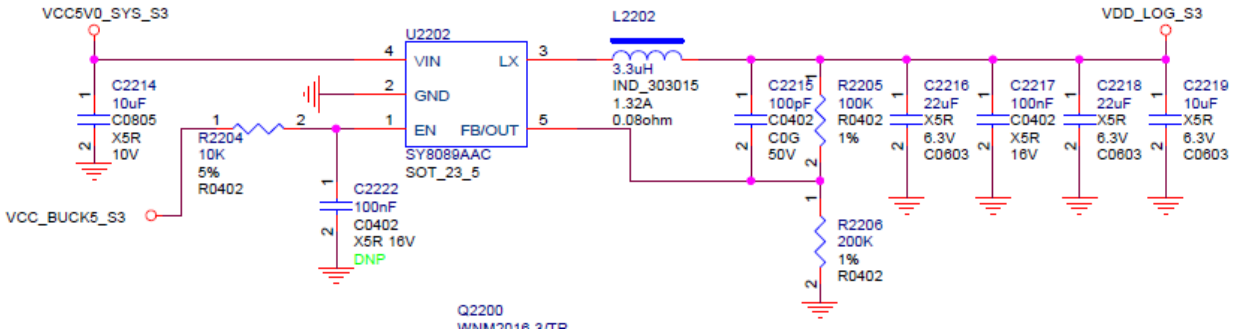



Figure 2–29 RK3399Pro VDD_LOG Power

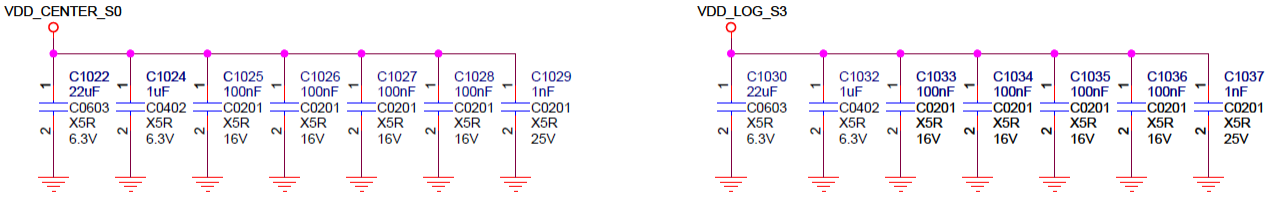



Figure 2–30 RK3399Pro Logic Power Decoupling

- **2.2.2.6 DDR Power**

RK3399Pro CPU DDR controller interface supports DDR3/DDR3L/LPDDR3/LPDDR4 protocol. Only need to supply power for DDRIO_VDD and the power level is different for different DDR components. There are several levels 1.5V/1.35V/1.2V/1.1V to be adjusted. Please confirm to meet the product design requirement according to the component used.

RK3399Pro DDR controller internally integrates Vref circuit to generate the required reference voltage Vref_mcu=VCC_DDR/2. The Vref of DRAM side is generated by resistance divider circuit, Vref_CA=VCC_DDR/2, while Vref_DQ can be adjusted according to ODT strategy, the corresponding Vref voltage can be adjusted according to the drive strength and the ODT value.

Take LPDDR3 as an example: At 800MHz frequency, the drive strength of RK3399Pro chip side is 34.3ohm, DRAM side ODT is configured as 240ohm, when ODT is enabled, calculate according to the formula DRAM Vref=0.56*VCC_DDR.

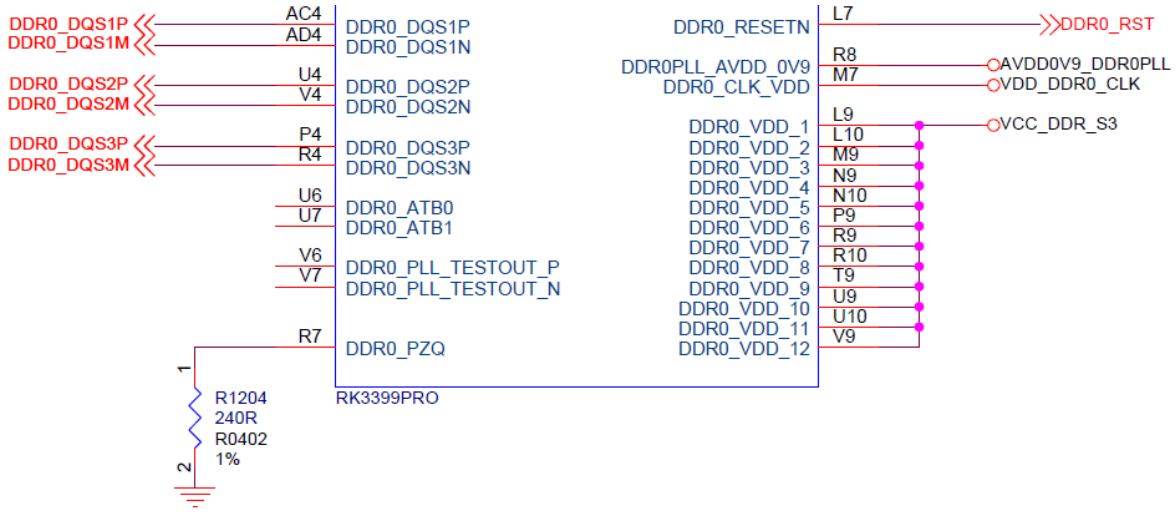



Figure 2–31 RK3399Pro DDR Controller Power

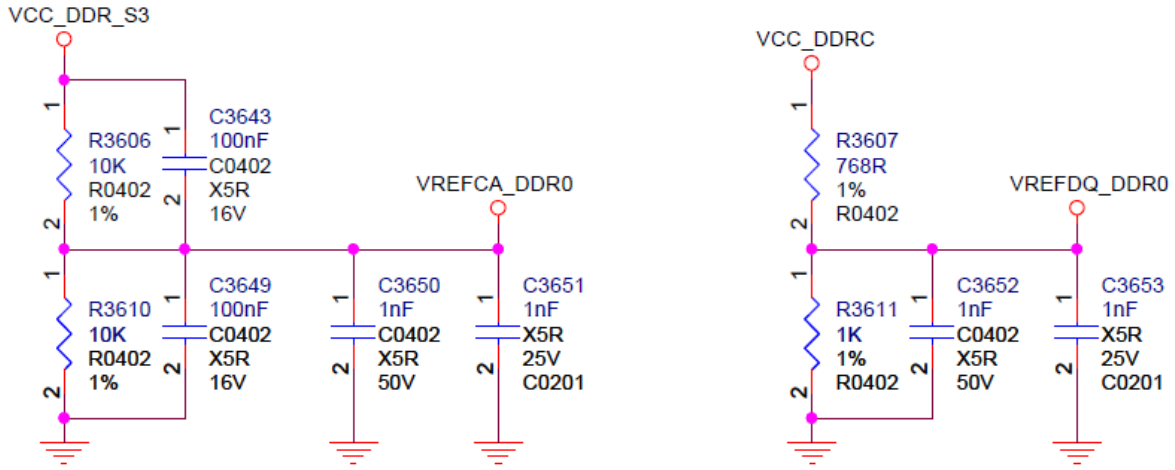



Figure 2–32 RK3399Pro LPDDR3 DRAM VREF Power Design

**Note**

*As for Vref_DQ design of various components:*

*LPDDR2 doesn't support ODT function; LPDDR4 Vref_DQ can be adjusted through software within the component; DDR3/DDR3L internal pull up/down will occur at the same time when ODT function is enabled, Vref_DQ- Vref_CA=VCC_DDR/2; So only LPDDR3 needs to adjust Vref_DQ separately.*

RK3399Pro DDR controller's internal clock is generated by a separate PLL and PLL needs a separate power supply（DDR0PLL_AVDD_0V9, DDR1PLL_AVDD_0V9）. Need to place a 100nF decoupling capacitor for each DDR PLL power pin and it should be placed close to the power supply pin.

RK3399Pro uses VCC_DDR_S3 to supply power for the power supply pin of DDR CLK signal (DDR0_CLK_VDD, DDR1_CLK_VDD). Recommend to series connect resistors routed star from the source to avoid the power noise from VCC_DDR_S3 power plane. Need to place a 100nF decoupling capacitor for each power supply pin and it should be placed close to the power supply pin.

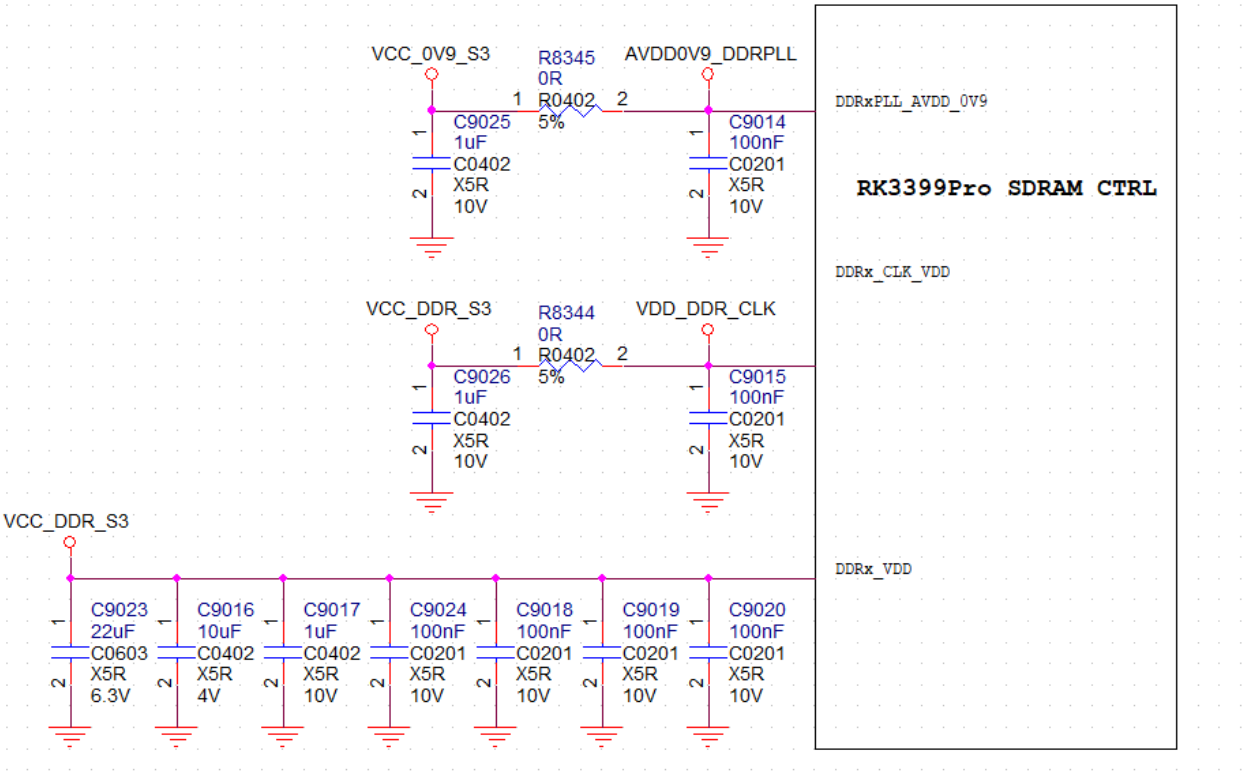



Figure 2–33 RK3399Pro DDR Controller Power Design

The DRAM VREF_DQ and VREF_CA of LPDDR3 use a separate VREF voltage reference circuit. The power of VREF_DQ pin can be supplied by a 1K ohm resistors divider (1% accuracy), because VREF_CA power is constantly supplied, change to use a 10Kohm resistors divider (1% accuracy) can reduce the standby power consumption and parallel connect 100nF capacitor can improve the power following characteristic of VCC_DDR_S3. Place a 1nF decoupling capacitor close to each reference power pin.

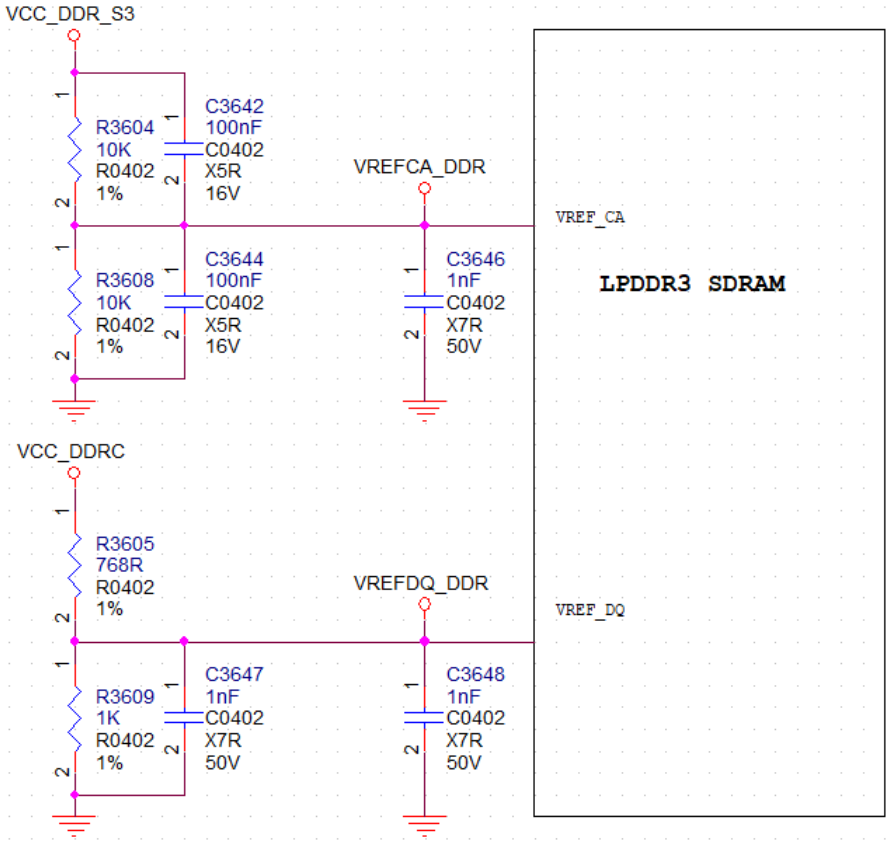



Figure 2–34 RK3399Pro LPDDR3 DRAM VREF Power Design

- **2.2.2.7 GPIO Power**

Refer to Section 2.1.9 for GPIO power. Recommend to place a 100nF decoupling capacitor close to each power pin. For detailed design please refer to RK3399Pro reference design schematic.

### 2.2.3 RK809-3 Solution Introduction

- **2.2.3.1 RK809-3 Block Diagram**

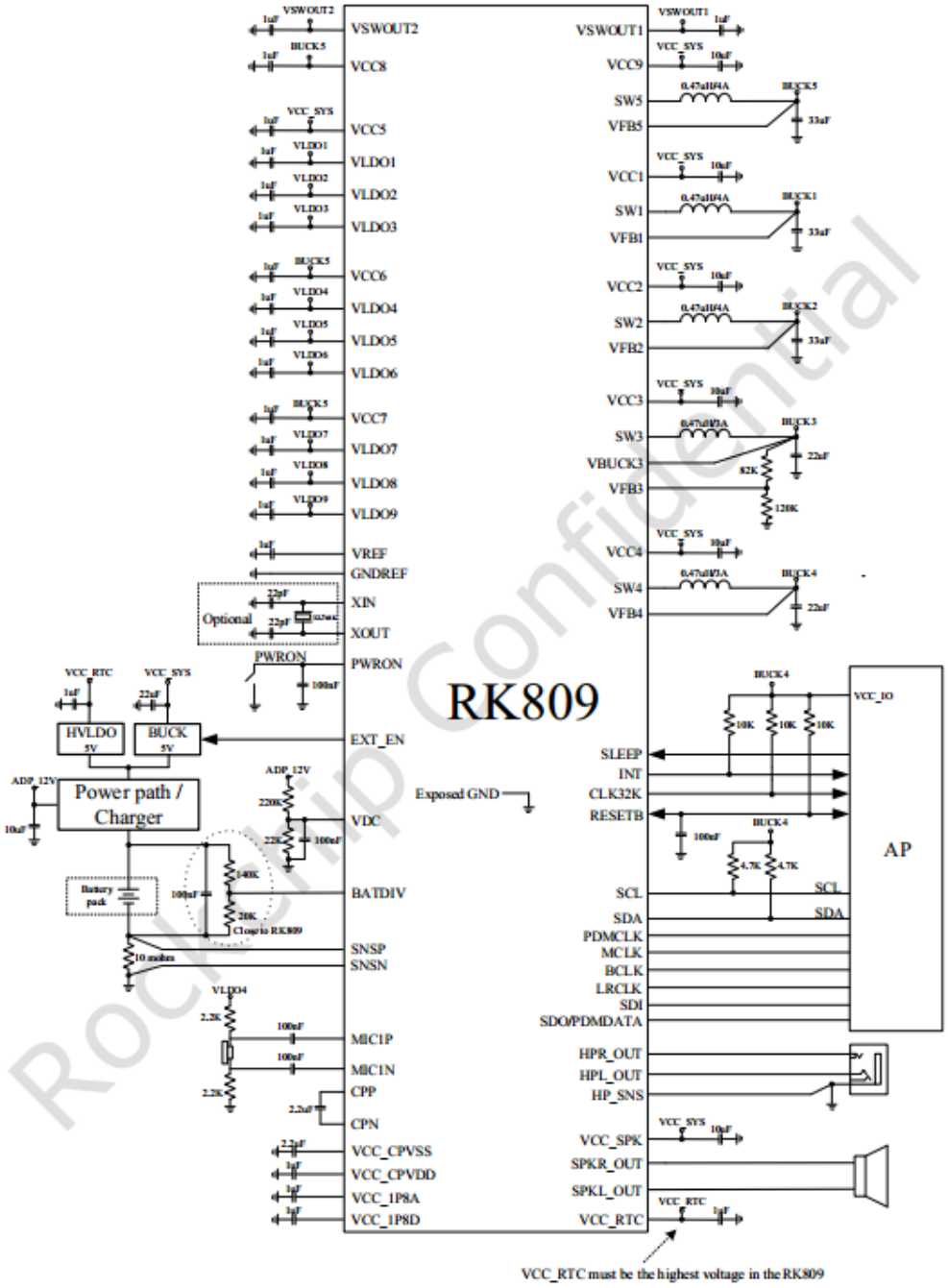



Figure 2–35 RK809-3 Block Diagram

- **2.2.3.2 RK809-3 Features**
  - Input range: 2.7V-5.5V
  - Accurate battery fuel gauge with two separate battery voltage and current ADC
  - Real time clock(RTC)
  - Low standby current of 16uA (at 32KHz clock frequency)
  - Real ground Headphone driver
  - 1.3W Class D PA without filter inductor
  - OTP programmable power up/down sequence and voltage
  - High performance audio codec
    - One internal PLL
    - Support microphone input
    - Support I2S as the digital signal interface for both DAC and ADC
    - Support Automatic Level Control(ALC),limiter and noise gating
    - Support programmable digital and analog gains
    - Audio resolution 16bits to 32bits
    - Sample rate up to 192KHz

- Provides master and slave work mode, software configurable
- Support 3 I2S formats (normal, left-justified, right-justified)
- Support PDM mode (externally input PCLK)

■ Power channels:
- Channel 1: Synchronous BUCK converter, 2.5A max
- Channel 2: Synchronous BUCK converter, 2.5A max
- Channel 3: Synchronous BUCK converter, 1.5A max
- Channel 4: Synchronous BUCK converter, 1.5A max
- Channel 5: Synchronous BUCK converter, 2.5A max
- Channel 6-7, 9-14: Low dropout regulator, 500mA max
- Channel 8: Low dropout regulator with low noise, high power supply rejection ratio, 100mA max
- Channel 15: Switch, 3A max
- Channel 16: Switch, 1.5A max

■ Package: 7mmx7mm QFN68

### 2.2.3.3 RK3399Pro+RK809-3 Power Tree

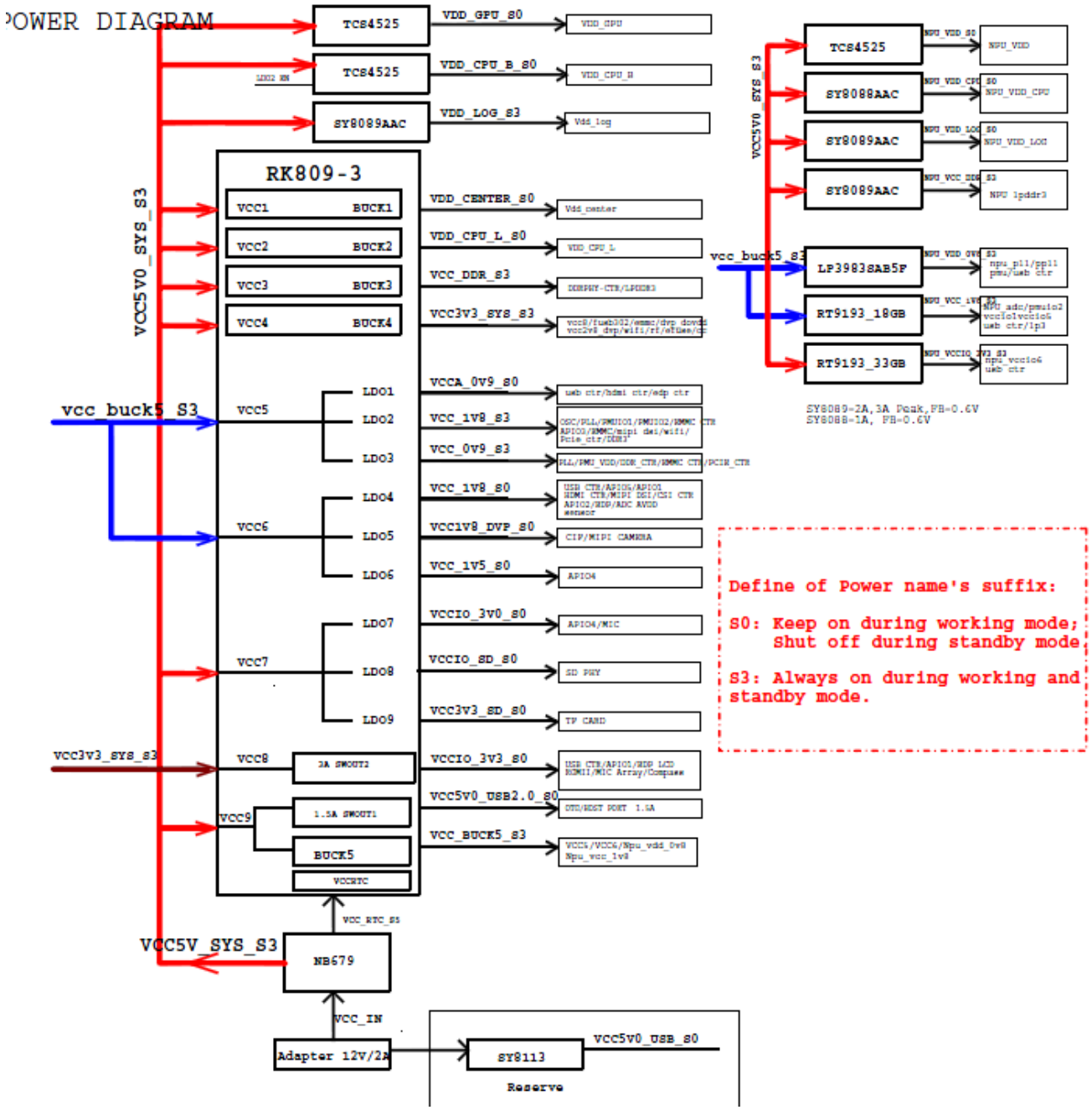



Figure 2–36 RK809-3 Power Tree

- **2.2.3.4 K809-3 Notice**
  - The recommended matching capacitance of 32.768KHz crystal is 22pF, and users can fine tune the parameter according to the specification of the crystal used.

---

Note

*In order to reduce the power consumption, PMIC RTC crystal oscillation is relatively weak, can not measure the oscillation signal on the XOUT or XIN pin with a normal oscilloscope, or oscilloscope probe will cause OSC stop working. Please test CLK32K pin if want to measure 32.768K signal.*

---

- VCC_RTC must be powered up first and the voltage value must be the highest one of the input powers supplying for RK809-3.
- The output capacitance of BUCK1, BUCK2 must be bigger than 30uF to ensure the good decoupling effect, especially in the case with large current and high dynamic load, you can appropriately increase the output decoupling capacitance.
- RK809-3 has the function of USB OTG power supply, short circuit protection, and can configure 1.0-1.5A output current limit.
- The power on logic directly controlled by input power is: when power input exists, primary DCDC buck output VCC5V0_SYS and VCC_RTC, the level input to VDC after external voltage divider circuit is more than 0.55V, and then PMIC starts to work and output the voltage.
- The power on/off logic controlled by the switch is: PWRON pin embeds pull up resistor, pull up to VCCRTC, it will automatically power on when detecting the low level over 500ms. After power on, if PWRON pin is pulled down over 6s, it will power off forcely (usually used for forced power off after system crash, then power on). Before sleep and resume operation, the low level of PWRON pin should maintain over 20ms.
- RK809-3 work basic condition:
  - VCC_RTC supply power.
  - VCC5V0_SYS supply power.
  - When detecting one of below three cases, RK809-3 will automatically power on: PWRON pin keeps low level for 500ms, VDC level is over 0.55V, internal RTC Alarm power on enabled and the time is up.
  - Start the power up process, each sequence interval is 2ms, the next sequence continues only when the output voltage of last sequence meets the requirement, until all sequences power up end, and release reset, finish the power up process.

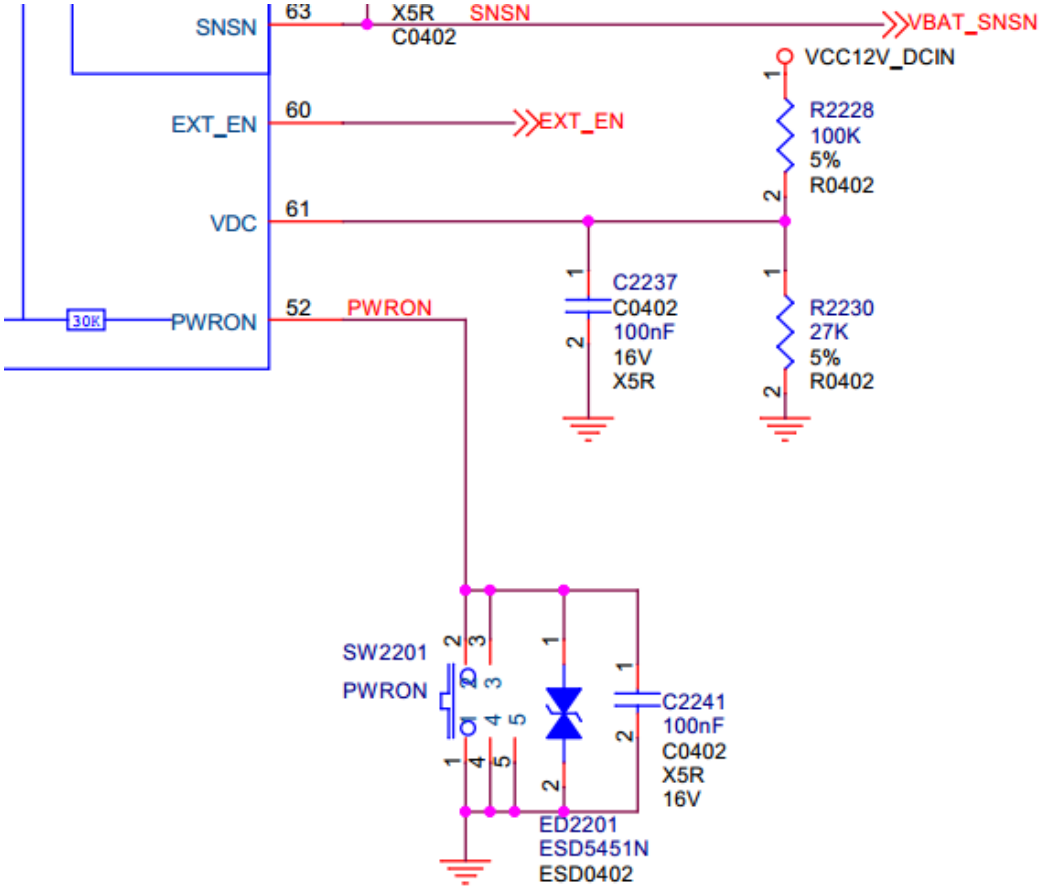



Figure 2–37 RK809-3 PWRON Pin

- When RK809-3 detects one of below two cases, it will automatically power off:
  - I2C write DEVICE_OFF=1
  - PWRON pin keeps low over 6s.
- When RK809-3 starts the power down process, it will pull down reset after one RTC clock cycle (around 30.5us), and then turn off all power output after 2ms, finish the power down process.

#### 2.2.3.5 RK809-3 Design Instruction

For RK809-3 detailed design instruction, please refer to Rockchip PMIC related design document 《RK809 Application Guide》.

### 2.2.4 Others

#### 2.2.4.1 Over Temperature Protection Circuit

When RK3399Pro CPU occurs over-temperature or crash, the TSADC_INT/GPIO1_A6 pin of the chip will output high level to reset RK809-3 and control the power off and restart, reset the whole system while the register is cleared.

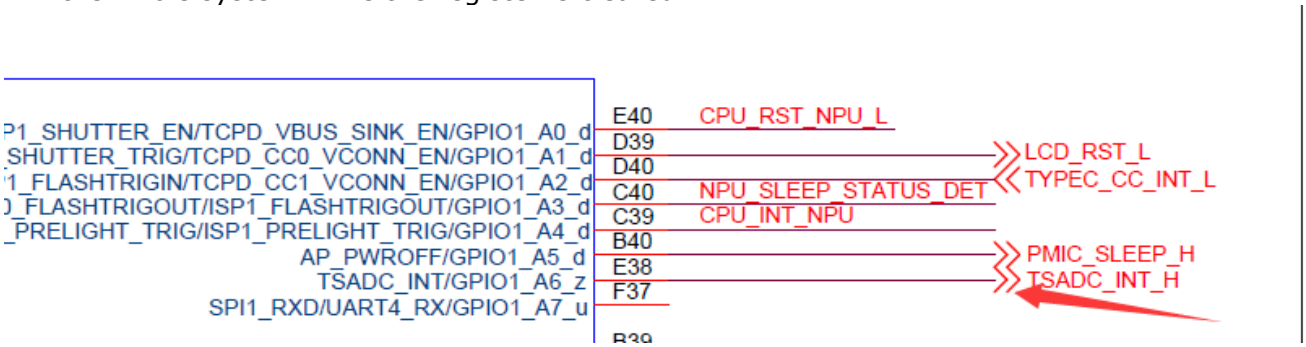



Figure 2–38 RK809-3 TSADC_INT_H Over Temperature Protection Output

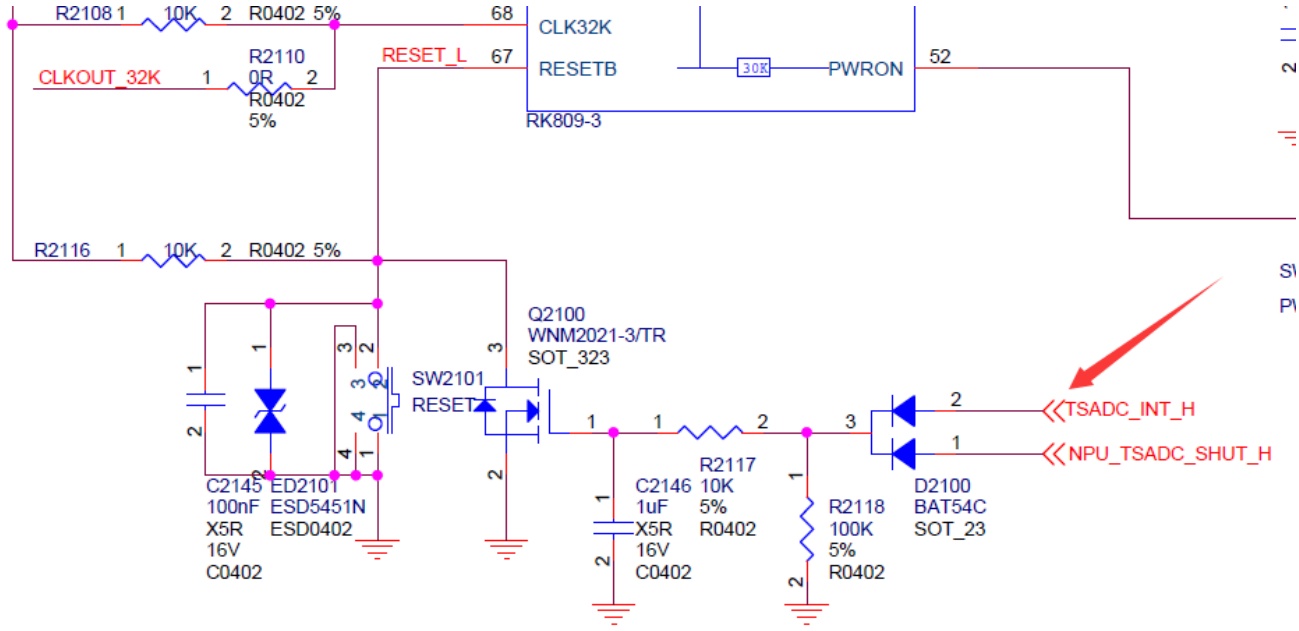



Figure 2–39 RK809-3 TSADC_INT_H over Temperature Protection Input

- **2.2.4.2 PMIC SLEEP Circuit**

When RK3399Pro is in work mode, the status pin PMIC_SLEEP of the chip will keep low level output.

When the system enters standby mode, the PMIC_SLEEP pin will output sleep indicating signal with high level, and then PMIC will enter sleep status controlled by the signal. According to the configuration of software dts file, some power supply will turn off, and some power supply will lower down the voltage.

When the system is resumed from standby mode, the PMIC_SLEEP pin will output low level at the first time, and the PMIC and all the power supply will be back to normal work

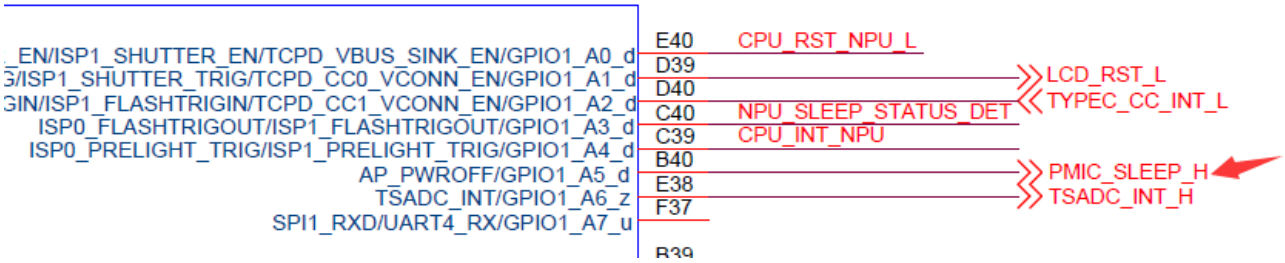



Figure 2–40 RK3399Pro PMIC_SLEEP Output

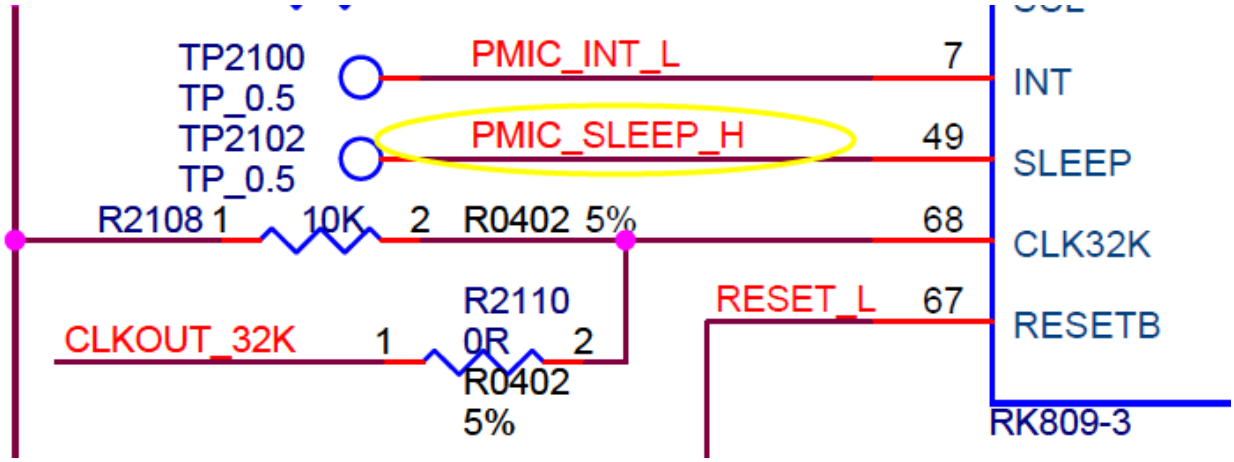



Figure 2–41 RK809-3 PMIC_SLEEP Input

### 2.2.5 CPU Power Peak Current

Below table shows the peak current test result of the running mode for RK3399Pro EVB, only for reference. The test conditions are as below:

- APK Version: antutu_benchmark_v7_3d+run.sh
- DDR component: 32bit LPDDR3 K4E6E304EB-EGCF
- Oscilloscope enables the 20MHz bandwidth limitation.

| Configuration | ITEM | SOC Model | CPU frequency | NPU frequency | Memory | GPU Render | GPU Frequency | DDR Type | DDR Frequency | Bat voltage (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| | RK3399Pro | Dual-core Cortex-A72 + Quad-core Cortex-A53 + NPU | A72 Max: 1800MHz 1.20V<br>A53 Max: 1416MHz 1.125V | Max: 800MHz 0.85V | CPU: 4G<br>NUP: 2G | Mail-T860MP4 | Max: 800MHz 1.075V | CPU: LPDDR3<br>NPU: LPDDR3 | CPU DDR Max: 800MHz<br>NPU DDR Max: 786M | |

Figure 2–42 RK3399Pro EVB Peak Current Test Condition

Table 2–10 RK3399Pro CPU Peak Current Table

| PowerName | Voltage（V） | Peak Current(mA) |
|---|---|---|
| VCC5V0_SYS | 4.970 | 3461.0 |
| VCC3V3_SYS | 3.291 | 378.2 |
| VCC_BUCK5_S3 | 3.302 | 529.5 |
| VDD_CPU_B_S0 | 1.220 | 2429.9 |
| VDD_CPU_L_S0 | 1.141 | 654.0 |
| VDD_GPU_S0 | 1.112 | 3403.9 |
| VDD_LOG_S0 | 0.901 | 1267.0 |
| VCC_DDR_S3 | 1.262 | 845.4 |
| VCC_0V9_S3 | 0.901 | 33.9 |
| VCC_1V8_S3 | 1.792 | 243.9 |

## 2.3 CPU Function Interface Circuit Design Guide

### 2.3.1 CPU Memory Card Circuit

RK3399Pro provides a SDMMC interface controller which can support SD v3.0 and MMC v4.51 protocol, shown as below:

- SDMMC controller has an independent power domain.
- SDMMC multiplexed with the functions such as UART2, JTAG etc., select function through SDMMC0_DET. For details please refer to section 2.1.4.
- Embedded LDO and electronic switch, SDMMC0_VDDPST pin only needs to externally connect a 100nF decoupling capacitor to GND, VDD power supply is provided internally.
- SDMMC0_VDD is IO power, need to externally provide 3.0V power supply (SD 2.0 mode) or 3.0V/1.8V adjustable power supply (SD 3.0 mode).

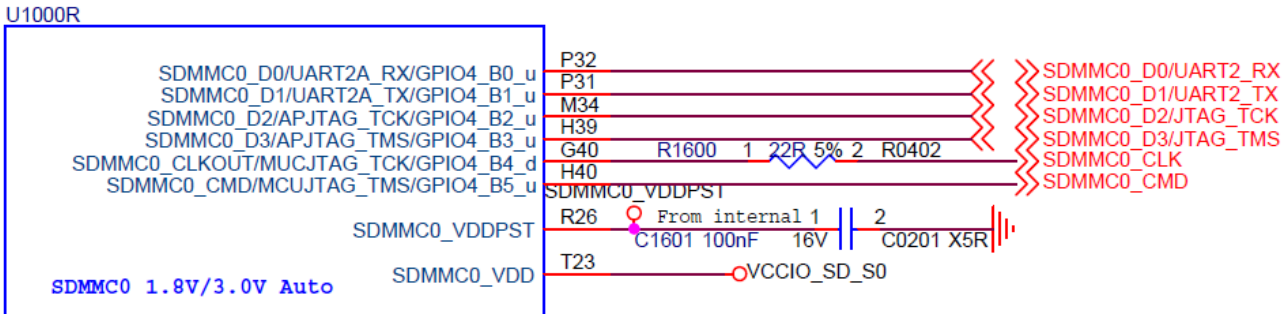



Figure 2–43 RK3399Pro SDMMC Module Circuit

The pull-up/down and matching design of the SDMMC interface are recommended as below table:

Table 2–11 RK3399Pro SDMMC Interface Design

| Name | Internal pull up/down | Connection method (SDR104 high-speed mode) | Description(chip side) |
|---|---|---|---|
| SDMMC_DQ[3:0] | Pull up | Series connect 22ohm resistor can be deleted if the trace is short | SD data output/input |
| SDMMC_CLK | Pull down | Series connect 22ohm resistor | SD clock output |
| SDMMC_CMD | Pull up | Series connect 22ohm resistor can be deleted if the trace is short | SD command output/input |

### 2.3.2 CPU Ethernet Port Circuit

RK3399Pro internally integrates a GMAC controller which can externally connect with different Ethernet PHY to support the 100M/1000M network function. For the detailed design, please refer to the design documents released by PHY vendors.

In giga mode, the work clock used by PHY needs to be provided by external crystal as

shown below:

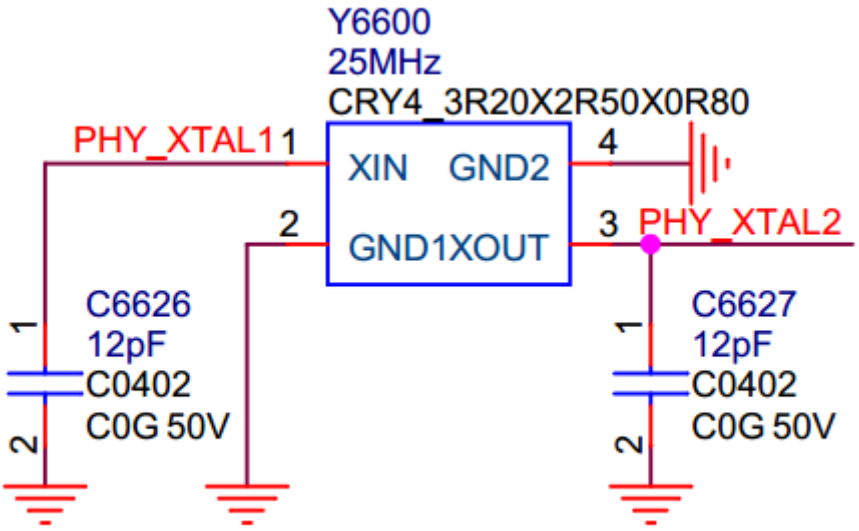



Figure 2–44 Giga PHY Work Clock

In Mega mode, the work clock used by PHY can be provided by MAC controller of RK3399Pro to save a crystal in PHY side.

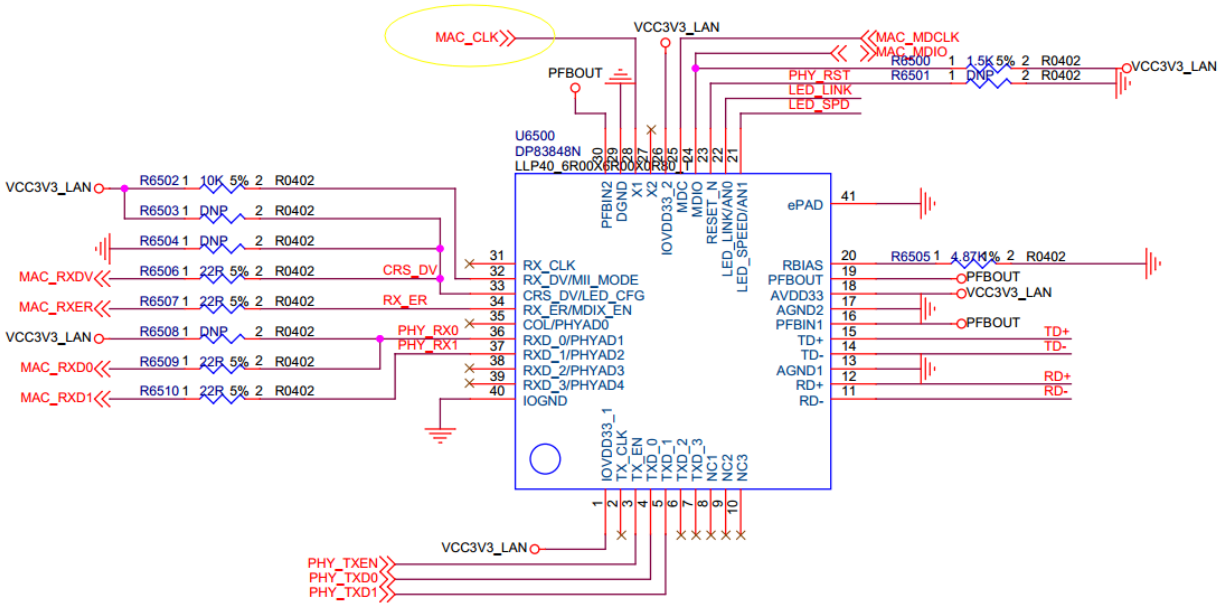



Figure 2–45 Mega PHY Work Clock

RK3399Pro MAC controller needs two power supply, core voltage is 1.8V（Pin J22）, IO voltage is 3.3V（Pin J23）, so the IO power supply voltage of PHY needs to be consistent with the IO level of MAC controller, that is 3.3V.

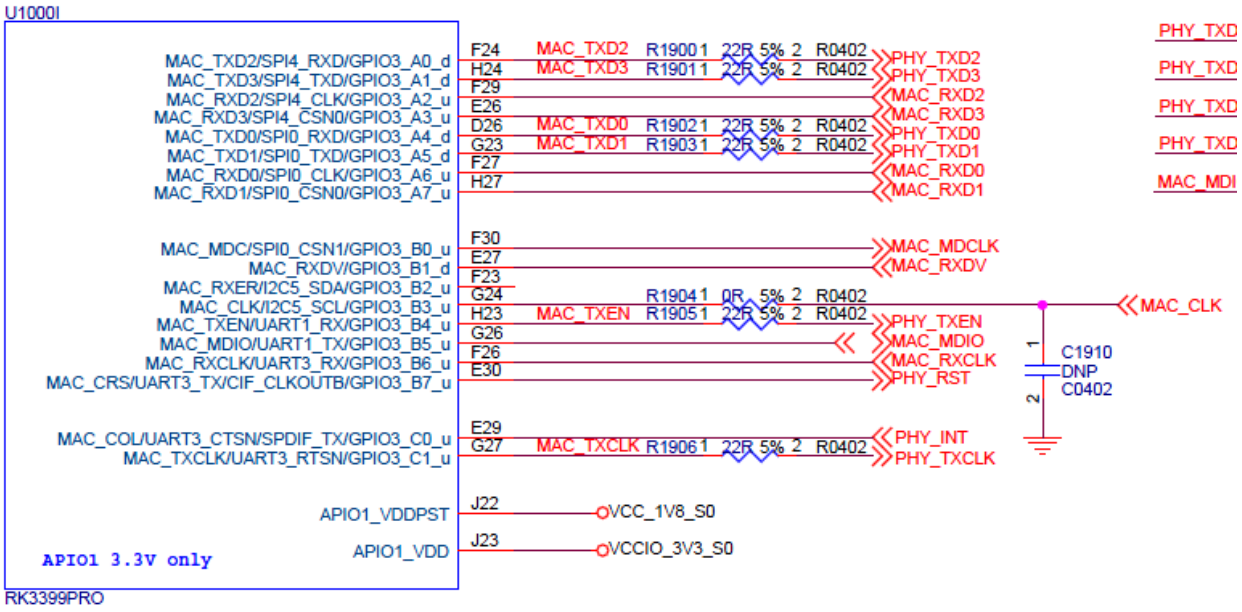



Figure 2–46 Mega PHY Work Clock

MAC controller can reset PHY via GPIO, and can also use the RC hardware reset circuit to do it, it should be noted that the PHY power supply must be controllable if using RC hardware reset circuit.

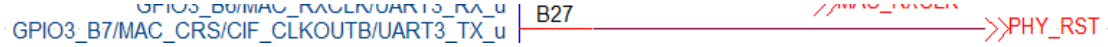



Figure 2–47 RK3399Pro MAC Controller Reset

MDIO interface, clock MDC signal and data MIDO signal are used to transmit the control and status information between MAC controller and PHY. It should be noted that MDIO signal needs to be pulled up as shown below:


Figure 2–48 RK3399Pro RGMII MDIO Signal

- **2.3.2.1 1000M MAC**

RK3399Pro supports 10/100/1000M MAC. Now introduce the 1000M GMAC part design and notices as below:

Table 2–12 RK3399Pro RGMII Interface Design

| Name | Internal pull up/down | Connection method | Description |
|---|---|---|---|
| MAC_TXCLK | Pull up | Series connect 22ohm resistor close to MAC side | Reference clock for data output |
| MAC_RXCLK | Pull up | Series connect 22ohm resistor close to PHY side | Reference clock for data input |
| MAC_TXD[3:0] | Pull down | Series connect 22ohm resistor | Data output |

| | | | |
|---|---|---|---|
| | | close to MAC side | |
| MAC_RXD[3:0] | Pull up | Series connect 22ohm resistor close to PHY side | Data input |
| MAC_TXEN | Pull up | Series connect 22ohm resistor close to MAC side | Data output enable |
| MAC_RXDV | Pull down | Series connect 22ohm resistor close to PHY side | Receive data valid indication |
| MAC_MDC | Pull up | Direct connection | Configure interface clock |
| MAC_MDIO | Pull up | Direct connection | Configure interface I/O |
| MAC_CLK | Pull up | Series connect 22ohm resistor close to PHY side | MAC main clock input, 125MHz |

- On RGMII interface output/input signal line, the TX_CLK and RX_CLK frequency is 125 MHz. In order to achieve the transmission rate of 1000 Mb, TXD and RXD signal lines are sampled in the bilateral edge of the clock. Data enable signal (MAC_TXEN, MAC_RXDV) must be enabled before data transmit is valid.

#### 2.3.2.2 100M MAC

RK3399Pro supports 10/100/1000M GMAC. Now introduce the 100M MAC part design and notices as below:

Table 2–13 RK3399Pro RMII Interface Design

| Name | Internal pull up/down | Connection method | Description |
|---|---|---|---|
| MAC_TXCLK | Pull up | Series connect 22ohm resistor close to MAC side | Reference clock for data output |
| MAC_RXCLK | Pull up | Series connect 22ohm resistor close to PHY side | Reference clock for data input |
| MAC_TXD[1:0] | Pull down | Series connect 22ohm resistor close to MAC side | Data output |
| MAC_RXD[1:0] | Pull up | Series connect 22ohm resistor close to PHY side | Data input |
| MAC_TXEN | Pull up | Series connect | Data output enable |

| | | | |
|---|---|---|---|
| | | 22ohm resistor close to MAC side | |
| MAC_RXDV | Pull down | Series connect 22ohm resistor close to PHY side | Receive data valid indication |
| MAC_MDC | Pull up | Direct connection | Configure interface clock |
| MAC_MDIO | Pull up | Direct connection | Configure interface I/O |
| MAC_CLK | Pull up | Series connect 22ohm resistor close to MAC side | MAC main clock output, 50MHz |

- On RMII interface output/input signal line, the MAC_CLK frequency is 50MHz; it is reference clock for RMII data output/input and sampling the data once every clock cycle. Data enable signal (MAC_TXEN, MAC_RXDV) must be enabled before data output is valid.
- In 10/100M RMII mode, it should be noted that the PHY_CRS_DV must be connected to MAC_RXDV of RK3399Pro, but not MAC_CRS pin.

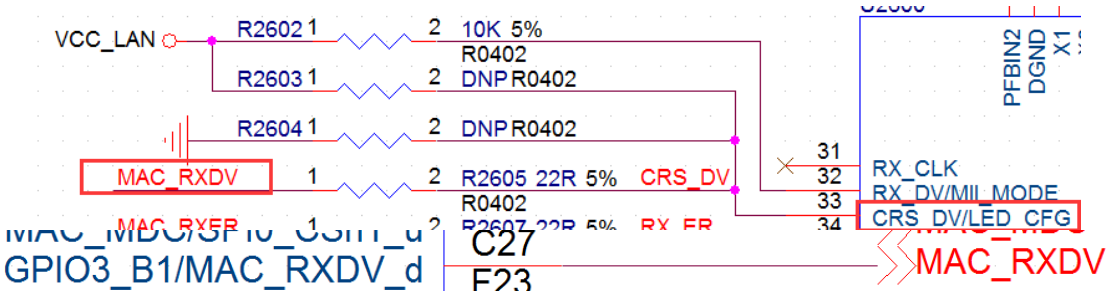



Figure 2–49 RK3399Pro RMII Interface MAC_RXDV

### 2.3.3 CPU USB Circuit

RK3399Pro CPU includes two USB 2.0 controllers and two USB 3.0 controllers, a USB 2.0 controller and a USB 3.0 controller used together can compose a complete USB 3.0 (or Type-C) interface.

**Note**

When USB 2.0 controller and USB 3.0 controller are used in conjunction, need to follow the rule that the USB 2.0 PHY0 should match with USB 3.0 PHY0 and USB2.0 PHY1 should match with USB 3.0 PHY1.

#### 2.3.3.1 USB 2.0

RK3399Pro USB 2.0 includes USB2.0 PHY0, USB2.0 HOST0, USB2.0 HOST1 and USB2.0 OTG1 the four USB controllers and there are four USB 2.0 interfaces in total.

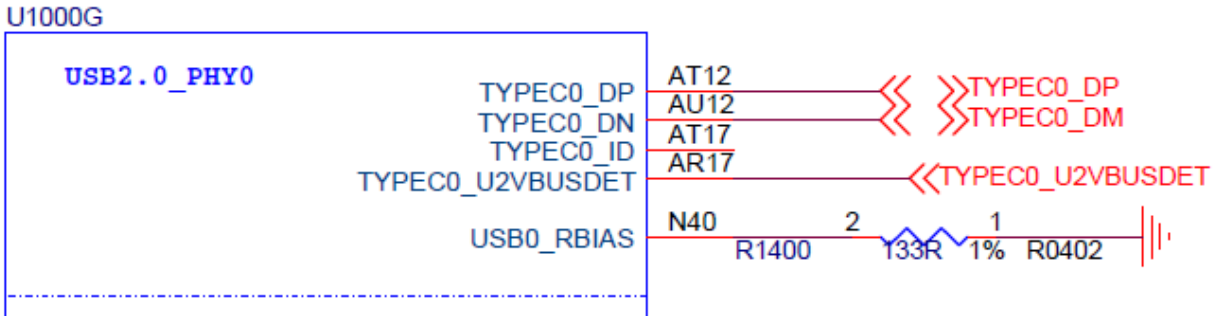



Figure 2–50 RK3399Pro USB 2.0 PHY0

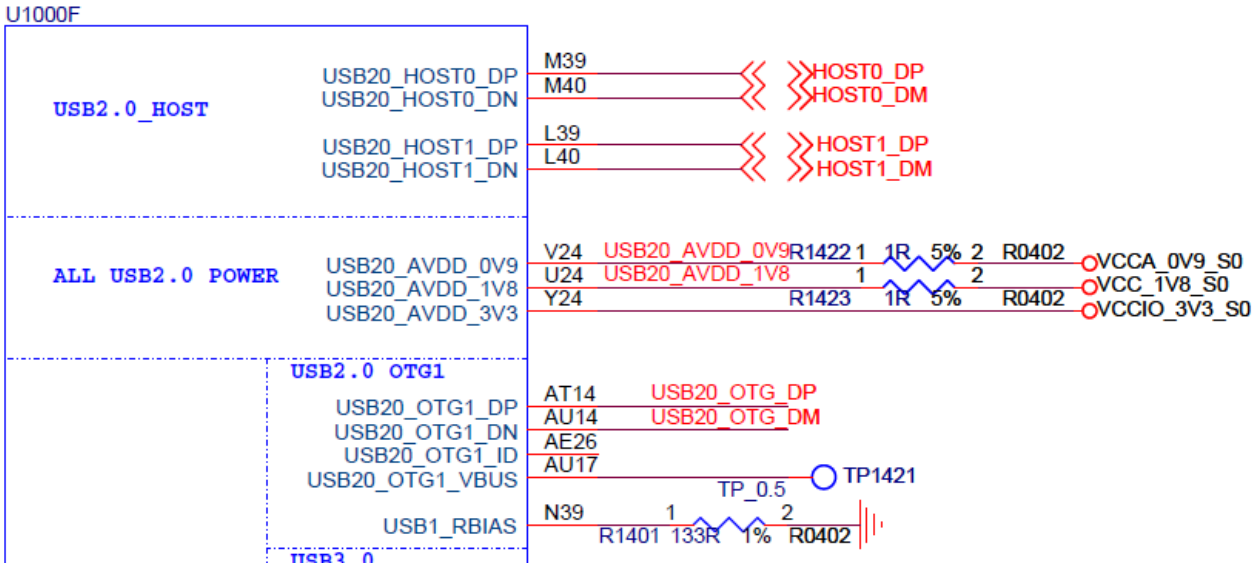



Figure 2–51 RK3399Pro USB 2.0 HOST0&HOST1&OTG1

Please note for design:

- USB2.0_PHY0 interface is default used as system firmware download port which must be reserved for debugging.

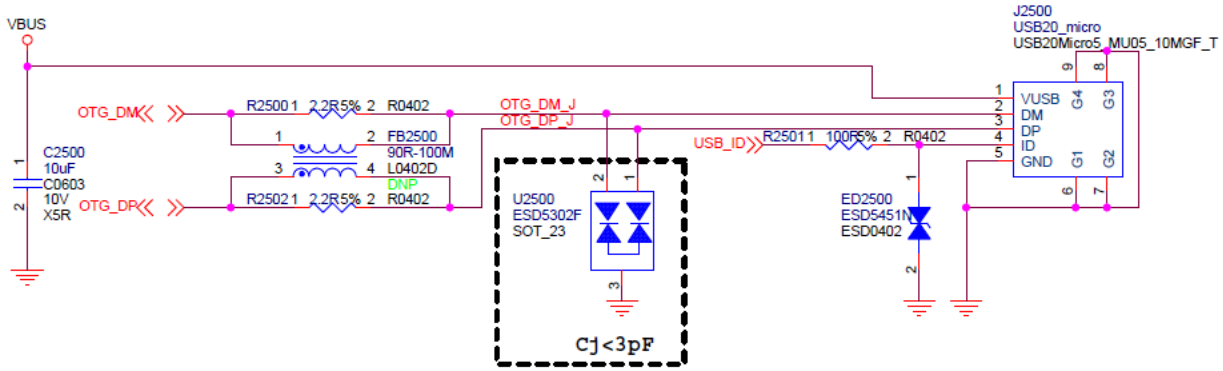



Figure 2–52 RK3399Pro USB Connection Socket

- USB2.0 OTG1 is used as the communication port of CPU and NPU, connected to NPU by default, and cannot be extended to be other USB.
- USB_ID has an internal 200K pull up resistor, pull up to USB_AVDD_1V8, so OTG is default used as Device mode.
- USB_VBUS (USB_DET) is used as USB insertion detection, and it means there is USB inserted when detecting high level.

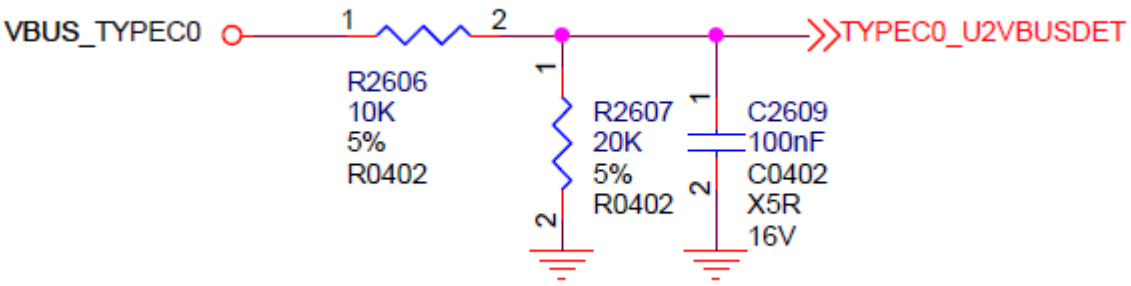



Figure 2–53 RK3399Pro USB Insertion Detection

- USB controller configuration reference resistor R1400 should select the resistor with 1% accuracy, because it will affect the USB amplitude and influence the quality of eye diagram.

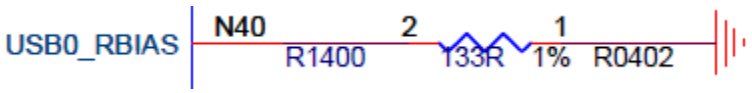



Figure 2–54 RK3399Pro USB20 Controller Reference Resistance 1

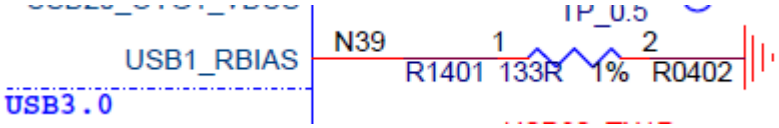



Figure 2–55 RK3399Pro USB20 Controller Reference Resistance 2

- The controller 0.9V/1.8V power needs to series connect 1ohm resistor to avoid the damage caused by surge.

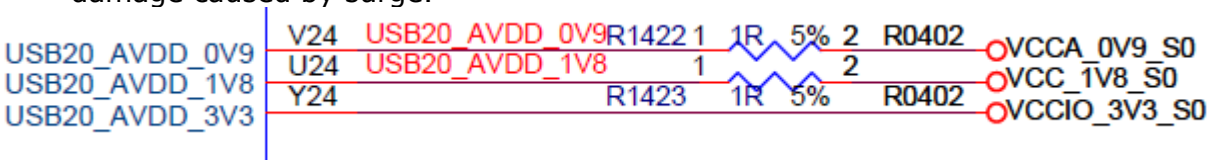



Figure 2–56 RK3399Pro USB Controller Power Anti-surge

- In order to improve USB performance, the decoupling capacitor of the controller power should be placed close to the pin.
- In order to suppress EMI, Common mode choke can be reserved in signal line and select to use resistor or common mode choke according to the actual situation during debugging.

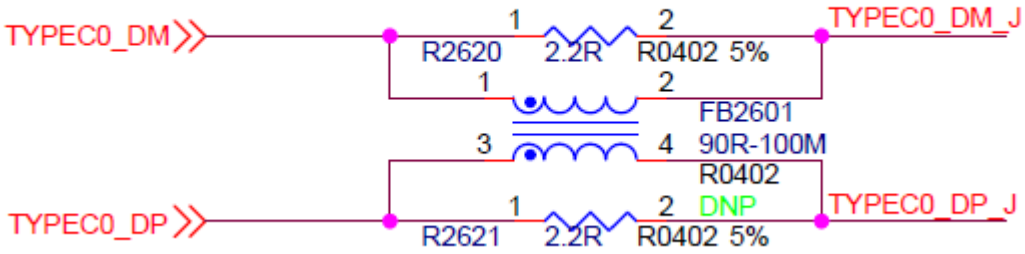



Figure 2–57 RK3399Pro USB Reserved Common Mode Choke

USB2.0 interface pull up/down and matching design are recommended as below table:

Table 2–14 RK3399Pro USB2.0 Interface Design

| Name | Connection method | Description |
|---|---|---|
| TYPEC0_DP/DM | Series connect 2.2ohm resistor | USB2.0 OTG0 input/output, can compose Type-C0 interface with USB3.0 PHY0 |
| TYPEC0_ID | Direct connect, internal pull up | USB2.0 OTG0 ID recognition, no need to connect for Type-C interface<br>Need to use for Micro-B interface |
| TYPEC0_U2VBUSDET | Resistor voltage divider detection | USB2.0 OTG0 insertion detection |
| USB0_RBIAS | | USB2.0 PHY0 configuration reference resistor, 133ohm connected to GND, effective for HOST0 and OTG0 |
| USB20_HOST0_DP/DM | Direct connection | USB2.0 HOST0 input/output |
| USB20_HOST1_DP/DM | Direct connection | USB2.0 HOST1 input/output |
| USB20_OTG1_DP/DM | Direct connection | USB2.0 OTG1 input/output, can compose Type-C1 interface with USB3.0 PHY1 |
| USB20_OTG1_ID | NA | USB2.0 OTG1 ID recognition, no need to connect for Type-C interface<br>Need to use for Micro-B interface |
| USB20_OTG1_U2VBUSDET | NA | USB2.0 OTG1 insertion detection |
| USB1_RBIAS | | USB2.0 PHY1 configuration reference resistor, 133ohm connected to GND, effective for HOST1 and OTG1 |

- **2.3.3.2 USB 3.0**

  RK3399Pro USB 3.0 includes TYPEC_PORT0 and USB3.0 PHY two interfaces.

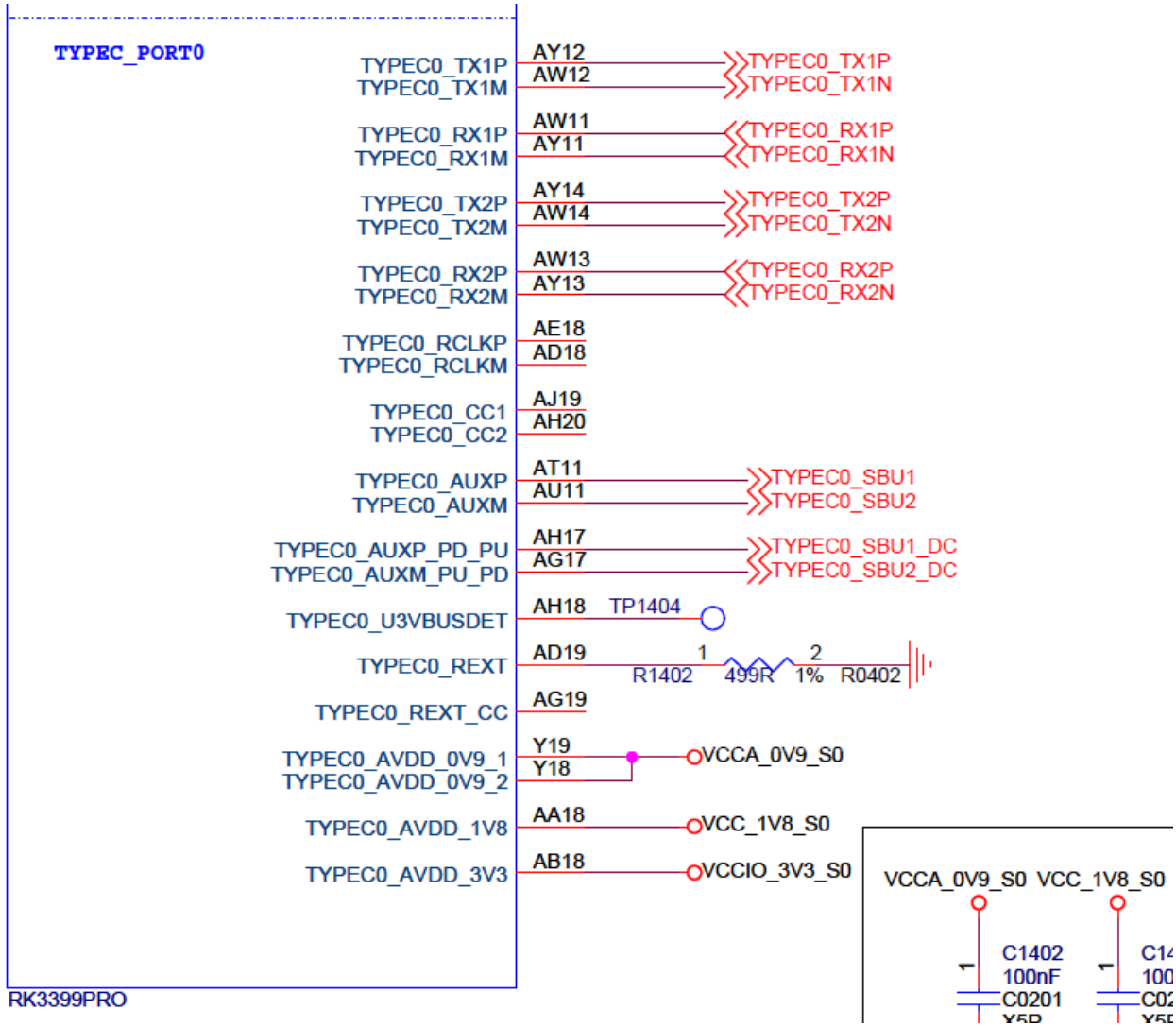



Figure 2–58 RK3399Pro USB3.0 TYPEC_PORT0

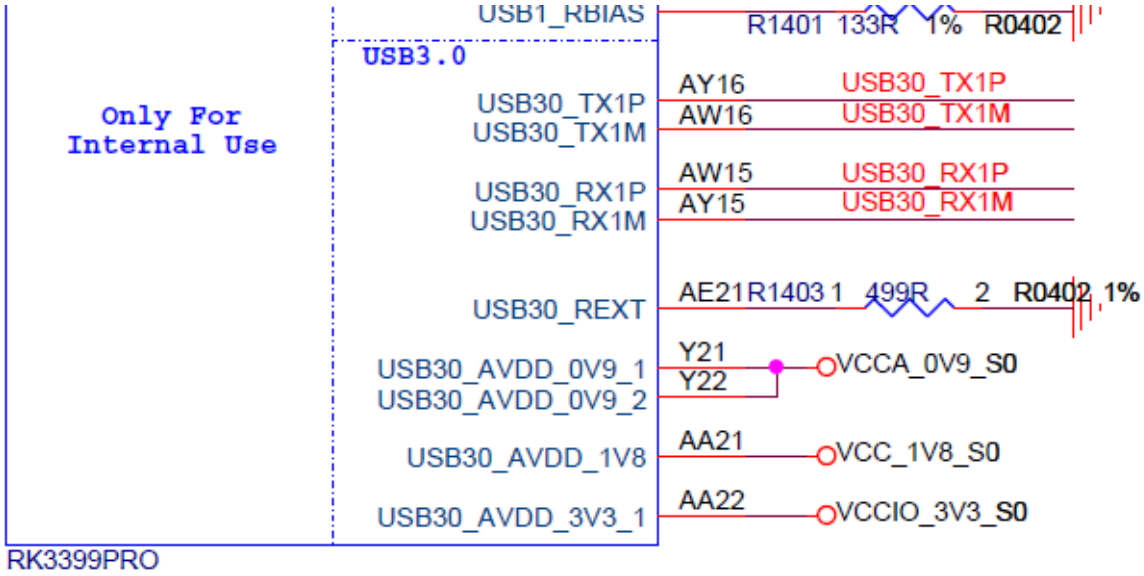



Figure 2–59 RK3399Pro USB3.0 PHY

USB3.0 interface pull up/down and matching design are recommended as below table:

Table 2–15 RK3399Pro USB3.0 Interface Design

| Name | Connection method | Description |
|---|---|---|
| TYPEC0_TX1P/TX1M | 100nF capacitor coupling connection | USB3.0 PHY0 SuperSpeed output data 1 |
| TYPEC0_TX2P/TX2M | 100nF capacitor coupling connection | USB3.0 PHY0 SuperSpeed output data 2 |
| TYPEC0_RX1P/RX1M | Direct connection | USB3.0 PHY0 SuperSpeed intput data 1 |
| TYPEC0_RX2P/RX2M | Direct connection | USB3.0 PHY0 SuperSpeed intput data 2 |
| TYPEC0_RCLKP/RCLKM | NA | USB3.0 PHY0 external reference clock, not used |
| TYPEC0_CC1/CC2 | NA | USB3.0 PHY0 embedded CC control signal, not used |
| TYPEC0_AUXP/AUXM | 100nF capacitor coupling connection | USB3.0 PHY0 auxiliary signal |
| TYPEC0_AUXP_PD_PU | NA | USB3.0 PHY0 auxiliary signal DC bias |
| TYPEC0_AUXM_PU_PD | NA | USB3.0 PHY0 auxiliary signal DC bias |
| TYPEC0_U3VBUSDET | NA | Not used |
| TYPEC0_REXT | | USB3.0 PHY0 configuration reference resistor, 499R connected to GND |
| TYPEC0_REXT_CC | NA | USB3.0 PHY0 embedded CC control signal configuration reference resistor, 499R connected to GND, not used. |
| USB30_TX1P/TX1M | 100nF capacitor coupling connection | USB3.0 PHY1 SuperSpeed output data |
| USB30_RX1P/RX1M | Direct connection | USB3.0 PHY1 SuperSpeed intput data |
| USB30_REXT | | USB3.0 PHY1 configuration reference resistor, 499R connected to GND. |

Usage note:

- CC1/CC2 is embedded CC controller signal, current reference design is using external CC/PD detection chip, so it is not used so far.
- USB 3.0 and USB 2.0 should be collocation used, in order to achieve the USB protocol compatible.
- If use USB 3.0 Type-A interface, default to use TYPEC0_TX1P/TX1M and TYPEC0_RX1P/RX1M as SSTX and SSRX signal, TYPEC0_TX2P/TX2M and TYPEC0_RX2P/RX2M cannot be used to separately support USB 3.0 Type-A interface.
- USB controller configuration reference resistor should select the resistor with 1% accuracy, and it will affect USB amplitude and influence the quality of eye diagram.

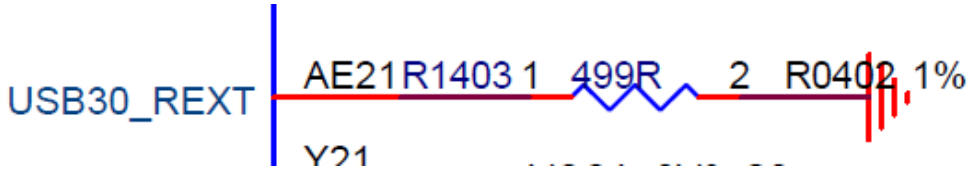



Figure 2–60 RK3399Pro USB30 Controller Reference Resistance

- In order to suppress EMI, common mode choke can be reserved in signal line and select to use resistor or common mode choke according to the actual situation during debugging.

#### 2.3.3.3 USB Type-C

USB Type-C interface should include a USB 2.0 OTG interface and a USB 3.0 interface. The reference design is shown as below:

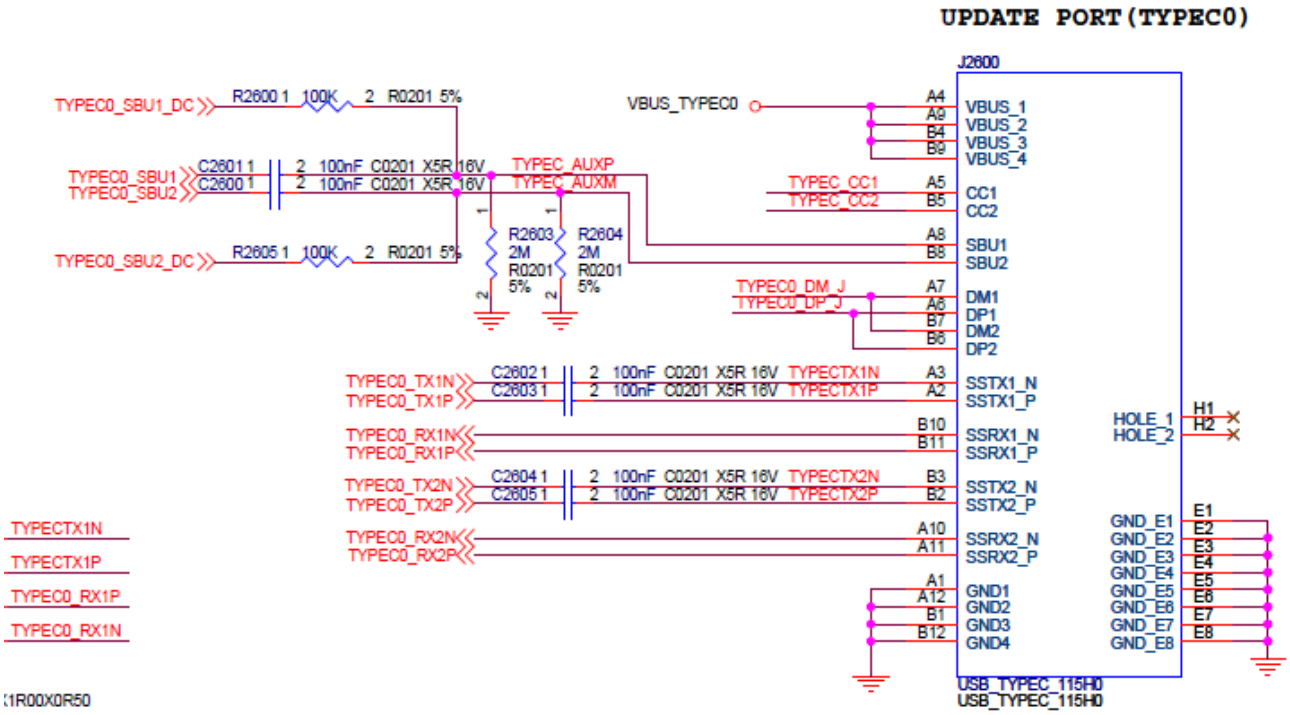



Figure 2–61 USB Type-C Interface

- The coupling capacitor of TX signal line should be placed close to the interface, the coupling capacitor of RX signal line is provided by the device.

### 2.3.4 CPU DP Circuit

RK3399Pro CPU USB3.0 PHY built-in DP（Display Port）controller, when determine to connect DP device, it can be connected directly without the control of USB protocol. The specific connection is divided into two cases: direct connect with DP device or DP conversion IC; or use USB Type-C cable to connect.

For the connection relationship in schematic, please make sure to follow the order in the table of this section to design.

#### 2.3.4.1 Device Direct Connection

In netbook product or industry application, DP panel or DP port conversion may be used, in this case, only need to connect the Type-C interface to the DP port according to the order of the signal.

Table 2–16 RK3399Pro DP Interface Design

| Name | Connection method | Description |
|---|---|---|
| TYPEC0_TX1P/TX1M | 100nF capacitor coupling connection | Correspond to DP_TX2P/TX2N |
| TYPEC0_TX2P/TX2M | 100nF capacitor coupling connection | Correspond to DP_TX1P/TX1N |
| TYPEC0_RX1P/RX1M | 100nF capacitor coupling connection | Correspond to DP_TX3P/TX3N |
| TYPEC0_RX2P/RX2M | 100nF capacitor coupling connection | Correspond to DP_TX0P/TX0N |
| TYPEC0_AUXP/AUXM | 100nF capacitor coupling connection, and provide DC bias | Correspond to DP_AUX auxiliary signal |

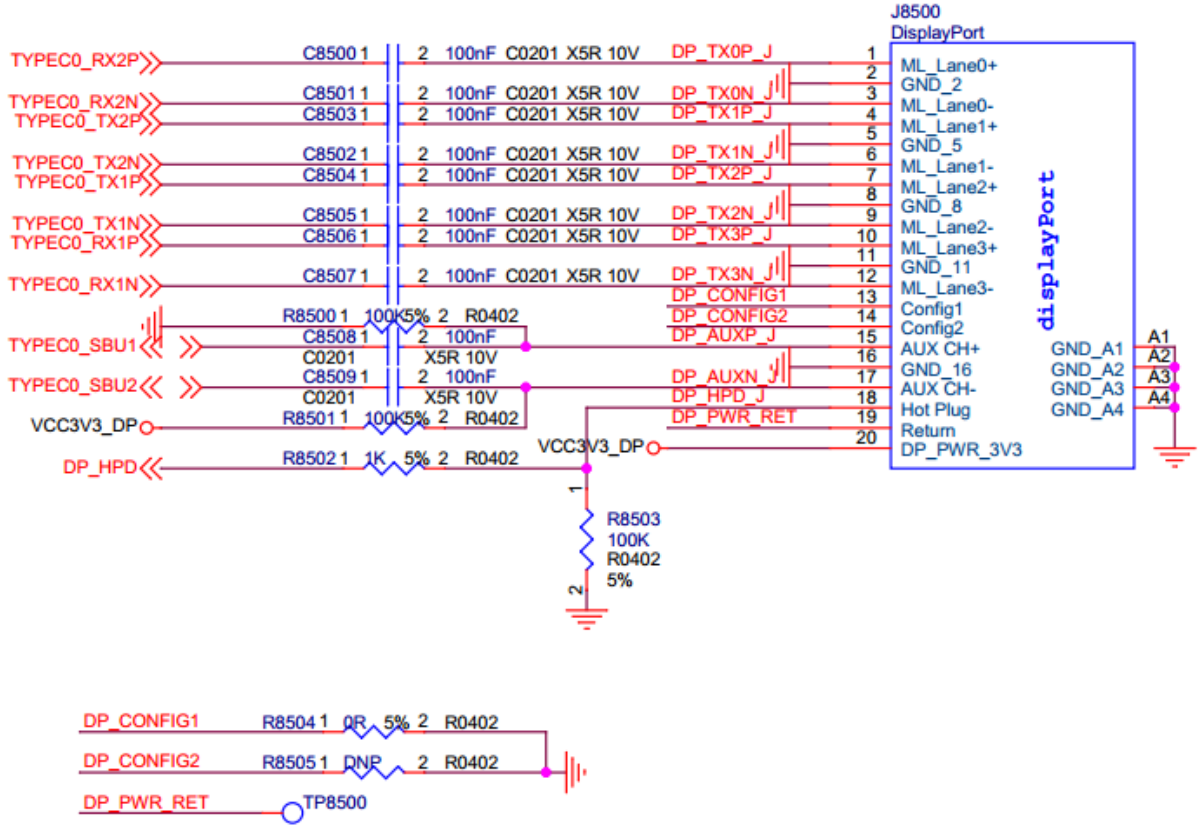



Figure 2–62 USB Type-C Converted to DP Port

- **2.3.4.2 Cable Connection**

In the application of split VR, it will occur that DP host uses USB Type-C cable to connect with the device, and the glass device uses DP converted to MIPI to output the image signal. Since the TX and RX in the USB Type-C cable are cross-over, need to do cross-processing for the signals on the device.

Table 3-15 is the Type-C cable connection relationship defined by the USB protocol:

Table 2–17 USB Full Function Type-C Standard Cable

| USB Type-C Plug #1 | | Wire | | USB Type-C Plug #2 | |
|---|---|---|---|---|---|
| Pin | Signal Name | Wire Number | Signal Name | Pin | Signal Name |
| A1,B1,A12,B12 | GND | 1[16] | GND_PWRrt1[GND_PWRrt2] | A1,B1,A12,B12 | GND |
| A4,B4,A9,B9 | Vbus | 2[17] | PWR_Vbus1[PWR_Vbus2] | A4,B4,A9,B9 | Vbus |
| A5 | CC | 3 | CC | A5 | CC |
| B5 | Vconn | 18 | PWR_Vconn | B5 | Vconn |
| A6 | Dp1 | 4 | UTP_Dp | A6 | Dp1 |
| A7 | Dn1 | 5 | UTP_Dn | A7 | Dn1 |
| A2 | SSTXp1 | 6 | SDPp1 | B11 | SSRXp1 |
| A3 | SSTXn1 | 7 | SDPn1 | B10 | SSRXn1 |
| B11 | SSRXp1 | 8 | SDPp2 | A2 | SSTXp1 |
| B10 | SSRXn1 | 9 | SDPn2 | A3 | SSTXn1 |
| B2 | SSTXp2 | 10 | SDPp3 | A11 | SSRXp2 |
| B3 | SSTXn2 | 11 | SDPn3 | A10 | SSRXn2 |
| A11 | SSRXp2 | 12 | SDPp4 | B2 | SSTXp2 |
| A10 | SSRXn2 | 13 | SDPn4 | B3 | SSTXn2 |
| A8 | SBU1 | 14 | SBU_A | B8 | SBU2 |
| B8 | SBU2 | 15 | SBU_B | A8 | SBU1 |
| Shell | Shield | Braid | Shield | Shell | Shield |

So RK3399Pro chip side is connected as shown in below table:

Table 2–18 RK3399Pro DP Interface Design – Chip Side

| Name | Connection method | Description |
|---|---|---|
| TYPEC0_TX1P/TX1M | 100nF capacitor coupling connection | Correspond to DP_TX2P/TX2M |
| TYPEC0_TX2P/TX2M | 100nF capacitor coupling connection | Correspond to DP_TX1P/TX1M |
| TYPEC0_RX1P/RX1M | Direct connection | Correspond to DP_TX3P/TX3M |
| TYPEC0_RX2P/RX2M | Direct connection | Correspond to DP_TX0P/TX0M |
| TYPEC0_AUXP/AUXM | 100nF capacitor coupling connection, and provide DC bias | Correspond to DP_AUX auxiliary signal |

VR glass side is connected as shown in below table:

Table 2–19 RK3399Pro DP Interface Design – VR Glass Side

| Name | Connection method | Description |
|---|---|---|
| TYPEC_TX1P/TX1M | 100nF capacitor coupling connection | Correspond to DP_TX3P/TX3M |
| TYPEC_TX2P/TX2M | 100nF capacitor coupling connection | Correspond to DP_TX0P/TX0M |
| TYPEC_RX1P/RX1M | Direct connection | Correspond to DP_TX2P/TX2M |
| TYPEC_RX2P/RX2M | Direct connection | Correspond to DP_TX1P/TX1M |
| TYPEC_AUXP/AUXM | 100nF capacitor coupling connection, and provide DC bias | Correspond to DP_AUX auxiliary signal |

### 2.3.5 CPU Audio Circuit

RK3399Pro provides two groups of standard I2S interface, supporting master or slave mode. They all support the highest sampling rate up to 192 kHz, bit rate from 16 bits to 32 bits.

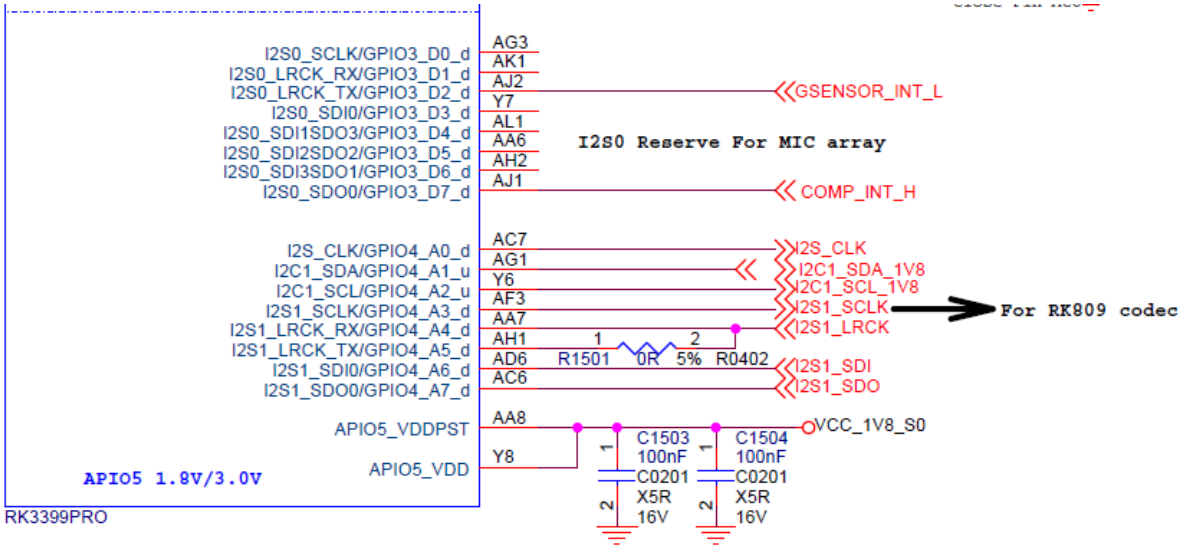



Figure 2–63 RK3399Pro I2S Module

- **2.3.5.1 I2S0**

I2S0 interface contains 1 SDI0,1 SDO0 and 3 SDIxSDOx interfaces, so it can flexibly configure SDIx and SDOx interface, support up to 8 channels input / 2 channels output or 2 channels input / 8 channels output at the same time. In order to meet the asynchronous sampling rate requirement of audio recording and playing, it provides two groups of frame clock (LRCKTX, LRCKRX). Need to pay attention to that, if SDOx and SDIx only refer to one group of frame clock, prefer to use LRCKTX as their common clock.

Need to pay attention to that, the I2S interface belongs to APIO5 power domain, and it is set to supply power for VCC_1V8_S0 by default. If I2S peripheral IO level is 3.3V, need to adjust the power supply, and match with the relative IO level of the power domain.

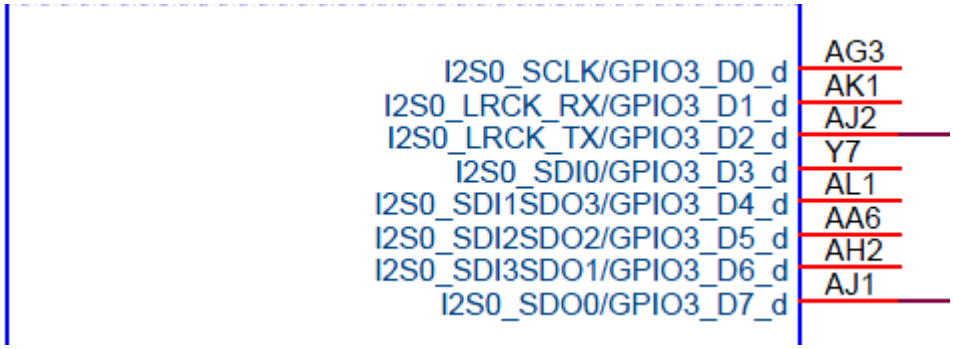



Figure 2–64 RK3399Pro I2S0 Module

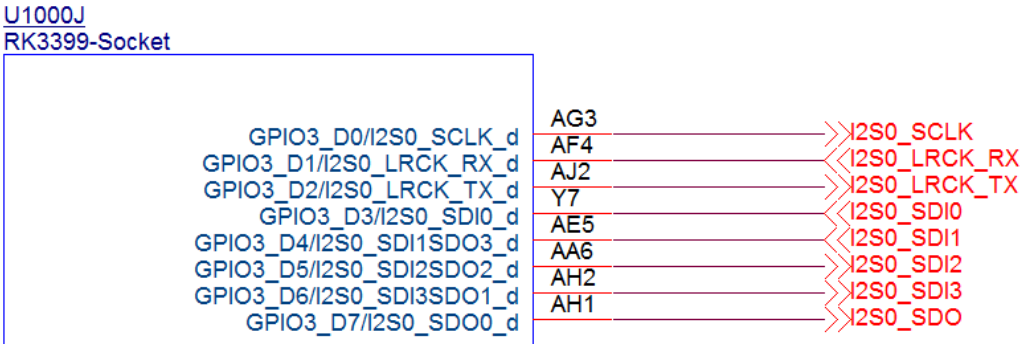



Figure 2–65 RK3399Pro I2S0 8 Channel Input and 2 Channel Output

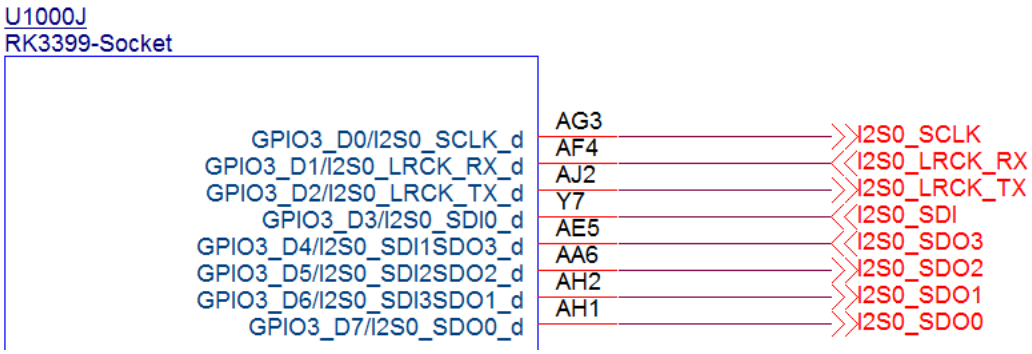



Figure 2–66 RK3399Pro I2S0 2 Channel Input and 8 Channel Output

I2S0 interface pull up/down and matching design are recommended as below table:

Table 2–20 RK3399Pro I2S0 Interface Design

| Name | Internal pull up/down | Connection method | Description(chip side) |
|---|---|---|---|
| I2S_CLK | Pull down | Series connect 22ohm resistor | I2S system clock output, supply for I2S0&I2S1 working |
| I2S0_SCLK | Pull down | Series connect 22ohm resistor | I2S0 bit clock output |
| I2S0_LRCK_TX/RX | Pull down | Series connect 22ohm resistor | I2S0 channel select input/output |
| I2S0_SDI0 | Pull down | Series connect 22ohm resistor | I2S0 data input channel 0 |
| I2S0_SDI1SDO3 | Pull down | Series connect | I2S0 data input channel 1/output |

| | | | |
|---|---|---|---|
| | | 22ohm resistor | channel 3 |
| I2S0_SDI2SDO2 | Pull down | Series connect 22ohm resistor | I2S0 data input channel 2/output channel 2 |
| I2S0_SDI3SDO1 | Pull down | Series connect 22ohm resistor | I2S0 data input channel 3/output channel 1 |
| I2S0_SDO0 | Pull down | Series connect 22ohm resistor | I2S0 data output channel 0 |

- **2.3.5.2 I2S1**

I2S1 supports 2 channels input and 2 channels output, and can be used as PCM interface. Connect to RK809 Codec I2S interface by default.

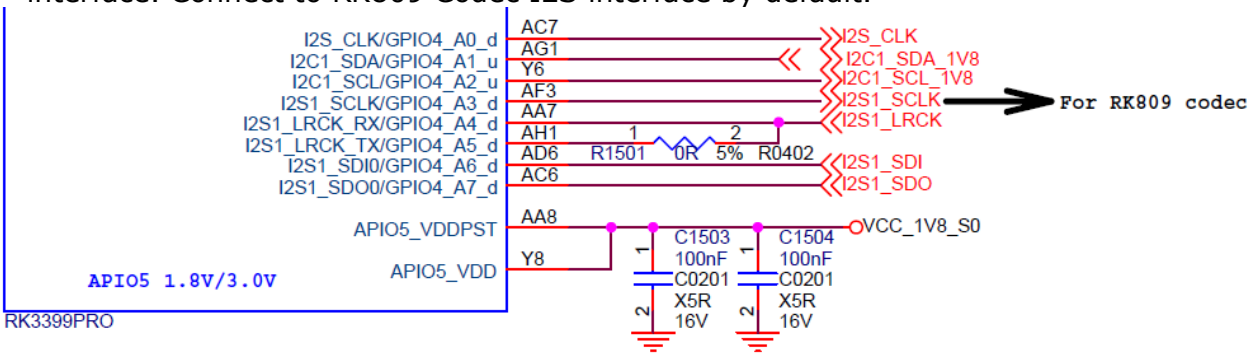



Figure 2–67 RK3399Pro I2S1 Module

I2S1 interface pull up/down and matching design are recommended as shown in below table:

Table 2–21 RK3399Pro I2S1 Interface Design

| Name | Internal pull up/down | Connection method | Description (chip side) |
|---|---|---|---|
| I2S1_SCLK<br>PCM_CLK | Pull down | Series connect 22ohm resistor | I2S1 bit clock output<br>PCM clock |
| I2S1_LRCK_TX/RX<br>PCM_SYNC | Pull down | Series connect 22ohm resistor | I2S1 channel select input/output<br>PCM data frame synchronous |
| I2S1_SDI0<br>PCM_IN | Pull down | Series connect 22ohm resistor | I2S1 data input channel 0<br>PCM data input |
| I2S1_SDO0<br>PCM_OUT | Pull down | Series connect 22ohm resistor | I2S1 data output channel 0<br>PCM data output |

- **2.3.5.3 Codec**

RK809-3 has embedded Codec, connected with RK3399Pro through I2S interface.

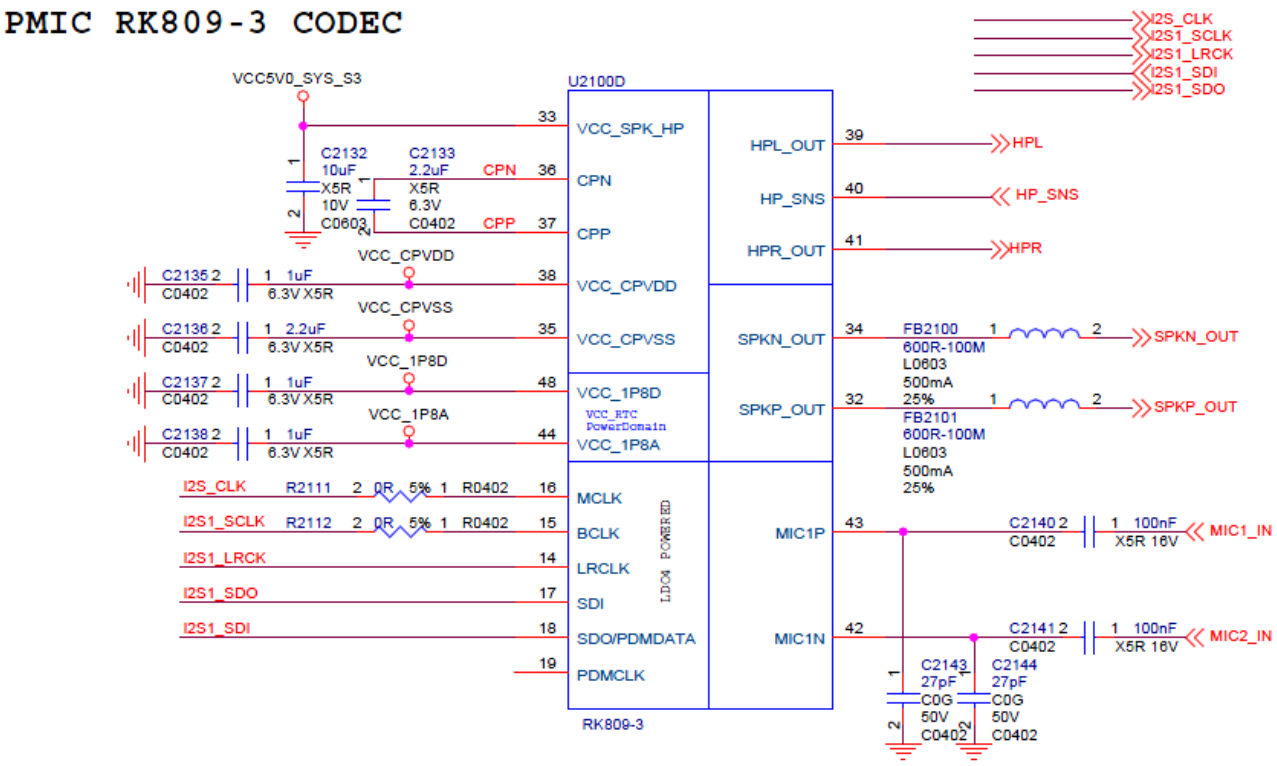



Figure 2–68 RK809-3 Codec Circuit

The HPSNS output from Codec is used as an internal Offset reference and needs to be connected to GND, which is connected with GND at the headset to reduce the level difference with the headphone GND. The traces should be accompanied in the middle of HPR/HPL to avoid the interference from other signals. If the Codec's GND is on the same complete GND plane as the headset GND, and the components layout is close, it can be connected directly to the GND plane.

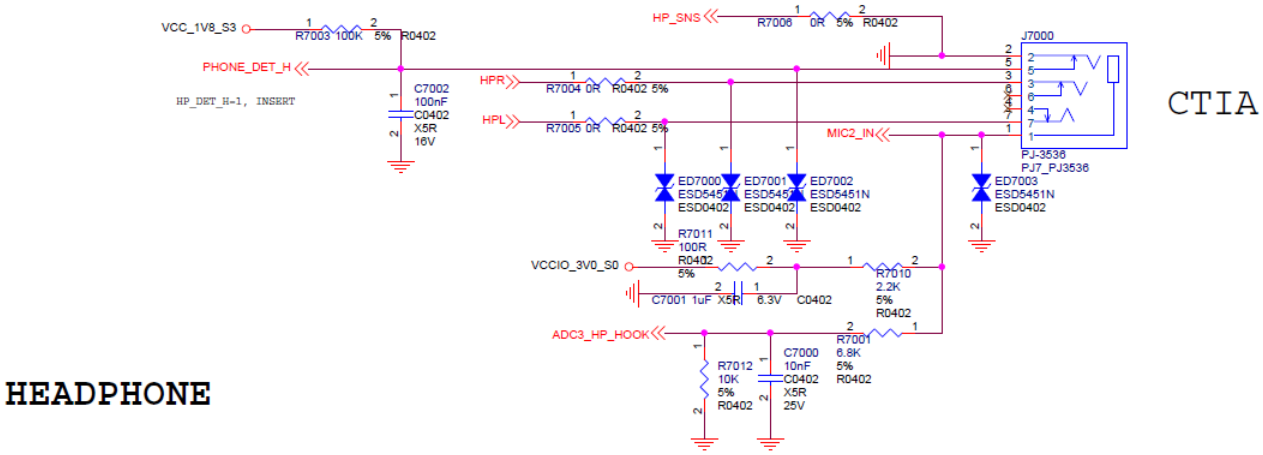



Figure 2–69 RK809-3 Headphone Circuit

Codec embedded Mono filter free speaker drive circuit can provide the drive strength of 1.3W@8ohm, which can meet the requirement of mono channel application with small power, the trace is simple, and can save the additional cost of external power amplifier.

# SPEAKER

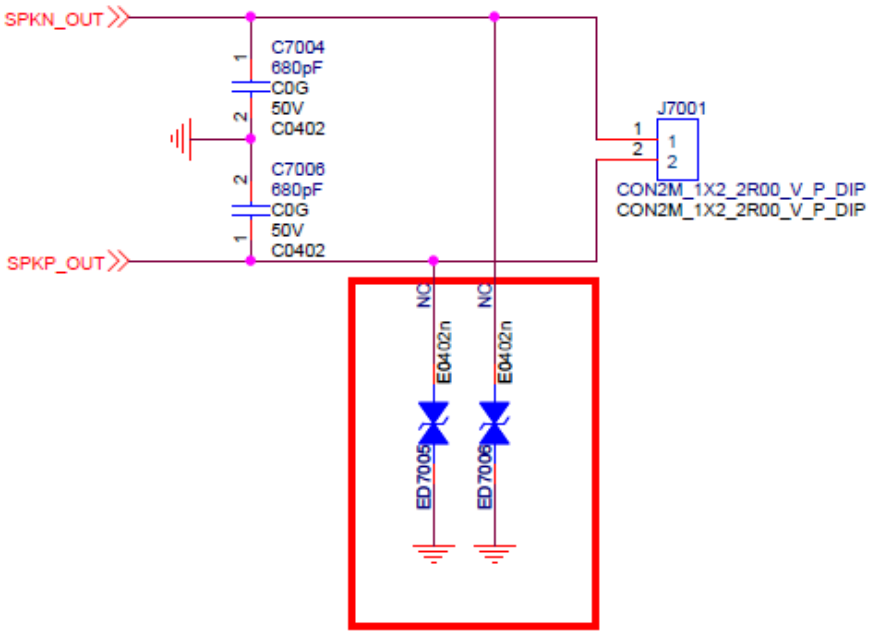



Figure 2–70 RK809-3 Speaker Circuit

When use the embedded power amplifier to do the mic array loop back, the recommended loop back circuit is as below, after voltage division and filter, output differential loop back signal to the audio ADC interface of RK809-3, complete A/D conversion by RK809-3 and then transmit back to RK3399Pro through I2S interface.

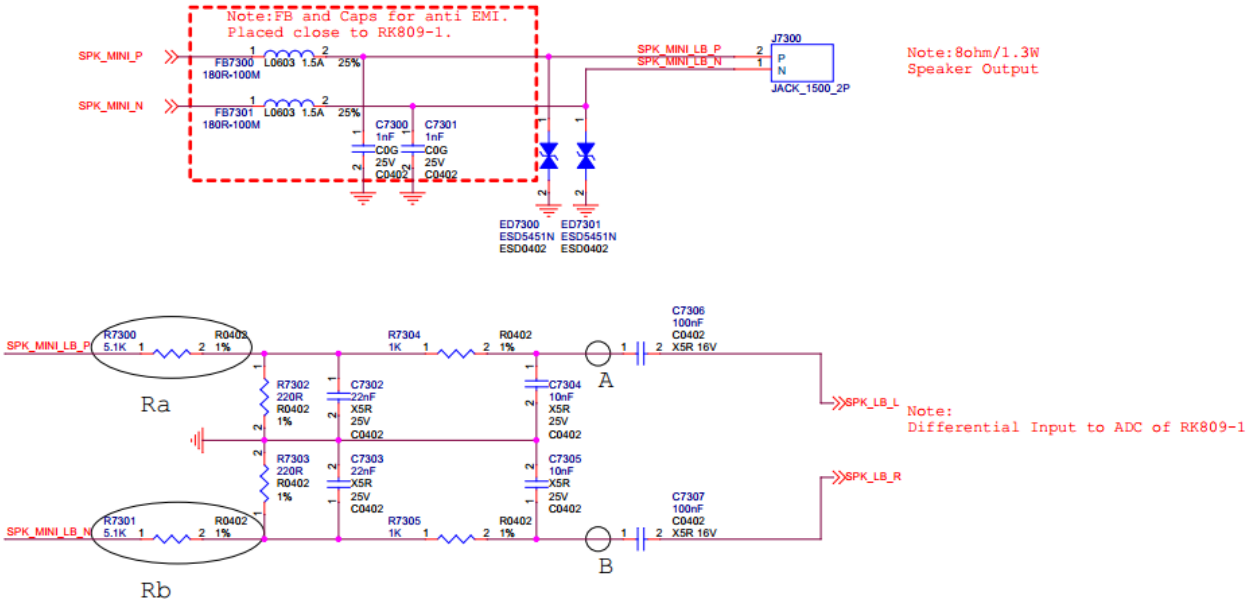



Figure 2–71 RK809-3 Speaker Circuit

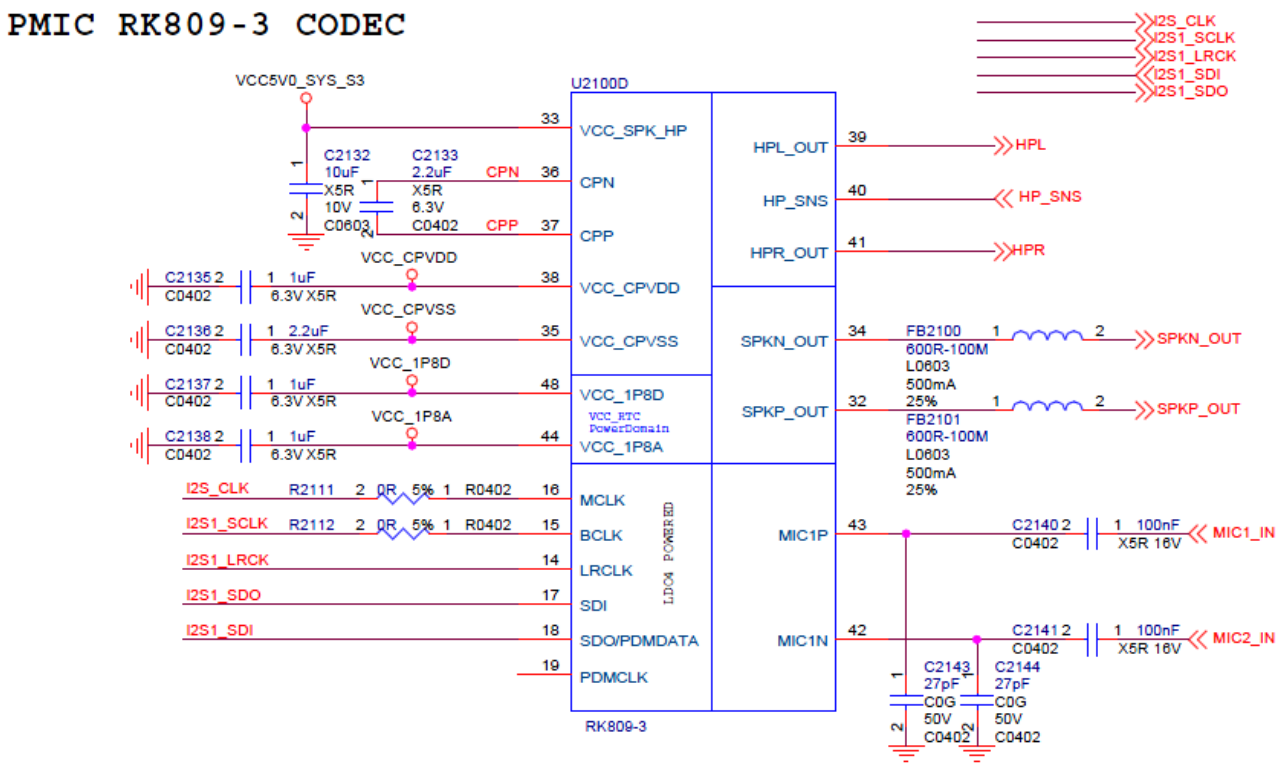



Figure 2–72 RK809-3 RK3399Pro Loop Back Path

If the embedded Mono speaker drive circuit of Codec cannot meet the drive strength requirement, external separate analog/digital power amplifier can be connected, and the loop back also can refer to the above circuit. Need to pay attention to that Ra\Rb resistance should be adjusted according to the output level of the separate power amplifier, to make the max level measured at A/B points is not bigger than the input limit value of ADC, which is recommended to be less than 500mV based on debugging status.

For Stereo requirement, ADC of RK809-3 should be configured as two channels of single-end input to meet the requirement of two channels of loop back. In order to be compatible with different types of power amplifier, the loop back collection point is place at LINEOUT side. Adjust according to the requirement of algorithm or use external ADC to do the loop back collection.

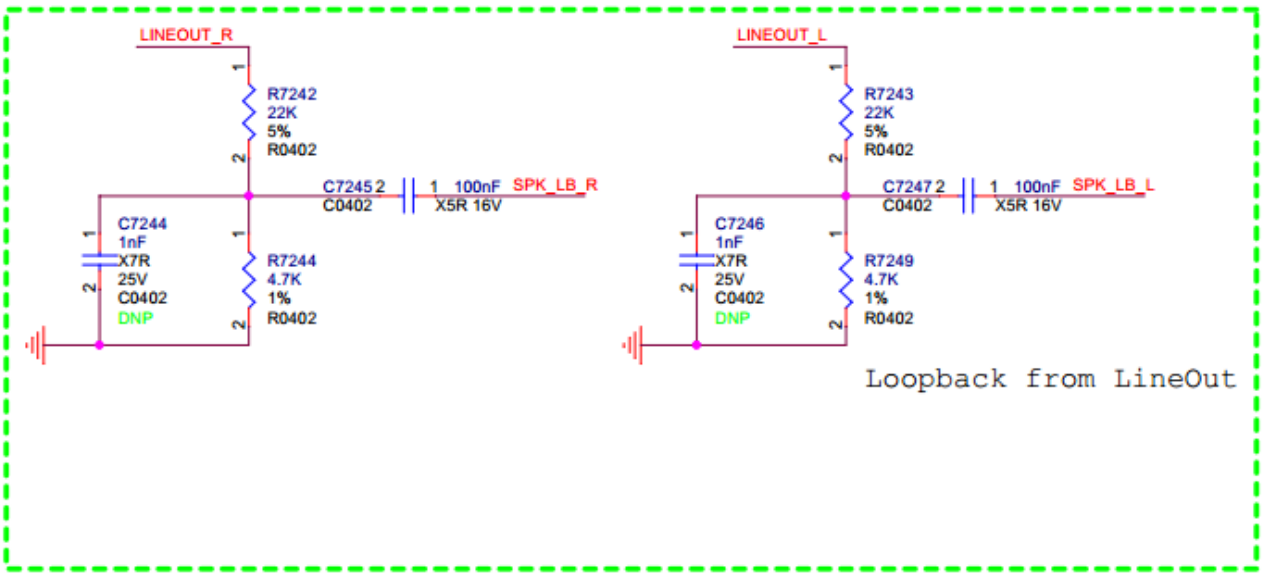



Figure 2–73 RK809-3 Stereo Loop Back

- **2.3.5.4 MIC**

MIC circuit is shown as Figure 3-64. Select appropriate voltage divider R7105 and R7106 according to the electret microphone specifications.

If use analog interface MEMS MIC, please refer to the recommended design circuit.

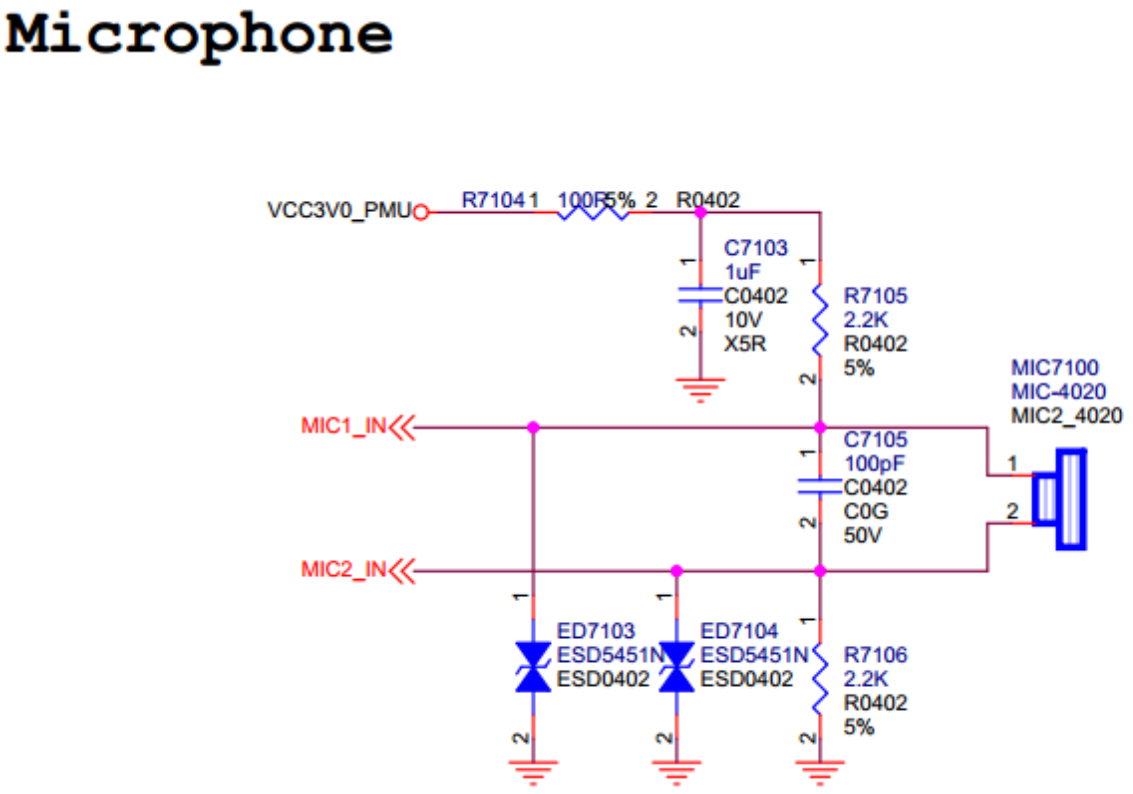



Figure 2–74 Differential Microphone

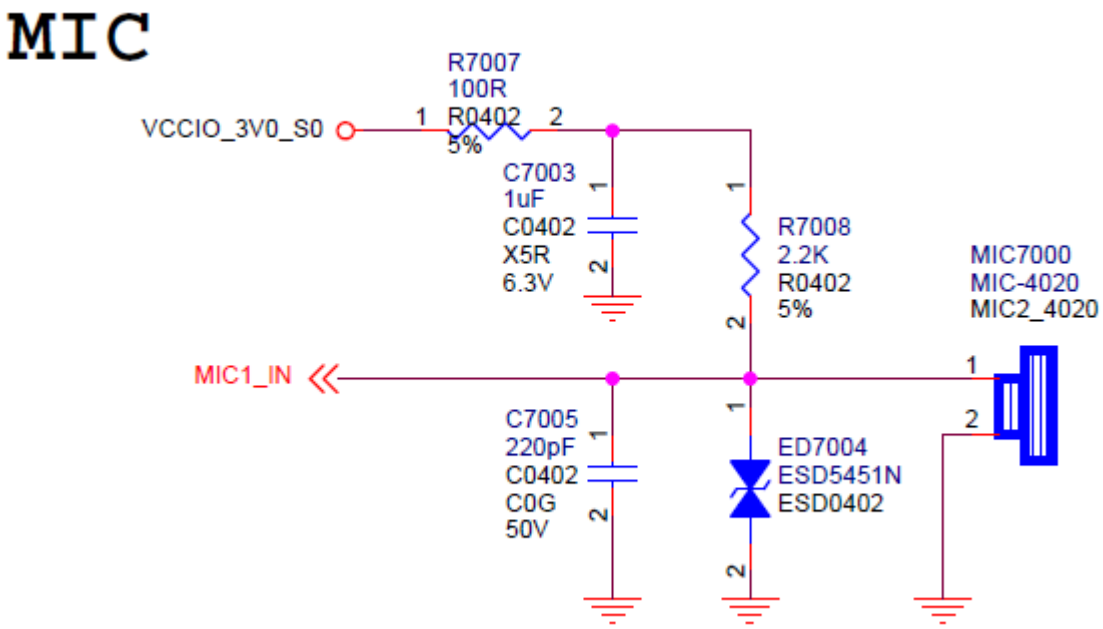



Figure 2–75 Single-end Microphone

If use digital interface MEMS, RK3399Pro only provides the analog microphone solution input by ADC. For the solution, need to place ADC close to the analog MIC, and convert the analog signal into digital signal as soon as possible for transmission to improve the anti-interference ability of the whole input path.

In multi-mic application, may connect multiple external ADC at the same time, need to note that the trace of I2S CLK should use Daisy Chain topology connection, shorten the branch of each node as much as possible, and both sides of the signal (especially CLK) should be surrounded by GND while routing and layout.

For the static electricity protection of analog mic, it is also useful to place ESD component close to MIC or series connect resistance with signal line.

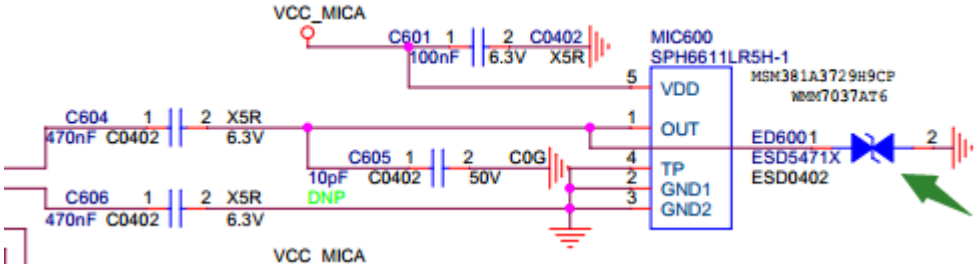



Figure 2–76 Analog Microphone

## 2.3.6 CPU Video Circuit

RK3399Pro has embedded video controller, supporting eDP/HDMI/MIPI-DSI three kinds of video output modes.

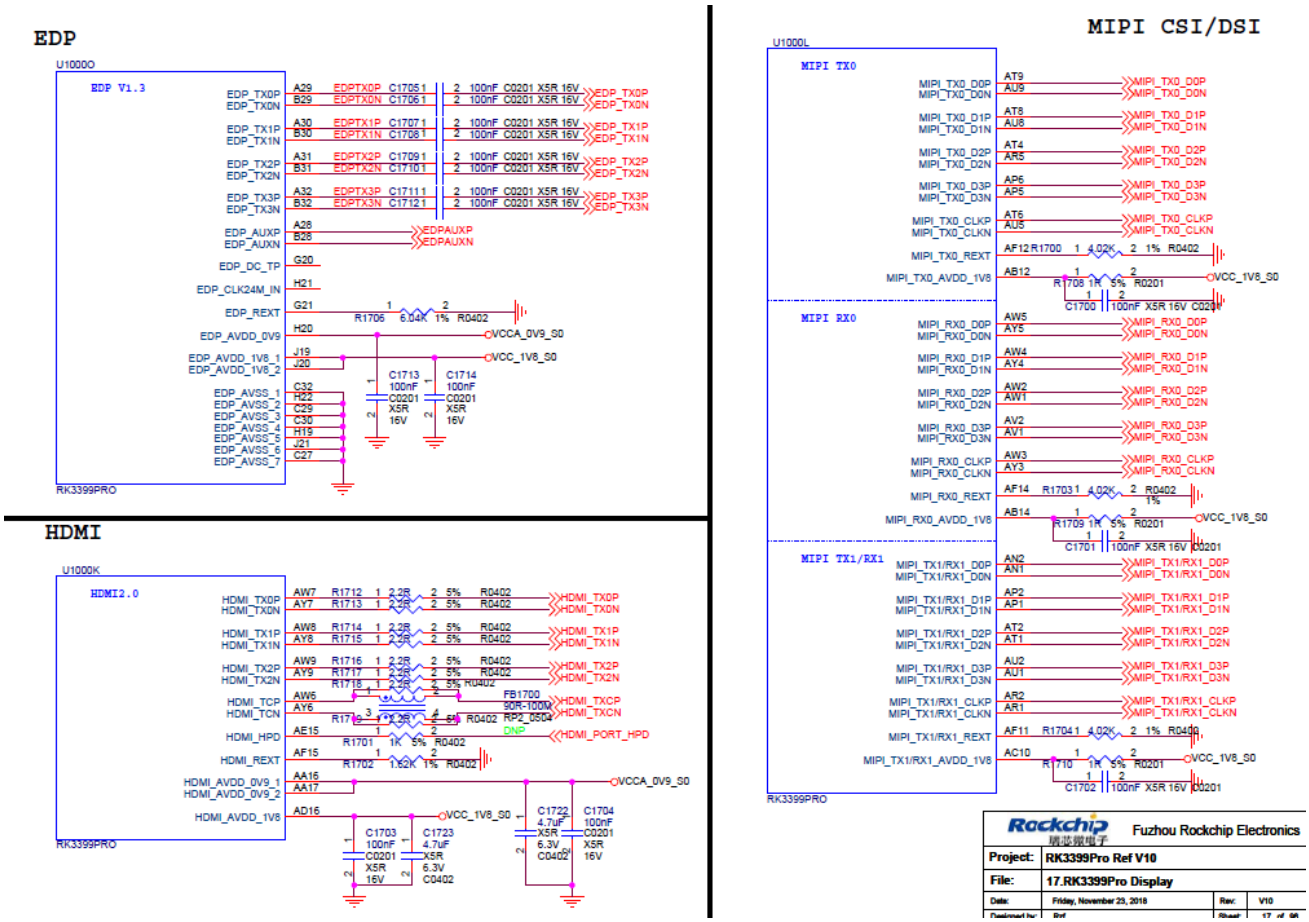



Figure 2–77 RK3399Pro Video Output Interface

### 2.3.6.1 eDP

- The reference resistor R1704 of eDP controller should select the resistor with 1% accuracy, and it will affect the signal quality of eye diagram.
- The coupling capacitor of EDP_TXn signal should be placed close to output side, that is connect side.

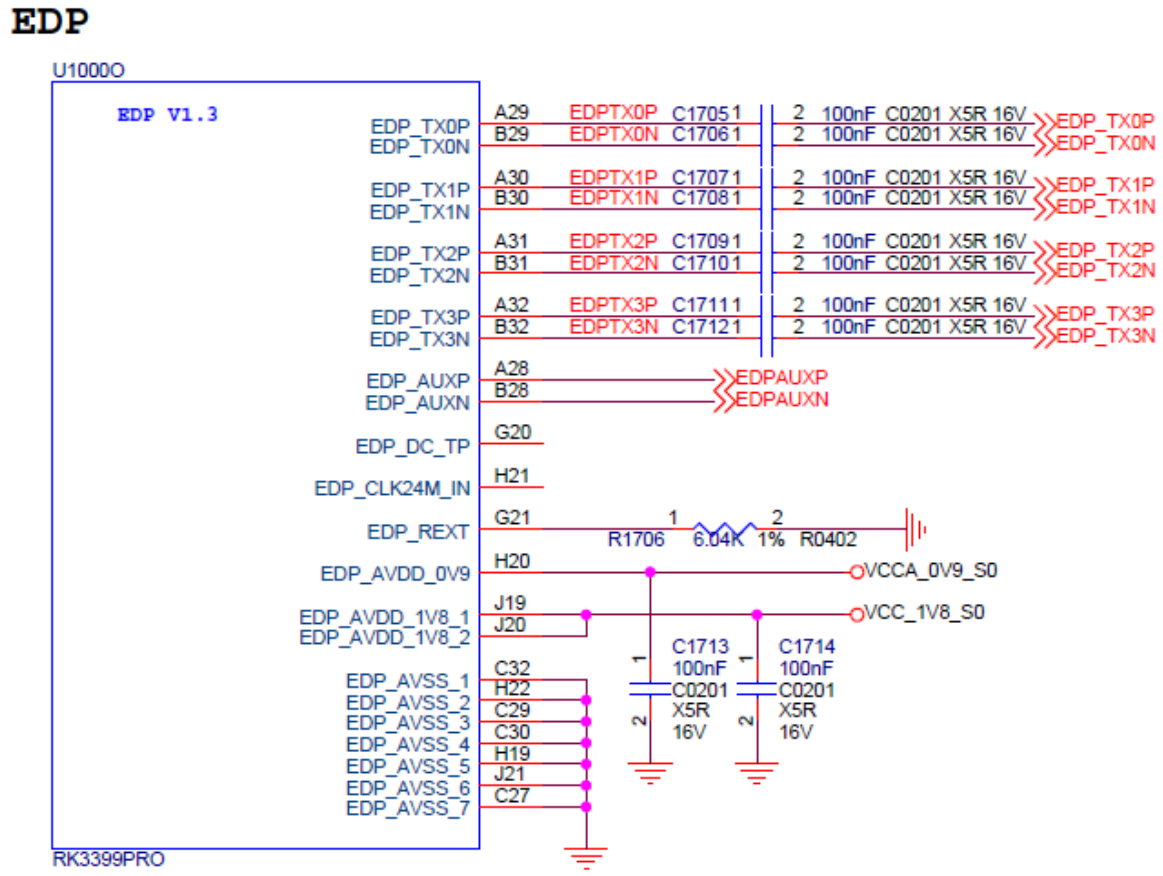



Figure 2–78 RK3399Pro eDP Module

- **2.3.6.2 HDMI OUT Mode**

  RK3399Pro provides an HDMI interface, supporting HDMI 2.0 protocol:

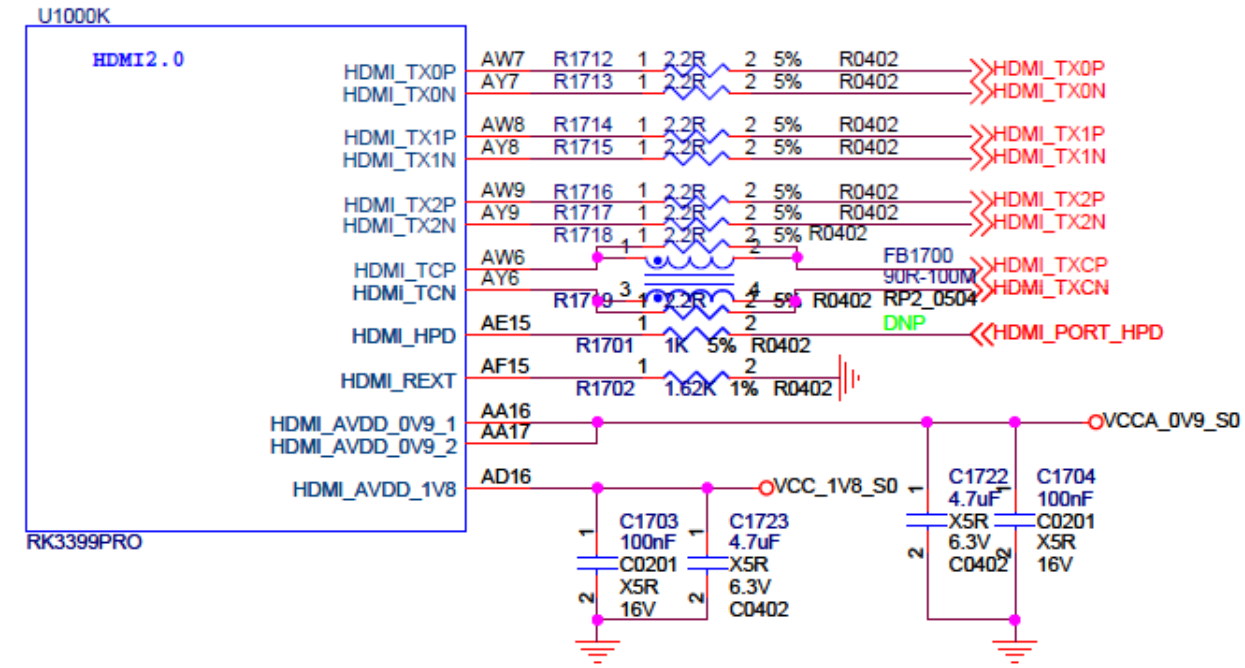



Figure 2–79 RK3399Pro HDMI Module

- The reference resistor R1702 of HDMI controller should select the resistor with 1% accuracy, and it will affect the signal quality of eye diagram.
- HDMI interface CEC circuit should pay attention to the level anti-irrigation design. For details, please refer to RK3399Pro reference design schematic.

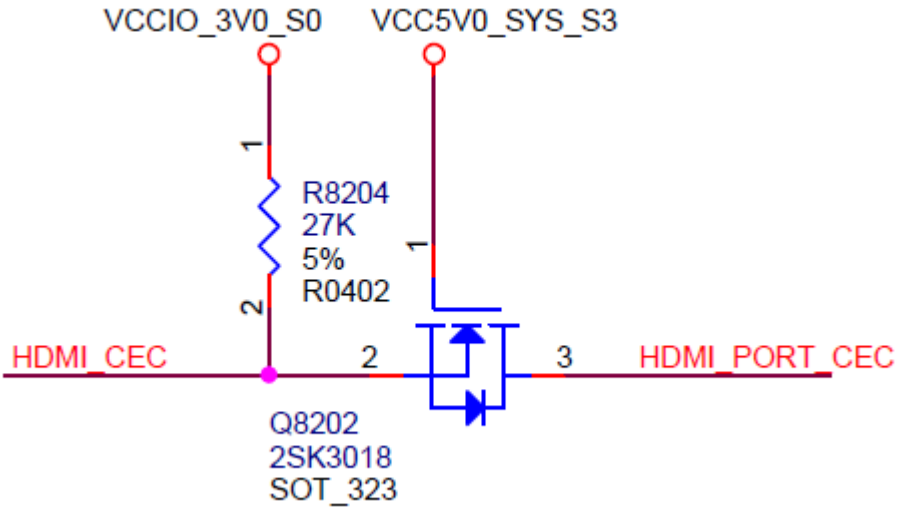



Figure 2–80 HDMI CEC Anti-irrigation Circuit

- RK3399Pro I2C doesn't support 5V, DDC/I2C bus need to add level conversion circuit.

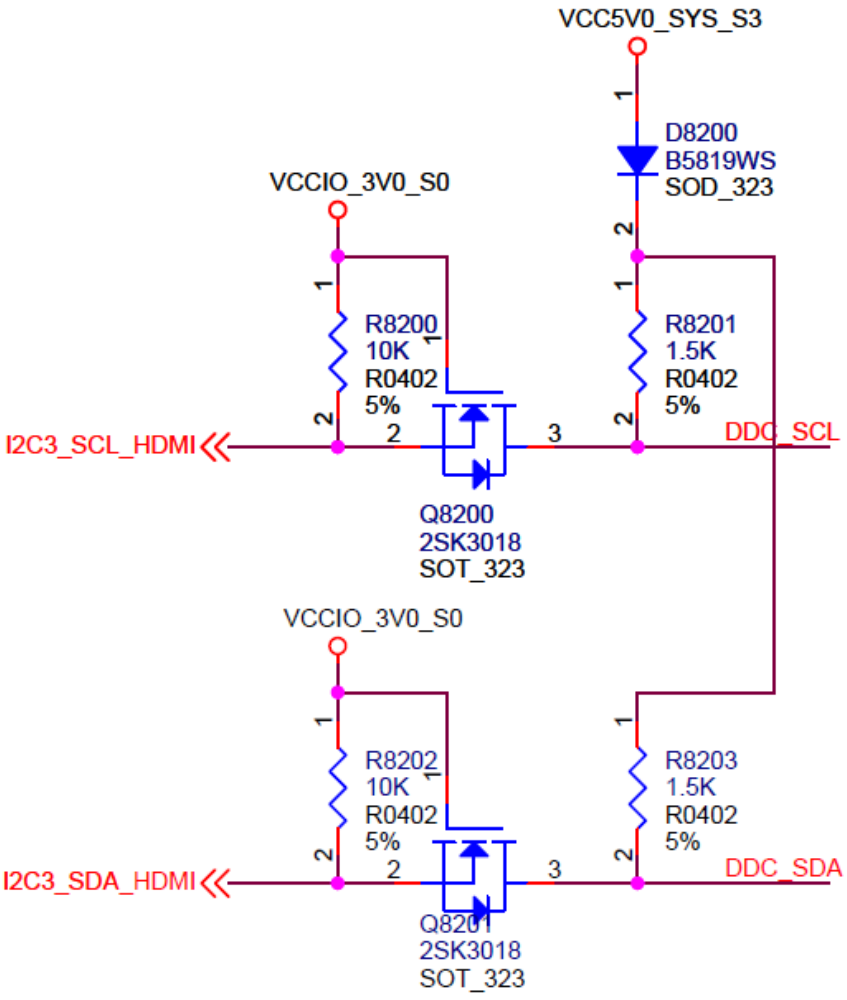



Figure 2–81 HDMI DDC Level-shift circuit

- The four groups of differential signals of HDMI need to have ESD protection. The ESD component should be placed close to HDMI port. The recommended capacitance should be less than 0.4pF.

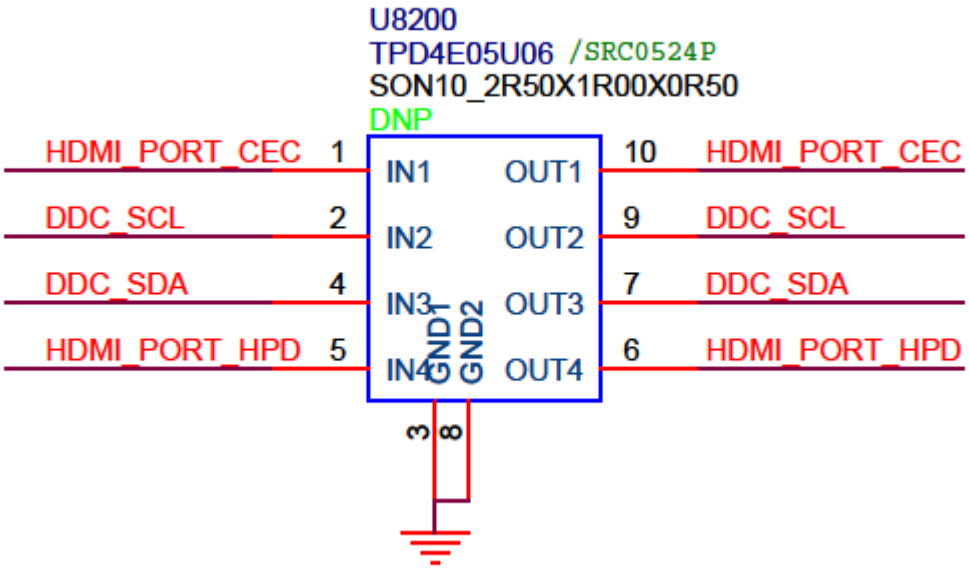



Figure 2–82 HDMI ESD protection

- **2.3.6.3 MIPI-DSI Mode**

RK3399Pro has 2 embedded MIPI-DSI controllers MIPI_DSI0 and MIPI_DSI1. MIPI_DSI1 multiplexed with MIPI_CSI1, so only one function can be used at the same time, and need to configure the corresponding input/output mode through software when used.

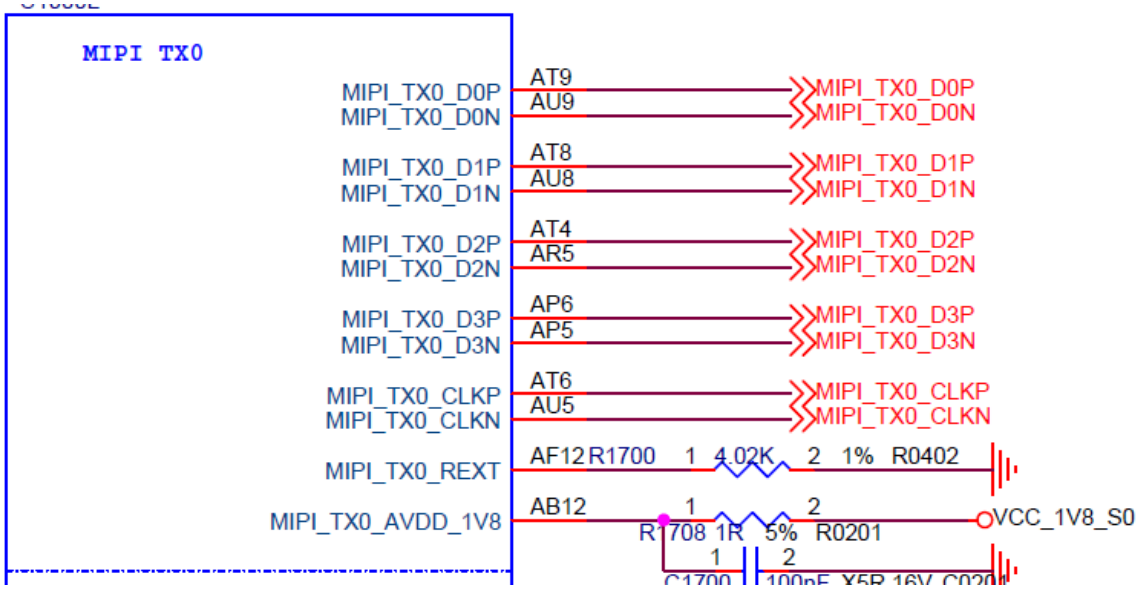



Figure 2–83 RK3399Pro MIPI-DSI0 Module

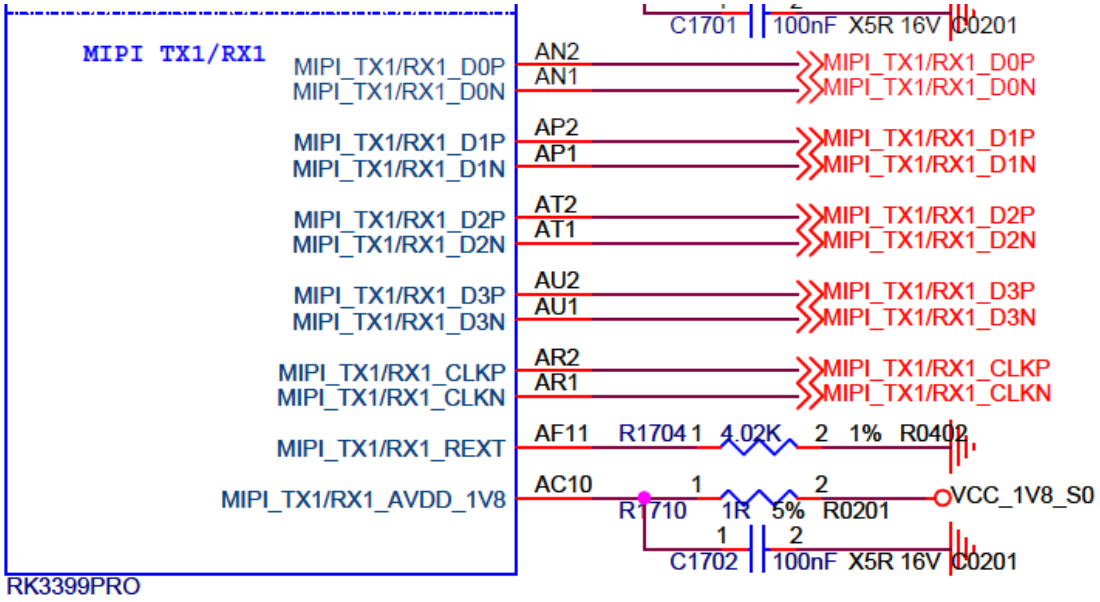



Figure 2–84 RK3399Pro MIPI-DSI1 Module

Please note for design:

- The reference resistor of MIPI-DSI controller should select the resistor with 1% accuracy, and it will affect the signal quality of eye diagram.

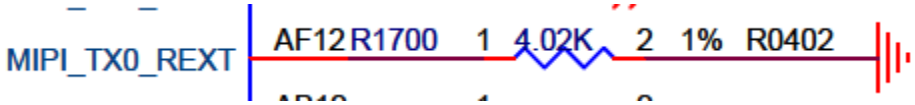



Figure 2–85 RK3399Pro MIPI-DSI0 Controller Reference Resistance

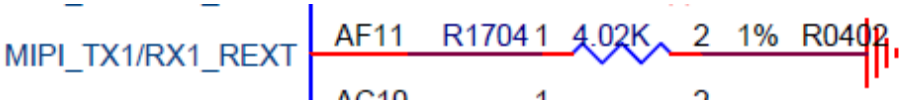



Figure 2–86 RK3399Pro MIPI-DSI1 Controller Reference Resistance

- In single MIPI output work mode, must use MIPI-DSI0 controller, that is MIPI_TX0 group, and MIPI-DSI1 cannot be used separately.
- In dual MIPI output work mode, MIPI TX0 and MIPI TX1/RX1 channels can be exchanged with the whole group according to the requirements of layout and routing.
- MIPI_TX_AVDD_1V8 and MIPI_TX/RX_AVDD_1V8 are the same power on chip package, so must use the same power supply. In order to avoid the damage of surge, 1.8V power of MIPI controller needs to series connect 1ohm resistor.

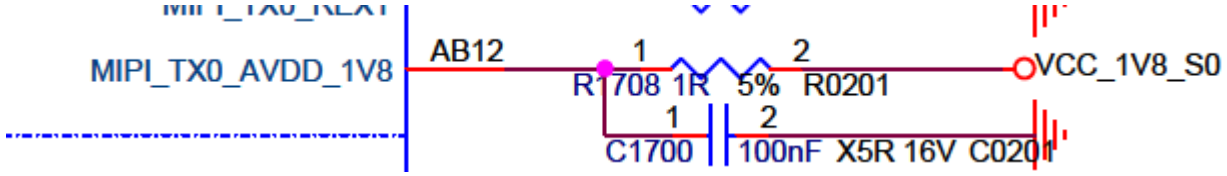



Figure 2–87 RK3399Pro MIPI-DSI0 Power Supply

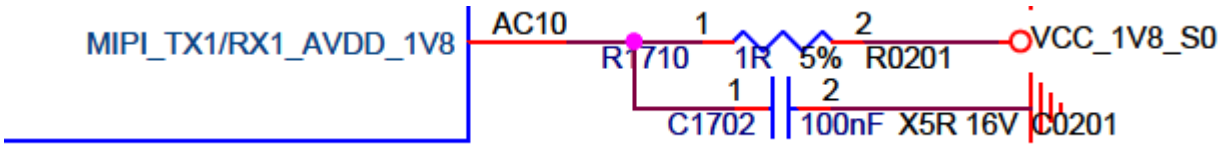



Figure 2–88 RK3399Pro MIPI-DSI1 Power Supply

- In order to improve MIPI performance, the coupling capacitor of the controller power should be placed close to the pin.

## 2.3.7 CPU Camera Circuit

- **2.3.7.1 USB CAMERA**

  For USB CAMERA, please refer to the USB design method in section 2.3.3

- **2.3.7.2 MIPI CSI**

RK3399Pro has two embedded MIPI-CSI controller MIPI_CSI0 and MIPI_CSI1, both embedded ISP processor, can be used at the same time for dual MIPI input. MIPI_CSI1 multiplexed with MIPI_DSI1, so only one function can be used at the same time and need to configure the corresponding input/output mode through software before using.

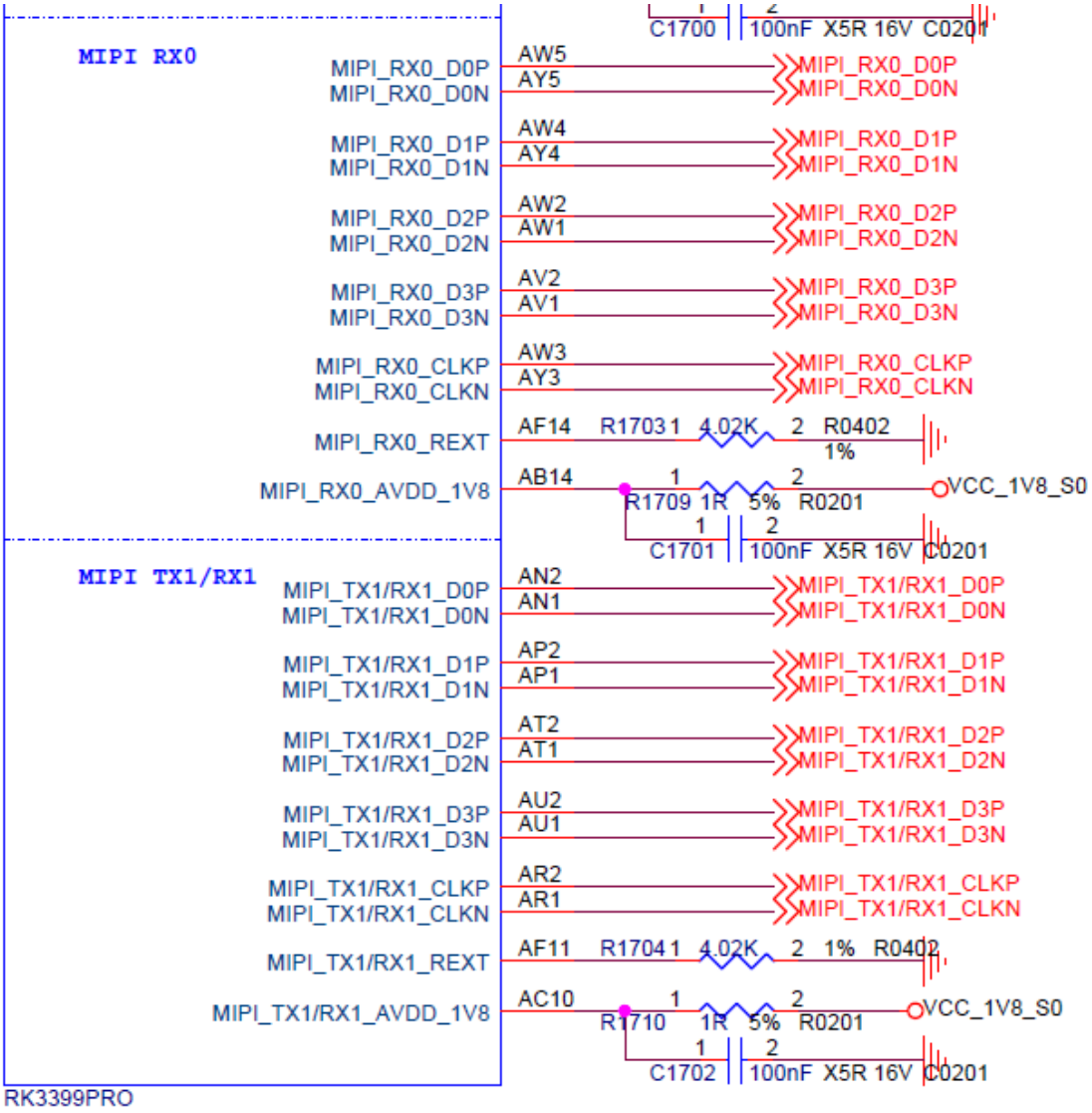



Figure 2–89 RK3399Pro MIPI-CSI Module

Please note for design:

- The reference resistor of the controller should select the resistor with 1% accuracy, and it will affect the signal quality of eye diagram.


Figure 2–90 RK3399Pro MIPI-CSI0 Controller Reference Resistance

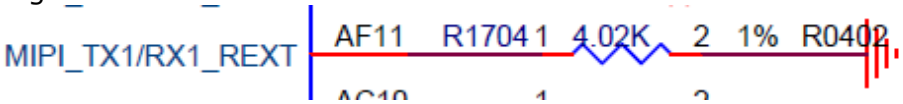



Figure 2–91 RK3399Pro MIPI-CSI1 Controller Reference Resistance

- In order to avoid the damage of surge, the power of MIPI-CSI controller needs to series connect 1ohm resistance.

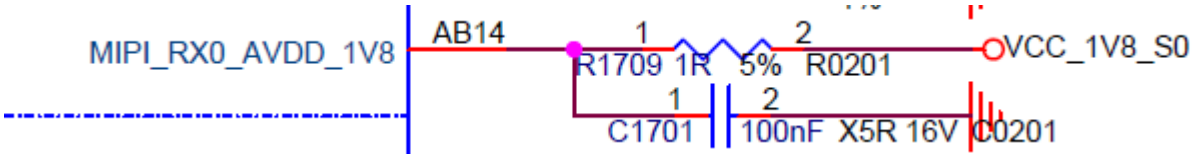



Figure 2–92 RK3399Pro MIPI-CSI0 Power Supply

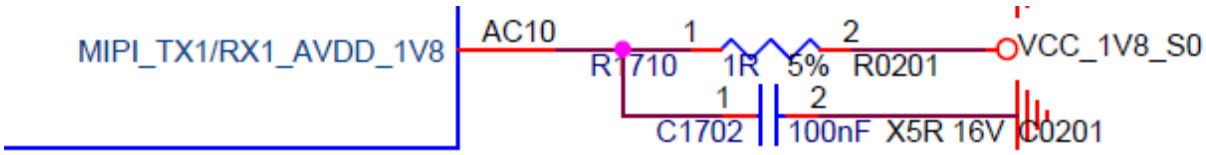



Figure 2–93 RK3399Pro MIPI-CSI0 Power Supply

- In order to improve MIPI-CSI performance, the coupling capacitor of the controller power should be placed close to the pin.

- **2.3.7.3 CIF CAMERA**

APIO2_VDD is the power domain of CIF interface, and it can support 1.8V and 2.8V. Please select the corresponding power supply for IO (1.8V or 2.8V) in the application according to the actual needs. Be noted that I2C pull-up level must be consistent with it otherwise the camera would not work normally.

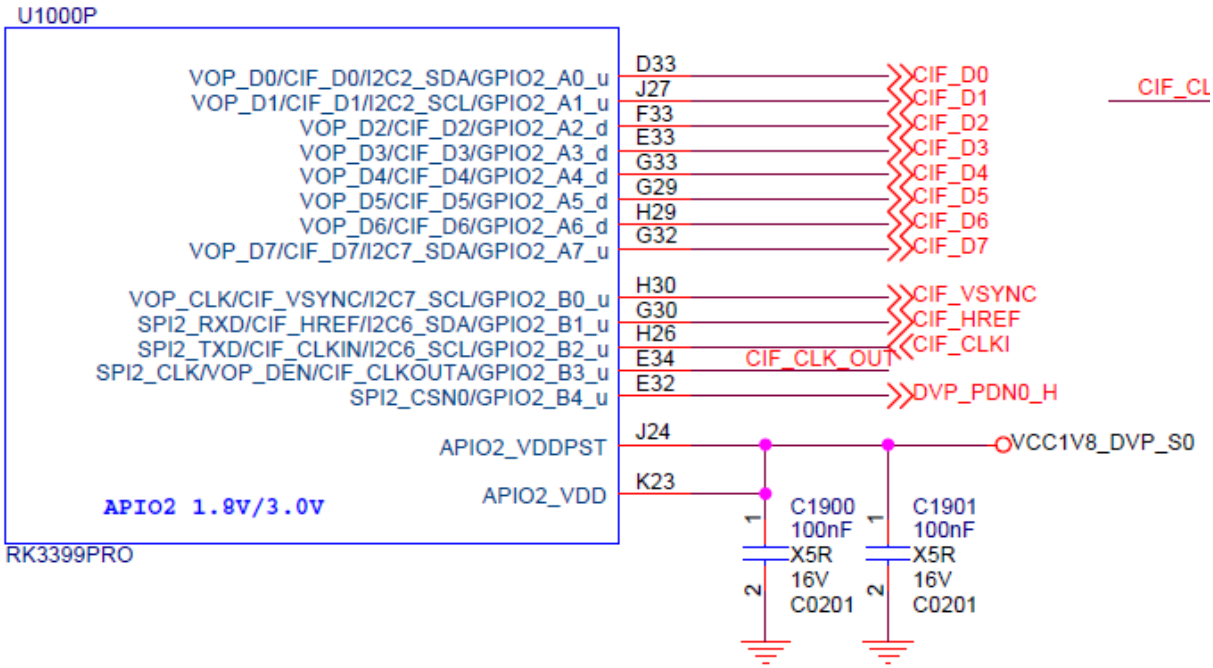



Figure 2–94 RK3399Pro CIF Module

## 2.3.8 CPU ADC Circuit

RK3399Pro uses ADC_IN2 of SARADC as the sampling port of key value input and multiplexed with Recovery mode button (no need to update LOADER) as shown below. If the system already has images, pull down ADKEY_IN when system boots up, keep ADC_IN2 level as 0V, then RK3399 will enter Rockusb flashing mode. When PC recognizes the USB device, release the button to make ADC_IN2 back to high level (1.8V), then the firmware can be downloaded to SOC.

Note

*Tablet, BOX and VR products all use this upgrading method, while Netbook uses EC flashing which requires the servoboard flashing tool.*

RK3399Pro SARADC sampling range is 0-1.8V and the accuracy is 10bits. The key array is in parallel, and the key value can be adjusted by adding or reducing the key and tunning the proportion of the divider resistor to accomplish the multiple-key input to meet the customers' product requirements. It is recommended that the values between any two keys must be bigger than +/-35, that is the central voltage difference must be bigger than 123mV.

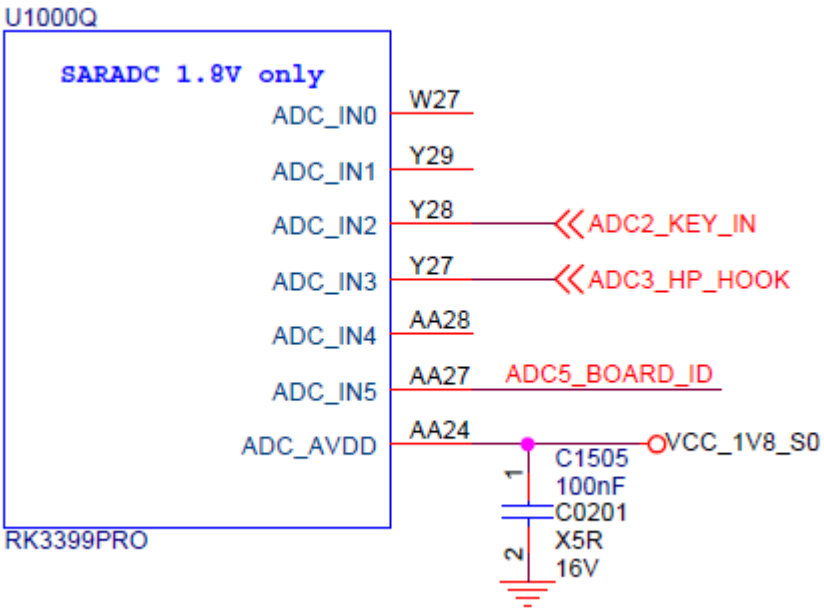



Figure 2–95 RK3399Pro SAR-ADC Module

### 2.3.9 CPU SDIO/UART Circuit

RK3399Pro supports SDIO 3.0 interface WIFI/BT module as shown below. It should be noted that the SDIO and UART controllers's power supply is 1.8V when using WIFI/BT modules with SDIO and UART interfaces, so IO level of the modules must also support 1.8V.

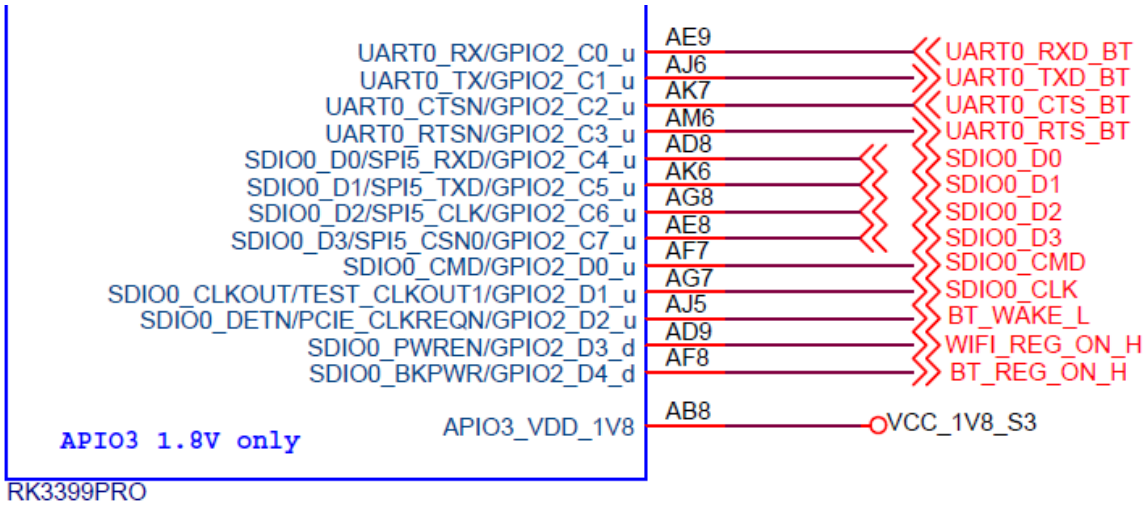



Figure 2–96 RK3399Pro SDIO/UART Module

- **2.3.9.1 SDIO**

SDIO interface pull up/down and matching design are recommended as below table:

Table 2–22 RK3399Pro SDIO Interface Design

| Name | Internal pull up/down | Connection method | Description (chip side) |
|---|---|---|---|
| SDIO0_DQn[0:3] | Pull up | Series connect 22ohm resistor can be deleted if the trace is short | SDIO data output/input |
| SDIO0_CLK | Pull down | Series connect 22ohm resistor | SDIO clock output |
| SDIO0_CMD | Pull down | Series connect 22ohm resistor can be deleted if the trace is short | SDIO command output/input |

- **2.3.9.2 UART**

UART interface pull up/down and matching design are recommended as below table:

Table 2–23 RK3399Pro UART Interface Design

| Name | Internal pull up/down | Connection method | Description (chip side) |
|---|---|---|---|
| UART0_RX | Pull up | Direct connection | UART1 data input |
| UART0_TX | Pull up | Direct connection | UART1 data output |
| UART0_CTSn | Pull up | Direct connection | UART1 permission output signal |
| UART0_RTSn | Pull up | Direct connection | UART1 request output signal |

### 2.3.10 CPU UART Debug Circuit

RK3399Pro Debug UART2 is reused with SDMMC interface, and you can externally connect UART-to-USB conversion board for debugging when needed.

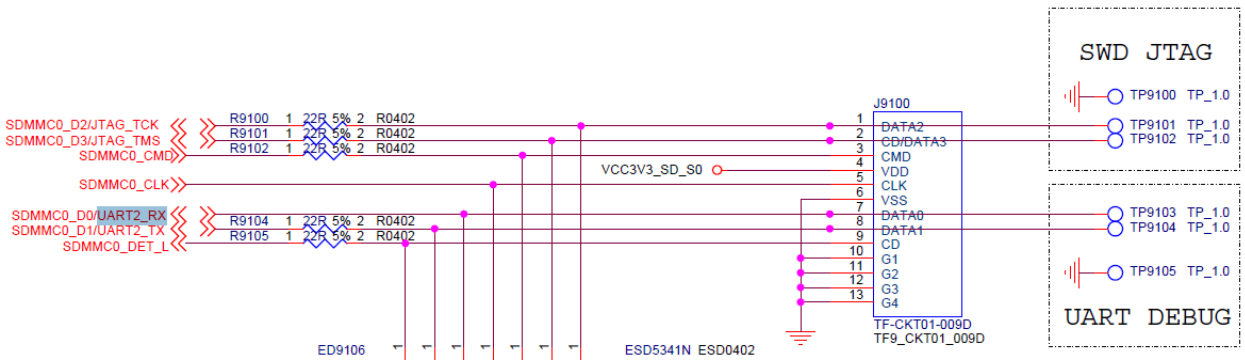



Figure 2–97 RK3399Pro UART2 Reuse Relationship

Please select the port number of the board which is connected to PC, the baud rate selects 1.5M, and Flow control RTS/CTS doesn't need to select. If PC embedded DB-9 port doesn't

support high speed mode, please use the USB-to-serial port conversion method.

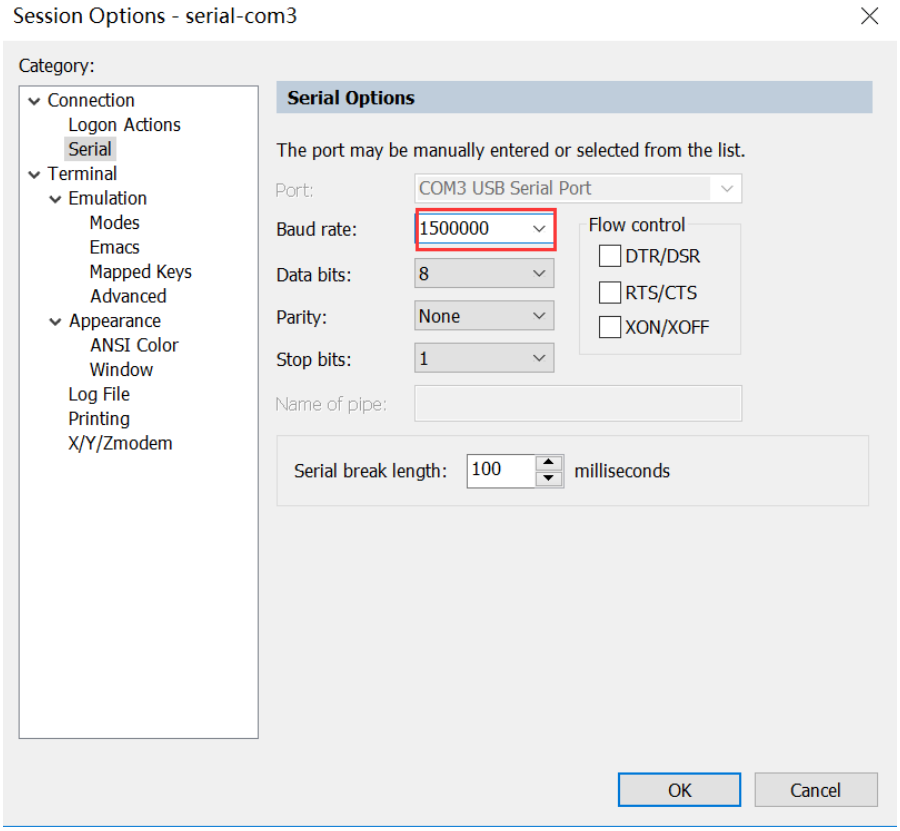



Figure 2–98 RK3399Pro Serial Port Configuration

### 2.3.11 CPU Digital Audio Circuit

SPDIF is the abbreviation for Sony/Philips Digital Interface Format, which is referred to SONY and PHILIPS digital audio interface. The SPDIF is divided into two kinds of coaxial and optical fiber, in fact, the transmitted signal is the same, but the carrier is different, the interface and connector appearance are also different. But the optical signal transmission does not consider the interface level and impedance problems, and the interface is flexible and the anti-interference ability is stronger.

RK3399Pro provides a SPDIF output interface, support maximum 24bits interpretation. The maximum transmission rate of optical fiber SPDIF connector determines the highest sampling rate of SPDIF. If the maximum transmission rate of optical fiber SPDIF connector is 16Mbps, the sampling rate can only reach 96 KHz. The sampling rate would support 192 KHz only when the optical fiber SPDIF connector supports 25Mbps.

The optical fiber SPDIF output circuit is shown as below. The signal traces need to be accompanied by ground traces.

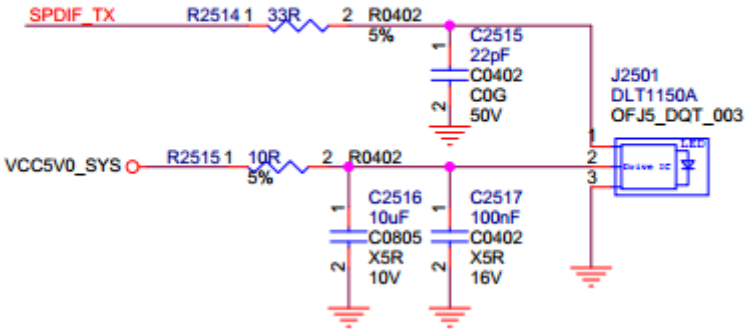



Figure 2–99 SPDIF Using Optical Fiber

The digital audio output coaxial interface circuit is shown as below. The signal traces need to be separated by coupling capacitors, otherwise there is a risk of buring the chip when the device end level doesn't match.

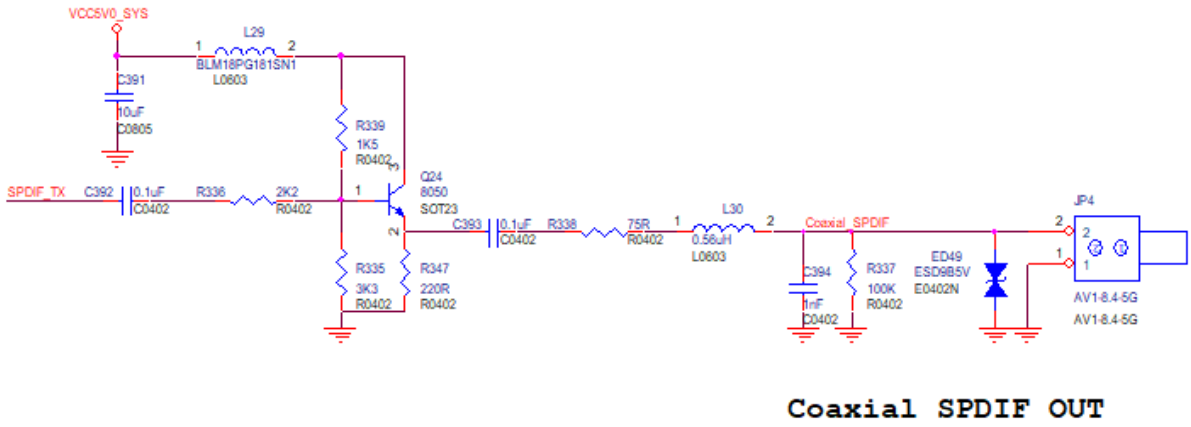



Figure 2–100 SPDIF Using Coaxial

### 2.3.12 CPU PCIe Circuit

PCIe is the abbreviation for PCI-Express. It is the latest bus and interface standard. RK3399Pro CPU supports PCIe V2.1 protocol and has the following features:

- Support Root Complex（RC）and End Point（EP）
- Support 4x/2x/1x mode, respectively have 4 pairs of TX and RX differential lines.
- Signal data channel supports signal transmission rate up to 2.5GTb/s, with 8b/10b form, so the maximum signal rate is 250MB/s.
- Work in full-duplex mode, and support data transmission rate up to 10GTb/s, that is 1GB /s.
- Support spread Spectrum Clock, SSC

The analog power PCIE_AVDD_0V9 and PCIE_AVDD_1V8 are RK3399Pro CPU PCIe controller's power supply. Recommend to power up PCIE_AVDD_0V9 earlier than PCIE_AVDD_1V8.

# PCIE

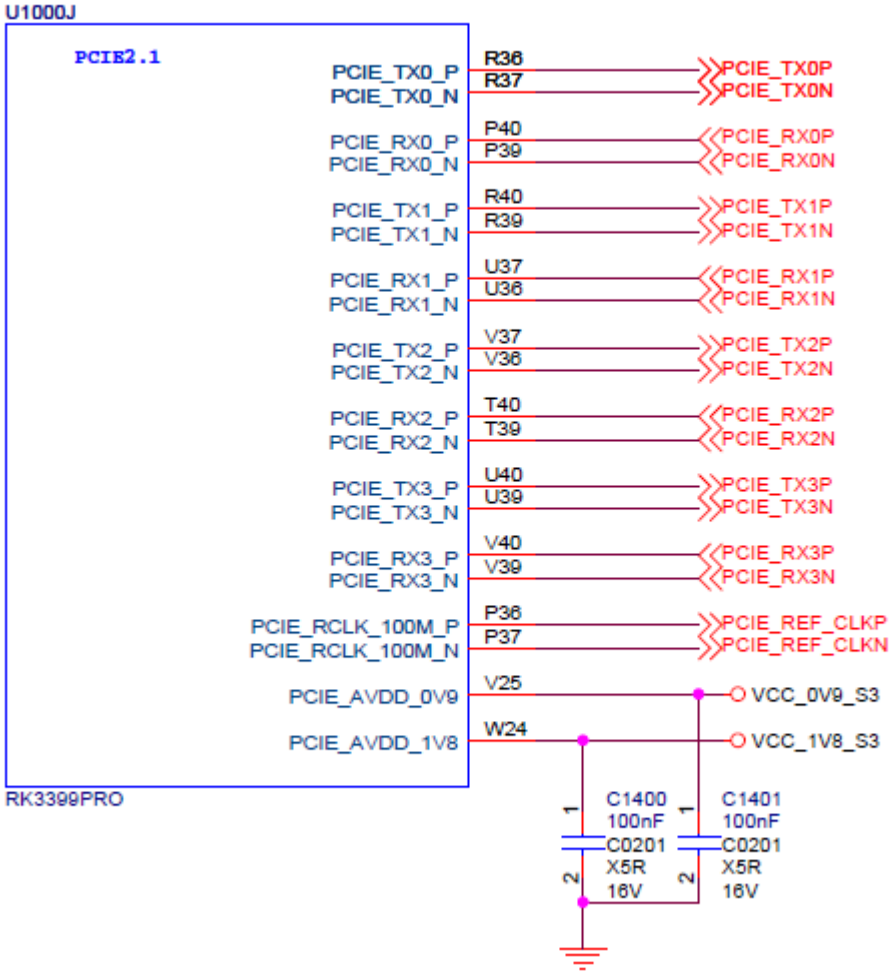



Figure 2–101 RK3399Pro PCIe Module

- The coupling capacitor of TX signal should be placed close to PCIe connector. RX capacitor is provided by device end.

❑ A bulk decoupling capacitor (greater than 10 µF) is recommended on each power supply used within a device on the add-in card. This bulk decoupling capacitor should be in close proximity to the add-in card device.

Figure 2–102 PCIe JEDEC Coupling Capacitor Place Requirement

- In the application, please pay attention to the PCIe device power supply. If it is SSD storage, the power consumption is relatively high; while the power consumption of network card devices is relatively low.

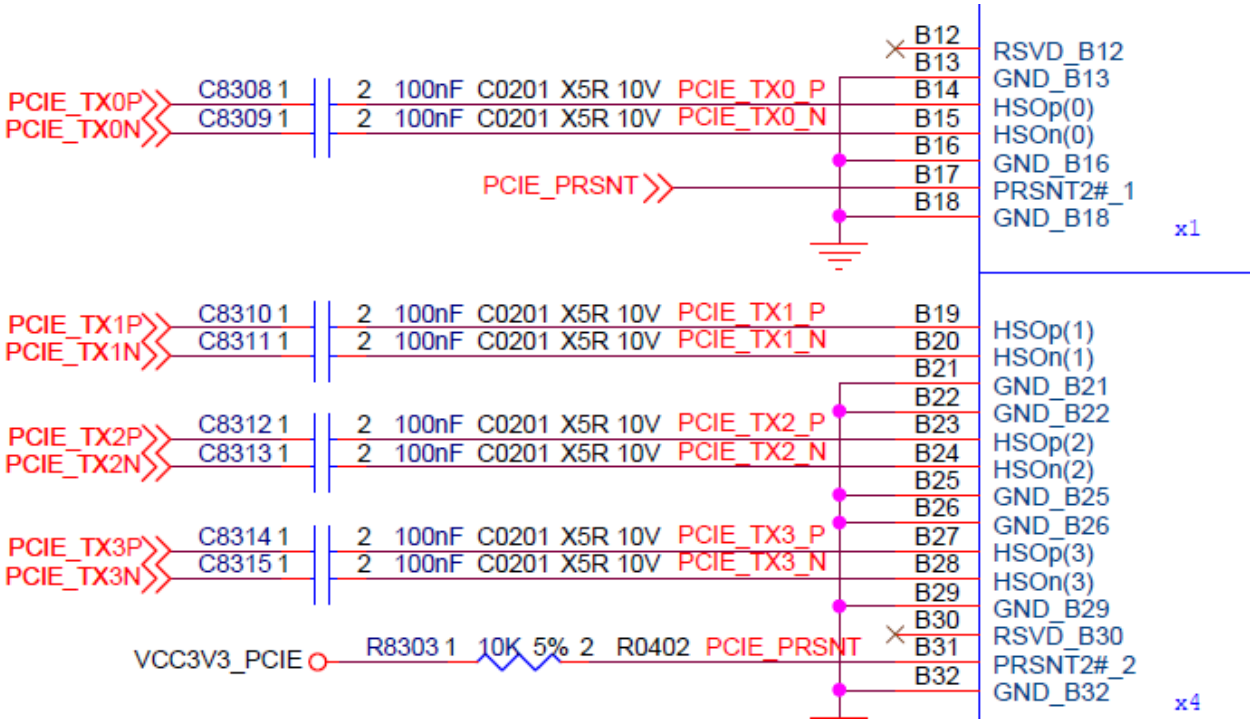



Figure 2–103 PCIe TX Coupling Capacitor

# 3 NPU Schematic Design Recommendation

## 3.1 NPU Minimum System Design

### 3.1.1 NPU Clock Circuit

RK3399Pro NPU clock is separated from CPU PLL frequency and no need to connect external crystal as shown below:

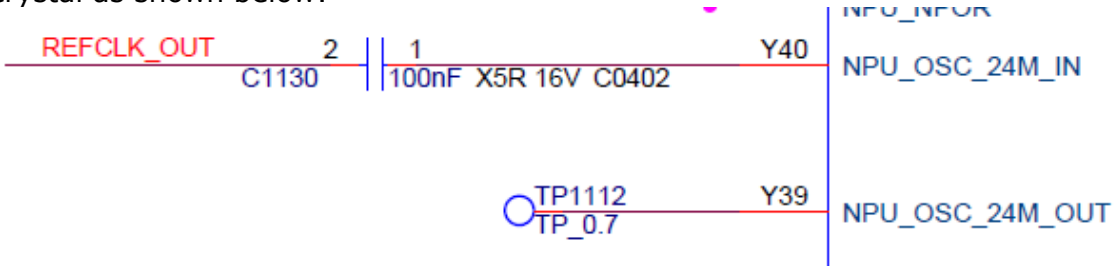



Figure 3–1 RK3399Pro NPU Crystal Connection Method and Component Parameter

When RK3399Pro NPU is in standby mode, it will switch the internal clock source to PVTM separated from the internal PLL frequency, and automatically generate the 32.768KHz clock to reduce the system clock frequency so as to lower down the system power consumption. The clock isn't provided externally as shown below:


Figure 3–2 RK3399Pro NPU Standby Clock Input

The clock parameters of the external 32.768KHz RTC are shown in below table:

Table 3–1 RK3399Pro NPU 32.768KHz Clock Requirement

| Parameter | Specification | | | Description |
|---|---|---|---|---|
| | Min. | Max. | Unit | |
| Frequency | 32.768000 | | kHz | |
| Frequency Tolerance | +/-30 | | ppm | Frequency tolerance |
| Work Temperature | -20 | 70 | ℃ | |
| Duty Ratio | 50 | | % | |

### 3.1.2 NPU Reset Circuit

RK3399Pro internally integrates POR (Power on Reset) circuit, effective with low level, and C1100 is used for debouncing, please place it close to RK3399Pro. To make the chip stable and work normally, the shortest reset time required is 100 times of 24MHz main clock cycles, that is at least 4us.

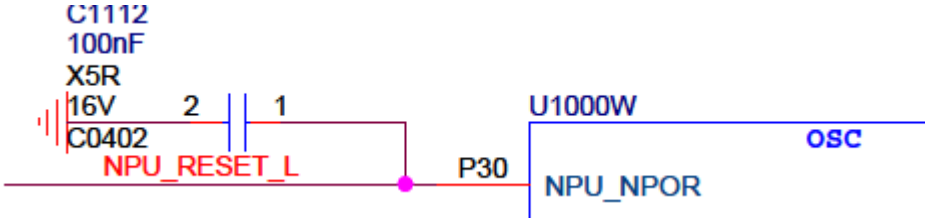



Figure 3–3 RK3399Pro NPU Reset Input

### 3.1.3 NPU System Boot Load Sequence

RK3399Pro NPU system boot load sequence priority from high to low is:

- SPI FALSH
- USB OTG

### 3.1.4 NPU System Initialization Configuration Signal

The OSC configuration pin of RK3399Pro NPU is an important signal which needs to be configured before powering up. In application, select t

PU clock input source through this pin.

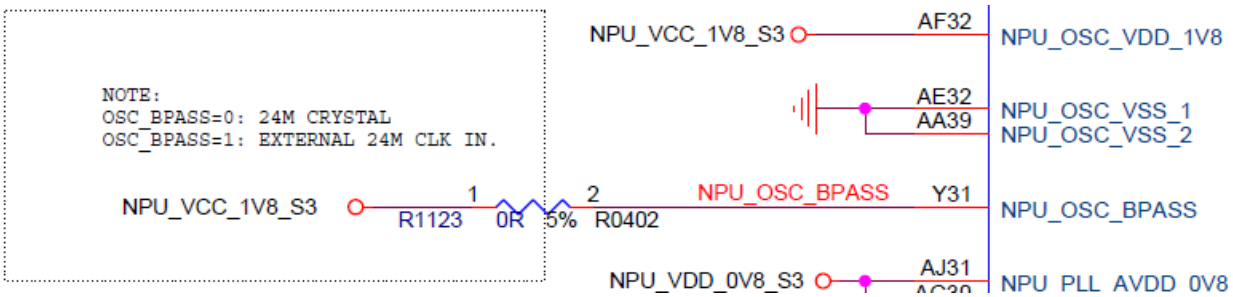



Figure 3–4 RK3399Pro NPU PMUIO2 Power Domain Level Configuration Pin

The configuration method of this pin is shown in below table.

Table 3–2 RK3399Pro NPU System Initialization Configuration Signal Description

| Signal name | Internal pull up/down | Description |
|---|---|---|
| NPU_OSC_BPASS | Pull down | NPU OSC selection pin:<br>0: system 24MHz crystal clock (default)<br>1: external 24MHz clock input. |

### 3.1.5 NPU JTAG Debug Circuit

RK3399Pro NPU JTAG interface is compliant with IEEE1149.1 standard. PC can be connected with DSTREAM emulator by SWD mode (two-line mode) to debug Core within the SoC.

JTAG interface is described as below table:

Table 3–3 RK3399Pro NPU JTAG Debug Interface Signal

| Name | Description |
|---|---|
| JTAG_TCK | JTAG clock input, recommend to pull down. |
| JTAG_TMS | JTAG mode selection input, recommend to pull up. |

### 3.1.6 NPU DDR Circuit

- **3.1.6.1 DDR Controller Introduction**

RK3399Pro NPU DDR controller interface is compliant with JEDEC SDRAM standard, and the controller has the following features:

- Support DDR3/DDR3L/LPDDR3 etc. standards.
- Provide a 32bit DDR controller interface, the controller interface separately provides 2 CS and 2 ODT, support data bus bit width, support the address bus up to 16bit.
- Support DDR size up to 4GB.
- Support Power Down, Self Refresh etc. low power consumption modes.

- **3.1.6.2 DDR Topological Structure and Connection Method**

Take LPDDR3 as an example, RK3399Pro SDRAM topological structure is shown as below:

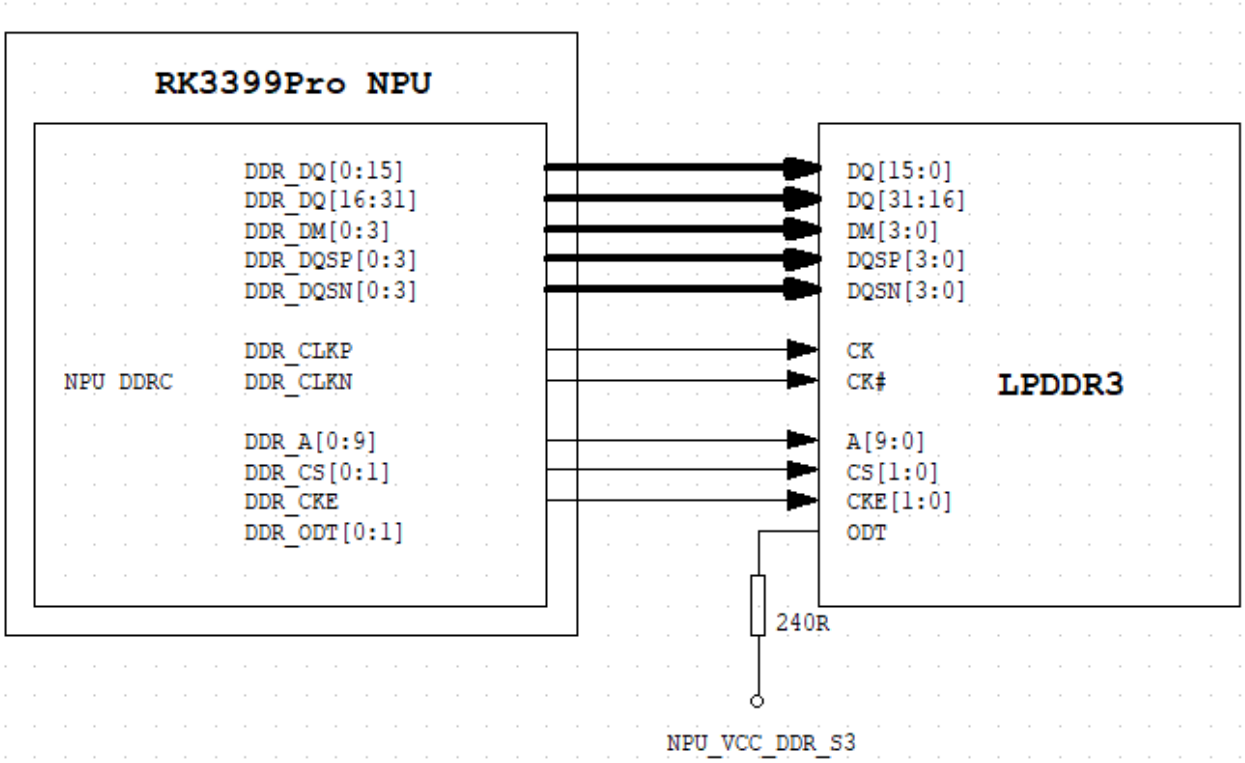



Figure 3–5 RK3399Pro NPU LPDDR3 Topological Structure

- **3.1.6.3 DDR Power Up Sequence Requirement**

RK3399Pro NPU DDR controller has two groups of power supply:

- NPU_VCC_DDR: supply power for DDR controller Core, interface I/O and buffer
- NPU_VREFO_DDR: DDR controller internal reference power output, can supply for VREF_DQ and VREF_CA of component end.

SDRAM component includes two groups of power supply, and for the power-up sequence please refer to respective JEDEC standards:

DDR3 SDRAM power-up sequence is shown as below:

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

OR

   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

Figure 3–6 DDR3 SDRAM Power-up Sequence

LPDDR3 DRAM power-up sequence is shown as below:

| After... | Applicable Conditions |
|---|---|
| Ta is reached | $V_{DD1}$ must be greater than $V_{DD2}$—200mV |
| | $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDCA}$—200mV |
| | $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDQ}$—200mV |
| | $V_{Ref}$ must always be less than all other supply voltages |

Figure 3–7 LPDDR3 SDRAM Power-up Sequence

- **3.1.6.4 DDR Support List**

The maximum operating frequency of RK3399Pro NPU DDR interfaces DDR3/LPDDR3 is up to 800MHz. For the approved components, please refer to 《Rockchip DDR Support List》 document released by Rockchip which can be downloaded from redmine through below link:

https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

### 3.1.7 NPU SPI Circuit

- **3.1.7.1 SPI Controller Introduction**

RK3399Pro NPU has a SPI controller which can be used to connect SPI device as boot. SPI controller power supply NPU_VCCIO5 will affect the system boot, so the power supply must be always on even if SPI controller is not used. SPI_CSN also cannot be pulled down.

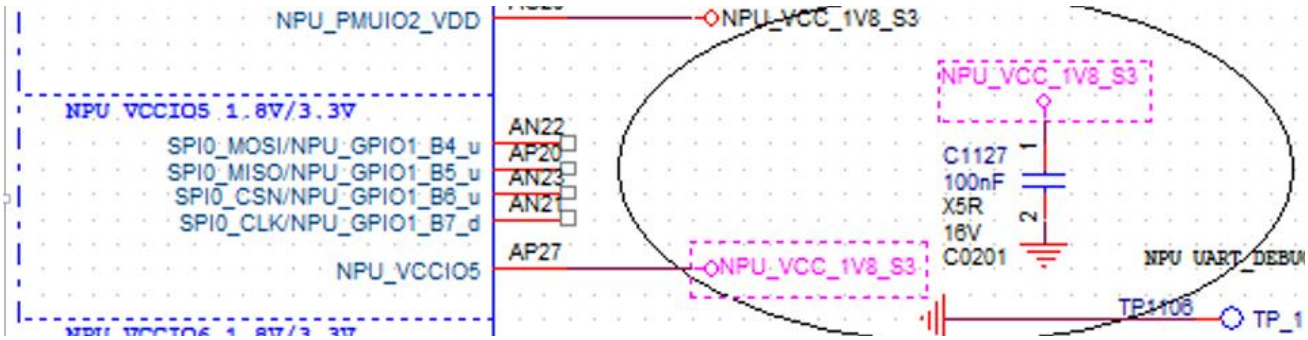



Figure 3–8 RK3399Pro NPU SPI Controller Power Supply

- **3.1.7.2 SPI Topological Structure and Connection Method**

SPI interface pull up/down and matching design are recommended in below table:

Table 3–4 RK3399Pro NPU SPI Interface Design

| Name | Internal pull up/down | Connection method | Description (chip end) |
|---|---|---|---|
| SPI0_MOSI | Pull up | Direct connection | SPI data output |
| SPI0_MISO | Pull up | Direct connection | SPI data input |
| SPI0_CSN | Pull up | Direct connection | SPI chip selection signal |
| SPI0_CLK | Pull down | Series connect | SPI clock output |

| | | | |
|---|---|---|---|
| | | 22ohm resistor | |

- **3.1.7.3 SPI Power-up Sequence Requirement**

SPI controller power-up sequence requirement should comply with the requirement of GPIO power domain power-up sequence, and must supply power constantly.

SPI Flash component only has one power, so there is no requirement on power-up sequence.

### 3.1.8 NPU GPIO Circuit

RK3399Pro NPU has two kinds of GPIO:

- 1.8V only, configure fixed 1.8V level.
- 1.8V/3.3V, can configure 1.8V or 3.3V level.

- **3.1.8.1 GPIO Drive Strength**

RK3399Pro NPU provides different drive strength and operating frequency ranges for different GPIOs:

Table 3–5 RK3399Pro NPU GPIO Drive Strength

| Power domain | GPIO type | I/O frequency @1.8V | I/O frequency @3.0V | Support drive strength type | Default drive strength |
|---|---|---|---|---|---|
| NPU PMUIO1 | 1.8V only | 150MHz | N/A | 2mA,4mA,8mA,12mA | 2mA |
| NPU PMUIO2 | 1.8V/3.3V | 150MHz | 50MHz | 2mA,4mA,8mA,12mA | 2mA |
| NPU VCCIO5 | 1.8V/3.3V | 150MHz | 50MHz | 2mA,4mA,8mA,12mA | 4mA |
| NPU VCCIO6 | 1.8V/3.3V | 150MHz | 50MHz | 2mA,4mA,8mA,12mA | 8mA |

- **3.1.8.2 GPIO Power**

The power pin of GPIO power domain is described as below:

Table 3–6 RK3399Pro NPU GPIO Power Pin Description

| Power domain | GPIO type | Pin name | Description |
|---|---|---|---|
| NPU PMUIO1 | 1.8V only | NPU_PMU_VDD_0V8 | 0.8V power for this domain (group of) GPIO. |
| | | NPU_PMUIO1_VDD_1V8 | 1.8V post drive for this domain (group of) GPIO. |
| NPU PMUIO2 | 1.8V/3.3V | NPU_PMUIO2_VDD | 1.8V or 3.3V power for this domain (group of) GPIO. |
| NPU VCCIO5 | 1.8V/3.3V | NPU_VCCIO5 | 1.8V or 3.3V power for this domain (group of) GPIO. |
| NPU VCCIO6 | 1.8V/3.3V | NPU_VCCIO6 | 1.8V or 3.3V power for this domain (group of) GPIO. |

Please follow the power rule as below in different applications:

- **1.8V only (PMUIO1 and APIO3 power domain)**

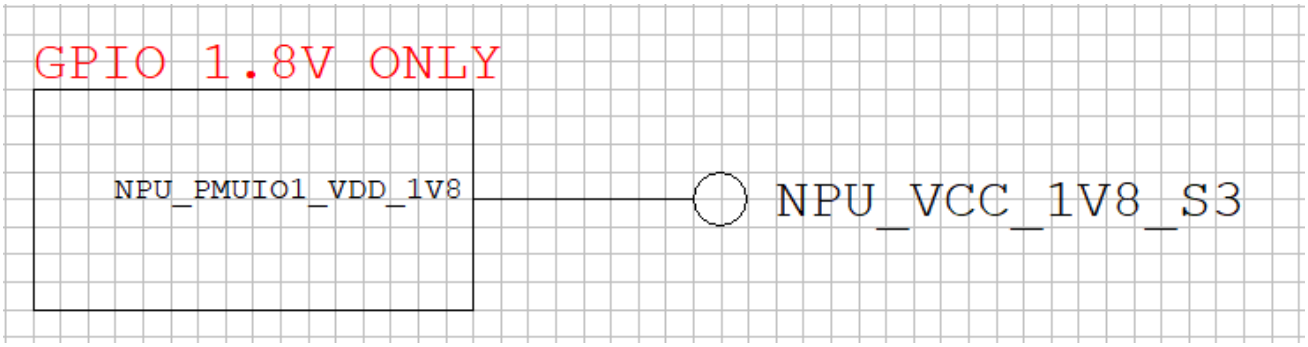



Figure 3–9 RK3399Pro NPU GPIO 1.8V only Power Setting

- **1.8V/3.3V at 1.8V mode (PMUIO2, VCCIO5 and VCCIO6 power domain)**

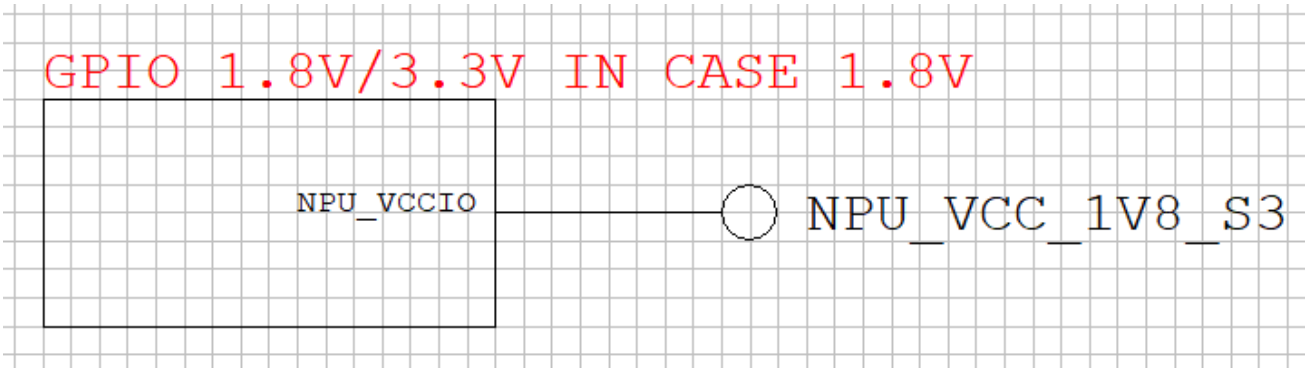



Figure 3–10 RK3399Pro NPU GPIO 1.8V/3.3V Power Setting – 1.8V Mode

- **1.8V/3.3V at 3.3V mode (PMUIO2, VCCIO5 and VCCIO6 power domain)**

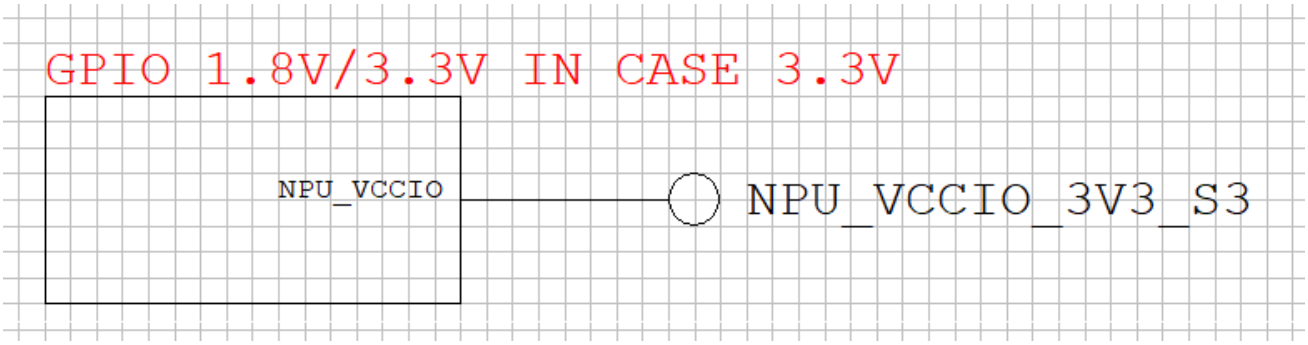



Figure 3–11 RK3399Pro NPU GPIO 1.8V/3.3V Power Setting – 3.3V Mode

## 3.2 NPU Power Design

### 3.2.1 NPU Minimum System Power Introduction

- **3.2.1.1 Power Requirement**
  - PLL:NPU_PLL_AVDD_0V8、NPU_PPLL_AVDD_0V8、NPU_OSC_VDD_1V8、NPU_PLL_AVDD_1V8、NPU_PPLL_AVDD_1V8、
  - CPU:NPU_CORE_VDD、NPU_CPU_VDD
  - LOGIC:NPU_LOGIC_VDD
  - DDR:NPU_DDR_VDD
  - GPIO:NPU_PMU_VDD_0V8、NPU_PMUIO1_VDD_1V8
- **3.2.1.2 Power-up Sequence**

Theoretically follow the rule to power up the low voltage earlier than the high voltage in the same IP and the same voltage in one IP could be powered up at the same time. There is no sequence requirement among different IPs.

Refer to the recommended power-up sequence as below:

NPU_VDD_LOG_S0&NPU_VDD_0V8--->NPU_VCC_1V8&NPU_VCC_DDR--->NPU_VDD_CPU--->NPU_VDD

### 3.2.2 NPU Power Design Recommendation

- **3.2.2.1 Standby Circuit Solution**

RK3399Pro board level system uses the standby solution and the system consists of constant power supply area and power-off in standby area which supply power independently as shown below:

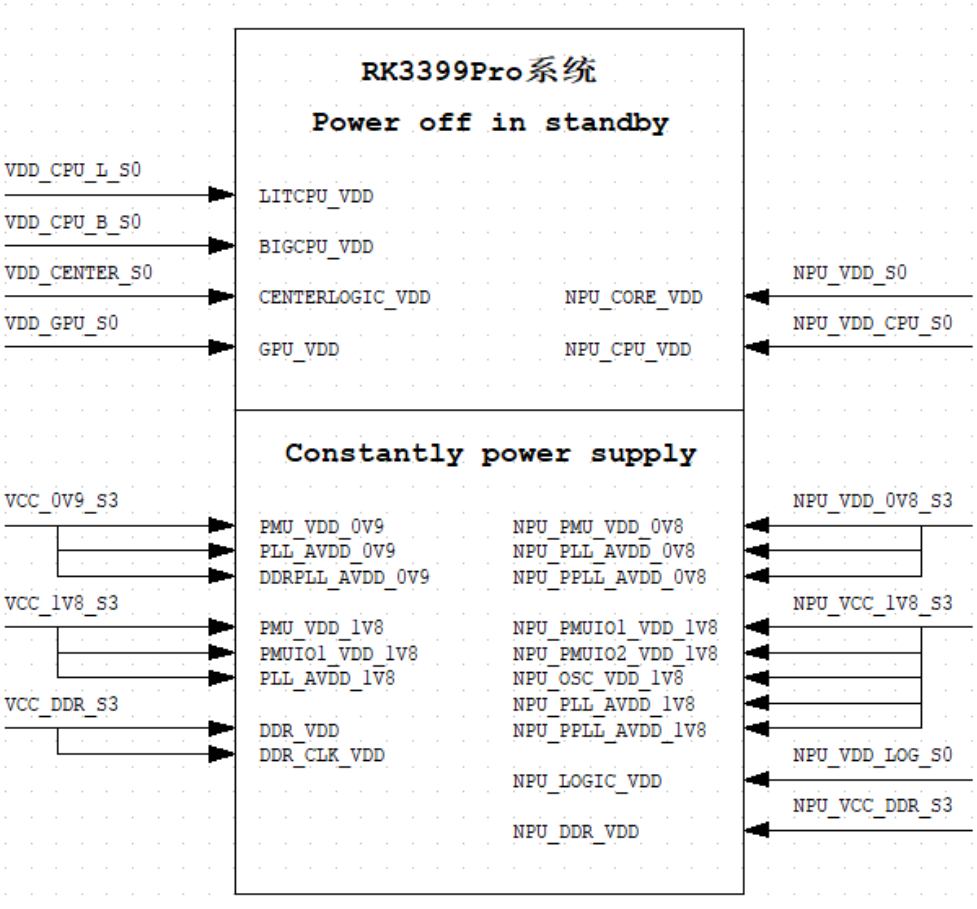



Figure 3–12 RK3399Pro NPU Standby Circuit Solution

The power-off in standby area is controlled by respective GPIO to turn on and turn off the power supply.

The constant power supply area is controlled by respective GPIO to turn on the power supply, and at least the following 4 groups of power supply must be always on in standby.

- DDR:NPU_VCC_DDR, supply power for DDR self-refresh.
- GPIO、PLL:NPU_VDD_0V8&NPU_VCC_1V8, supply IO power for PMUIO power domain to maintain output status and interrupt response, supply power for PLL and CPU OSC working
- LOGIC:NPU_VDD_LOG, supply power for chip logic and bus working

### 3.2.2.2 PLL Power

Recommend to use a LDO as a separate power supply for PLL within RK3399Pro, especially when DDR operating frequency is relatively high, the stable PLL power is helpful for improving the stability. The decoupling capacitor should be placed close to the pin.

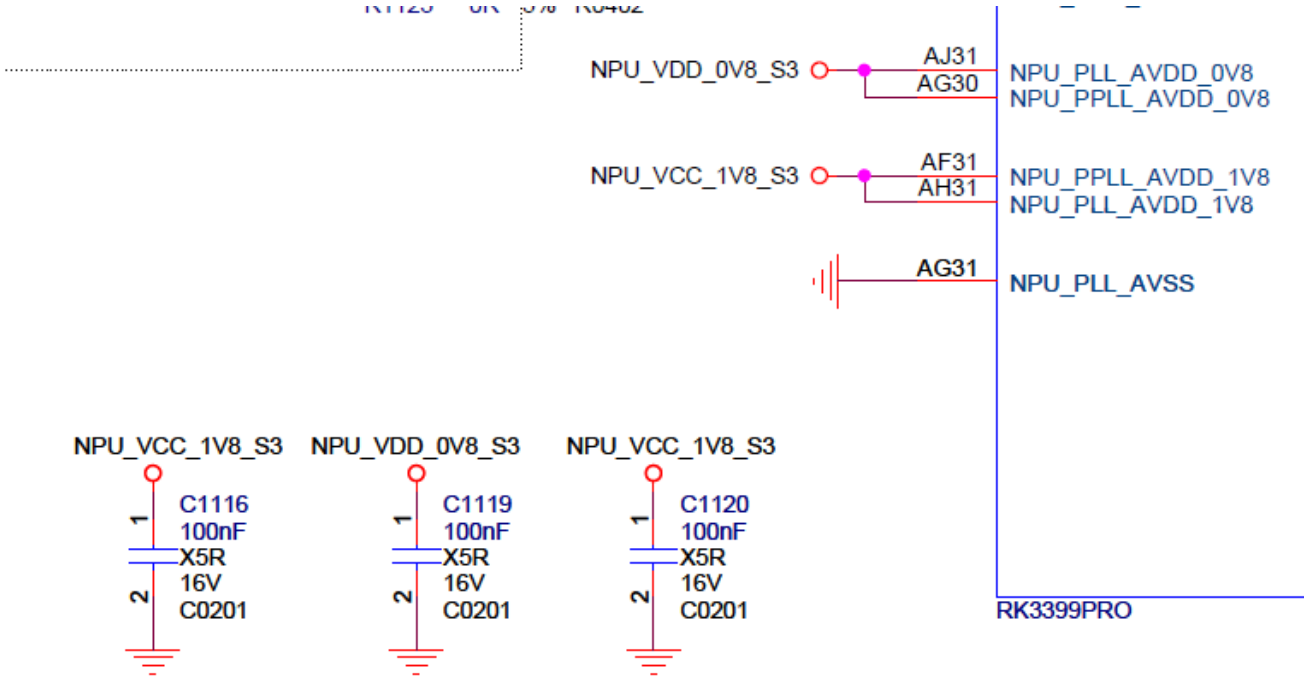



Figure 3–13 RK3399Pro NPU PLL Power

### 3.2.2.3 NPU Power

RK3399Pro NPU uses independent power domain to supply power, NPU_VDD_CPU is the core power supply of NPU, and the current is relatively small, fixed 0.85 is enough. NPU_CORE_VDD supply power for NPU, support DVFS dynamic voltage frequency scaling function, use separate DC-DC power supply, and the peak current can reach up to 2.1A, so please do not reduce or delete the capacitors in the reference design schematic. For layout, place the big capacitors on the back of RK3399Pro (or close to the SoC) to ensure that the power ripple is controlled within 80mV to avoid the power ripple abnormality with high load. The capacitor is shown as below:

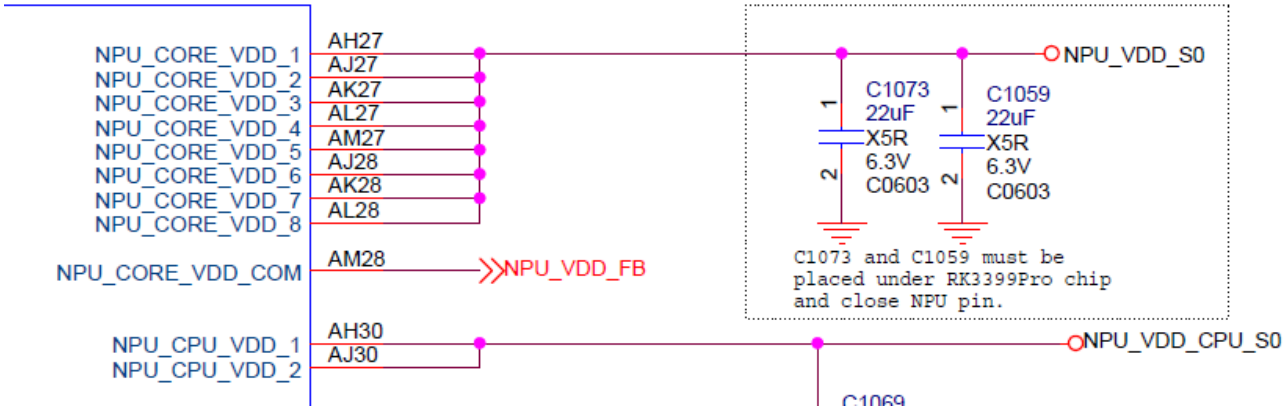



Figure 3–14 RK3399Pro NPU VDD_CPU Power

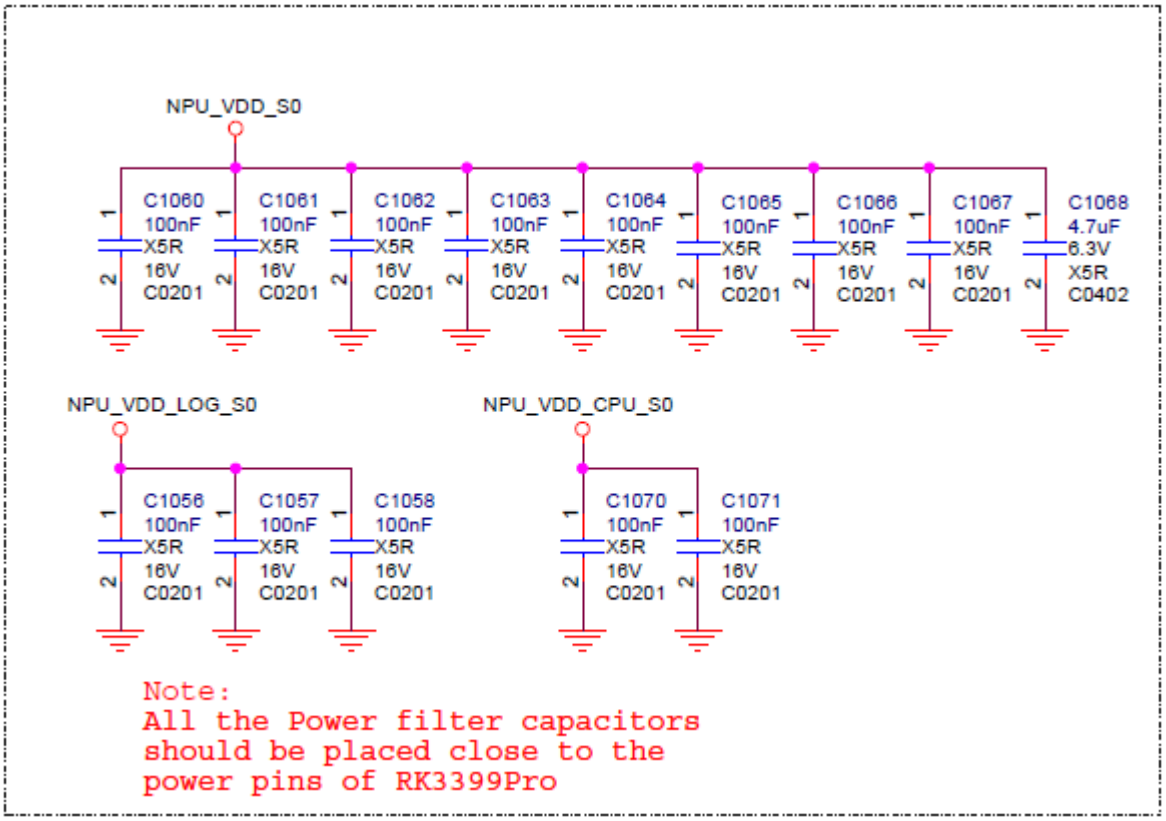



Figure 3–15 RK3399Pro NPU VDD_CPU Power Decoupling

NPU_CORE_VDD_COM is NPU_CORE_VDD power feedback pin of RK3399Pro and it should be connected to FB side of DC-DC power, which can compensate the loss of PCB power traces impedance and improve the real-time of dynamic adjustment power supply.

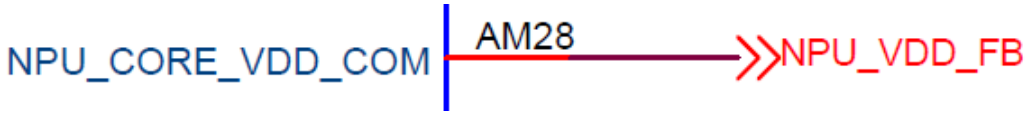



Figure 3–16 RK3399Pro NPU VDD_CPU_COM Power Feedback

- **3.2.2.4 LOGIC Power**

  RK3399Pro NPU digital logic part power is supplied separately by NPU_LOGIC_VDD.

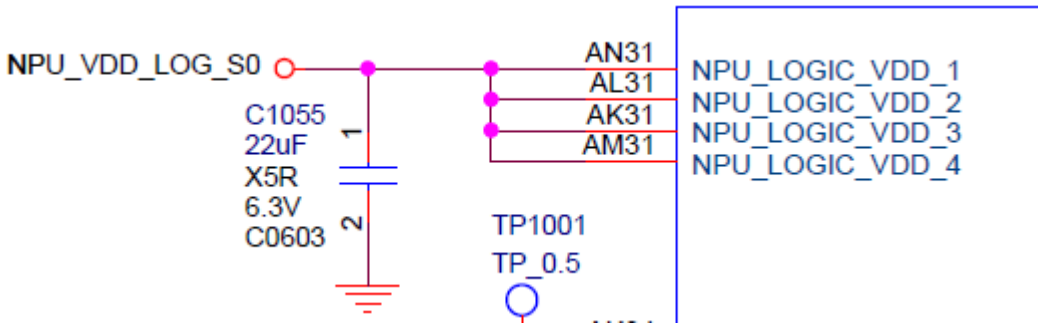



Figure 3–17 RK3399Pro NPU Logic Power

VDD_LOG_S3 uses fixed level 0.8V, so use DC-DC to supply power directly as shown below:

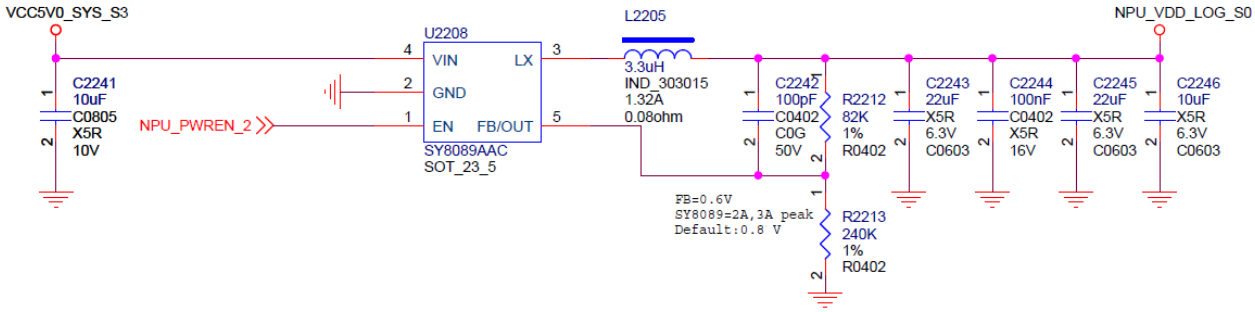



Figure 3–18 RK3399Pro NPU VDD_LOG Power

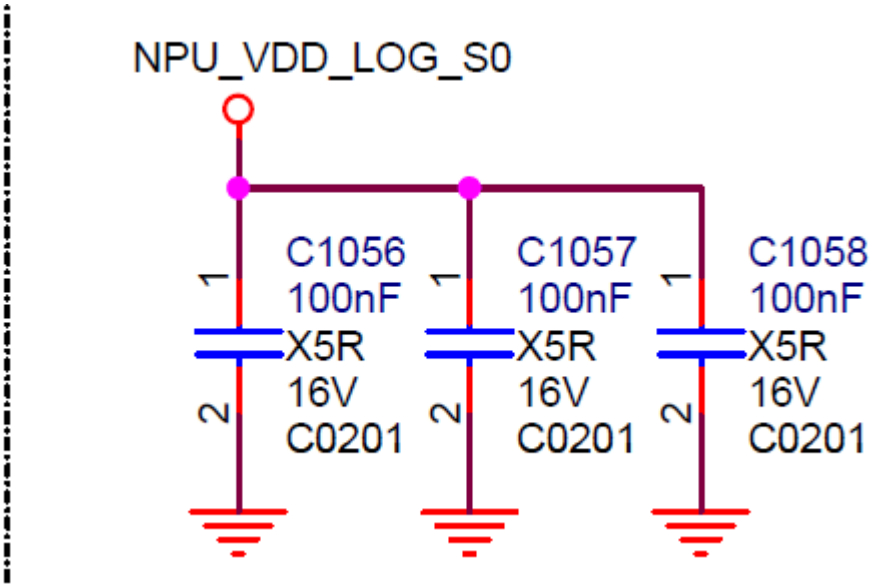



Figure 3–19 RK3399Pro NPU Logic Power Decoupling

- **3.2.2.5 DDR Power**

RK3399Pro NPU DDR controller interface supports DDR3/DDR3L/LPDDR3 level standards. Only need to supply power for NPU_DDR_VDD and the power level is different for different DDR components. There are several levels 1.5V/1.35V/1.2V to be adjusted. Please confirm to meet the product design requirement based on the component used.

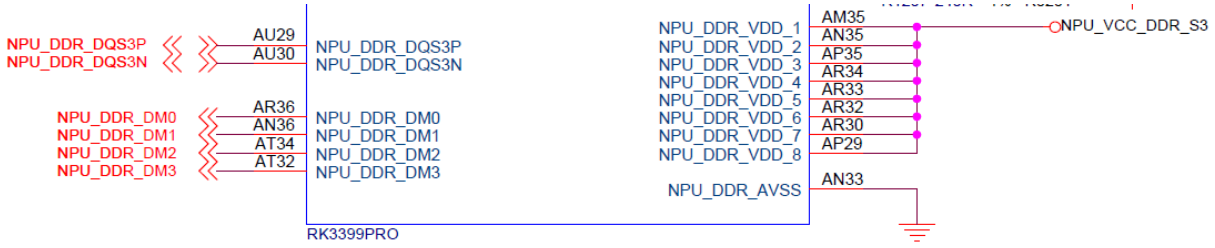



Figure 3–20 RK3399Pro NPU DDR Controller Power

RK3399Pro NPU DDR controller internally integrates Vref circuit to generate the required reference voltage Vref_mcu=VCC_DDR/2 and provide it to DRAM. The Vref of DRAM side can also be generated by resistance divider circuit, Vref_CA=VCC_DDR/2, while Vref_DQ can be adjusted according to ODT strategy, and the corresponding Vref voltage can be adjusted according to the drive strength and the ODT value.

Take LPDDR3 as an example: At 800MHz frequency, the drive strength of RK3399Pro NPU chip side is 34.3ohm, DRAM side ODT is configured as 240ohm, when ODT is enabled, calculate according to the formula DRAM Vref=0.56*VCC_DDR.

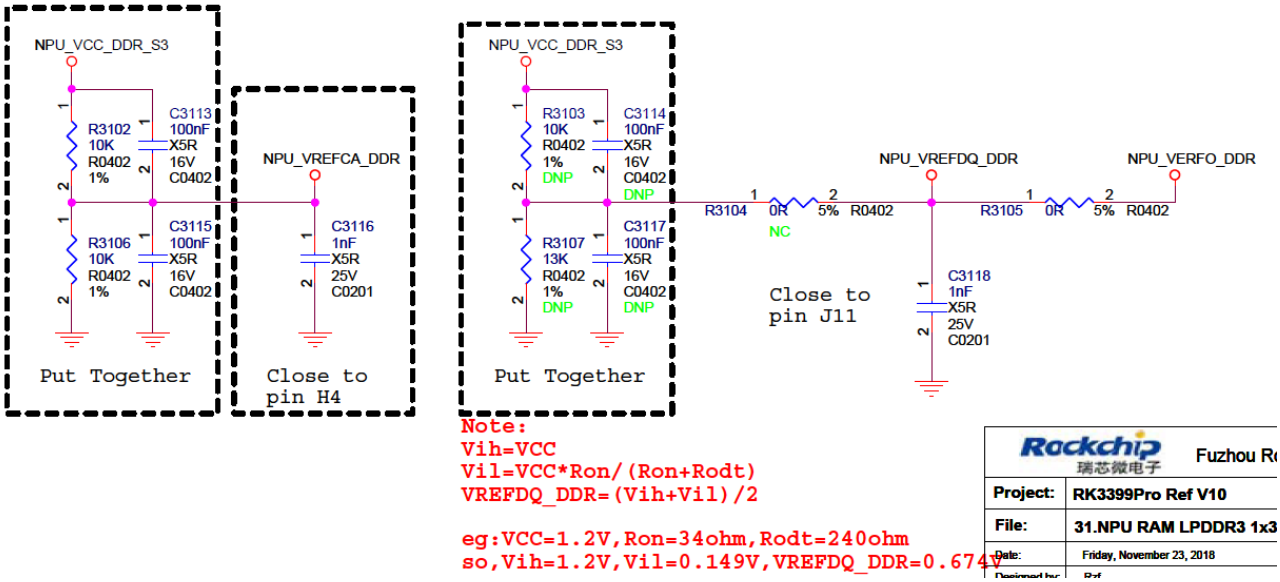



Figure 3–21 RK3399Pro NPU LPDDR3 DRAM VREF power supply

**Note**

*As for Vref_DQ design of various components:*

*DDR3/DDR3L internal pull up/down will occur at the same time when ODT function is enabled, Vref_DQ=Vref_CA=VCC_DDR/2; so only LPDDR3 needs to adjust Vref_DQ separately.*

The DRAM VREF_DQ and VREF_CA of LPDDR3 use a separate VREF voltage reference circuit. The power of VREF_DQ pin can be supplied by a 1K ohm resistors divider (1% accuracy), or by NPU_VREFO_DDR output from NPU DDR controller which voltage range can be adjusted by software. Because VREF_CA power is constantly supplied, use a 10Kohm resistors divider (1% accuracy) can reduce the standby power consumption and parallel connect 100nF capacitor can improve the power following characteristic of VCC_DDR_S3. Place a 1nF decoupling capacitor close to each reference power pin.

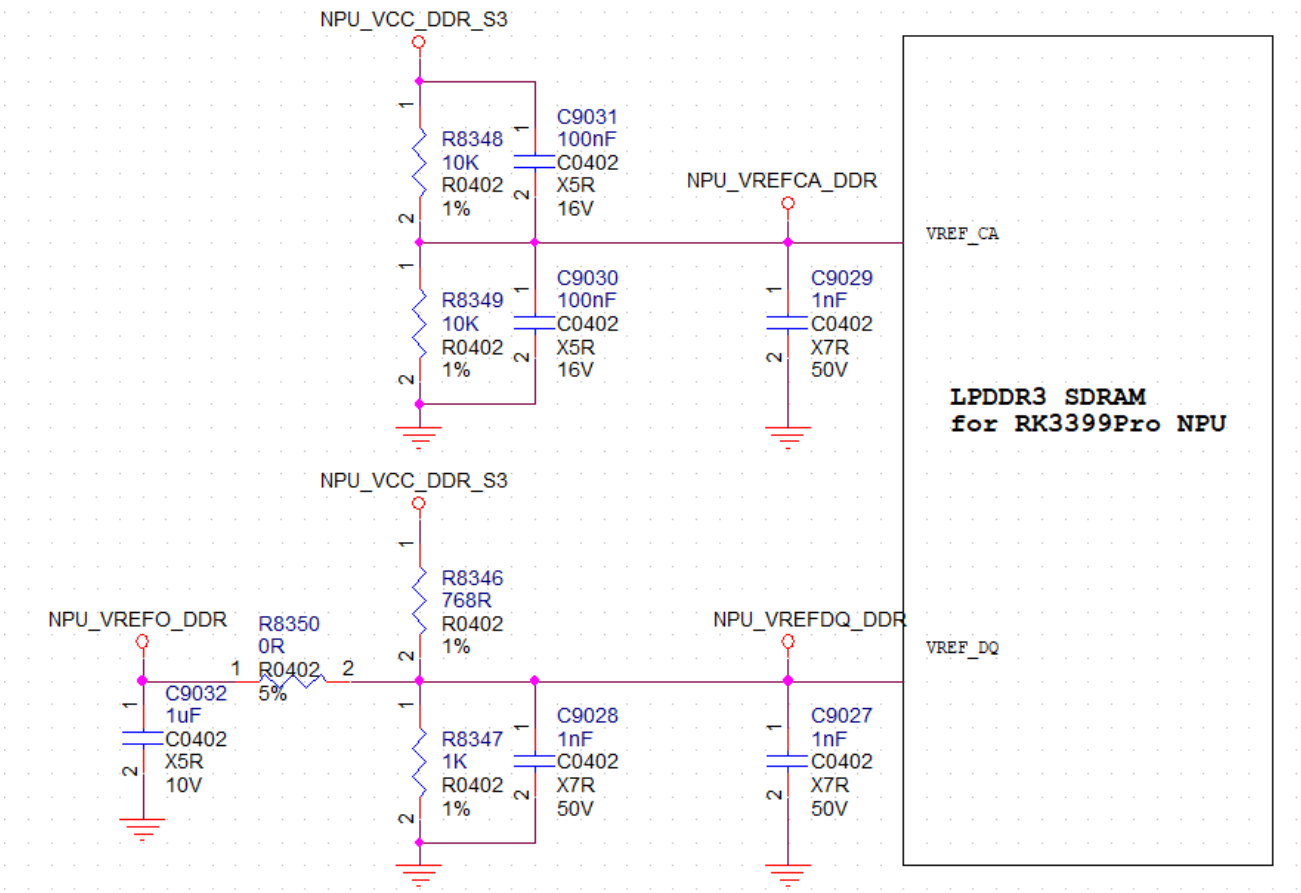



Figure 3–22 RK3399Pro NPU LPDDR3 DRAM VREF Power supply

- **3.2.2.6 GPIO Power**

GPIO power refers to section 3.1.8. Recommend to place a 100nF decoupling capacitor for each pin and place it close to the power pin. For detailed design, please refer to RK3399Pro reference design schematic.

### 3.2.3 NPU Over-temperature Protection Circuit

When RK3399Pro NPU occurs over-temperature or crash, the TSADC_SHUT/NPU_GPIO0_A6 pin of the chip will output high level to reset RK809-3 and control the power off and restart, reset the whole system while the register is cleared.

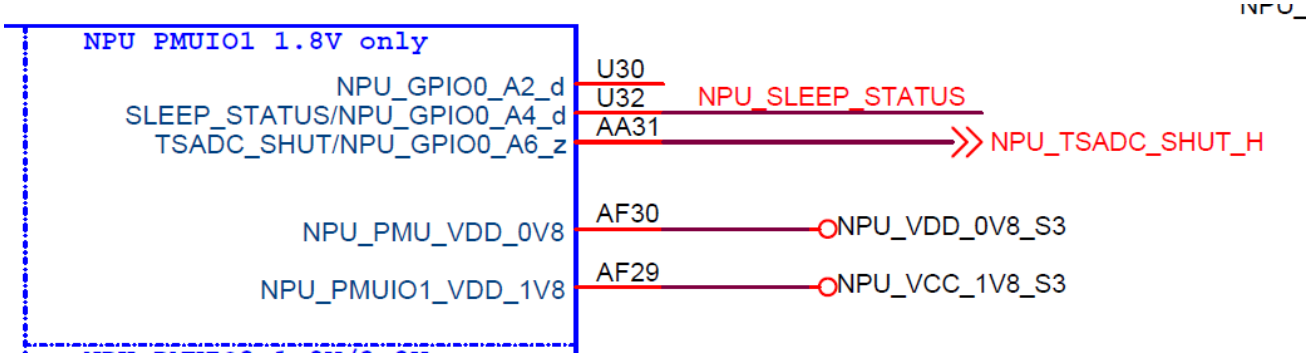



Figure 3–23 RK3399Pro NPU_TSADC_SHUT_H Over-temperature Protection Output

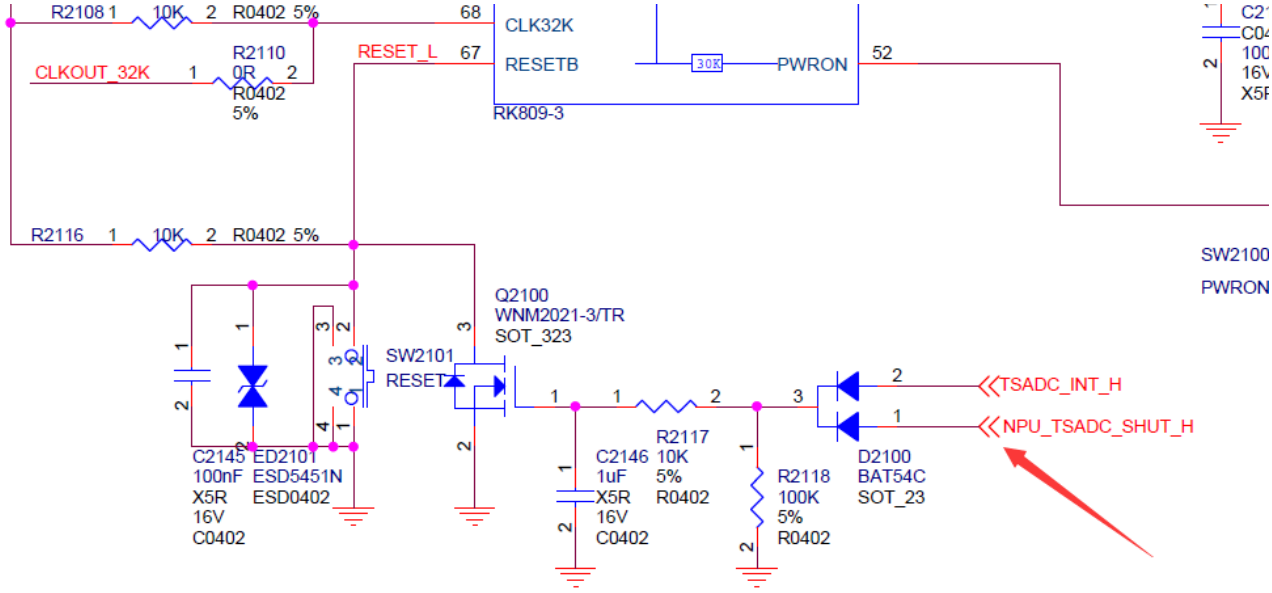



Figure 3–24 RK809-3 NPU_TSADCSHUT_H Over-temperature Protection Input

### 3.2.4 NPU Power Peak Current

Below table shows the peak current test result of the running mode for RK3399Pro EVB, only for reference. The test conditions are as below:

- APK version: antutu_benchmark_v7_3d+run.sh
- DDR component: 32bit LPDDR3 K4E6E304EB-EGCF
- Oscilloscope enables the 20MHz bandwidth limitation.

| Configuration | ITEM | SOC Model | CPU frequency | NPU frequency | Memory | GPU Render | GPU Frequency | DDR Type | DDR Frequency | Bat voltage (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| | RK3399Pro | Dual-core Cortex-A72 + Quad-core Cortex-A53 + NPU | A72 Max: 1800MHz 1.20V<br>A53 Max: 1416MHz 1.125V | Max: 800MHz 0.85V | CPU: 4G<br>NUP: 2G | Mail-T860MP4 | Max: 800MHz 1.075V | CPU: LPDDR3<br>NPU: LPDDR3 | CPU DDR Max: 800MHz<br>NPU DDR Max: 786M | |

Figure 3–25 RK3399Pro EVB Peak Current Test Condition

Table 3–7 RK3399Pro NPU Peak Current Table

| PowerName | Voltage（V） | Peak Current(mA) |
|---|---|---|
| NPU_VDD_CPU_S0 | 0.870 | 191.0 |
| NPU_VDD_S0 | 0.874 | 2047.0 |
| NPU_VDD_LOG_S0 | 0.865 | 279.9 |
| NPU_VCC_DDR_S3 | 1.294 | 520.4 |
| NPU_VDD_0V8_S3 | 0.860 | 63.9 |
| NPU_VCC_1V8_S3 | 1.789 | 106.6 |

# 3.3 NPU Function Interface Circuit Design Guide

## 3.3.1 NPU USB Circuit

RK3399Pro NPU includes a USB 2.0 controller and a USB 3.0 controller, and they can compose a complete USB 3.0 interface when used together.

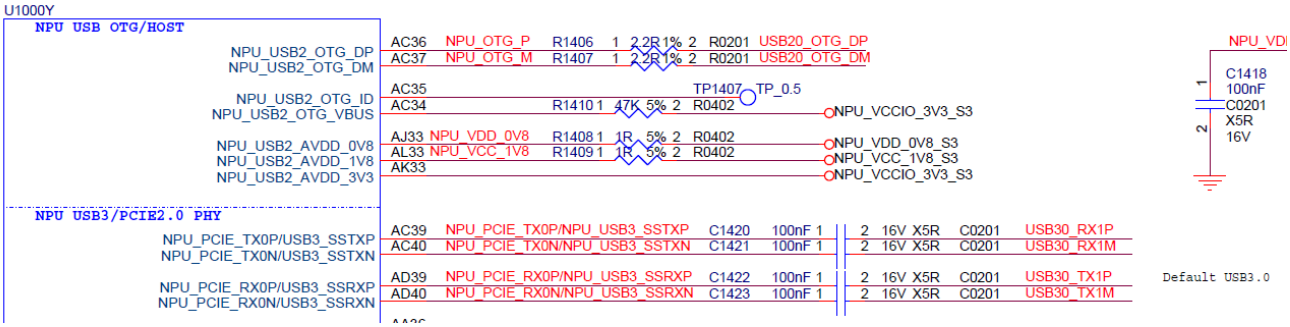



Figure 3–26 RK3399Pro NPU USB Module

Please note for design:

- USB interface as the communication port between CPU and NPU can only be connected to CPU, used to load images.
- USB3 multiplexed with PCIE, default used as USB function.
- USB_VBUS (USB_DET) is used to detect USB insertion, need to be pulled up externally.

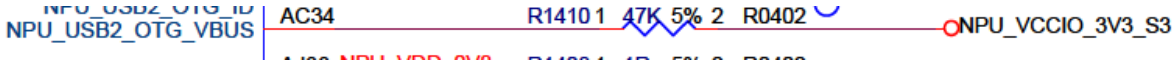



Figure 3–27 RK3399Pro NPU USB Insertion Detection

- USB controller configuration reference resistor should select the resistor with 1% accuracy, and it will affect the USB amplitude and influence the quality of eye diagram.

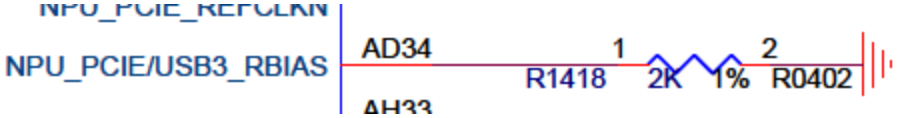



Figure 3–28 RK3399Pro NPU USB0 Controller Reference Resistance

- In order to avoid the damage caused by surge, the 0.8V/1.8V power of the controller needs to series connect 1ohm resistance.

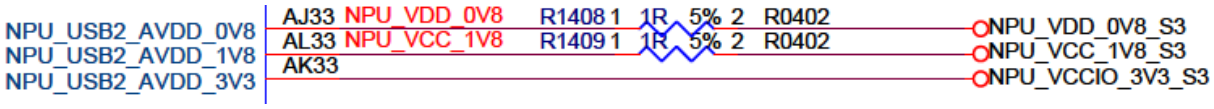



Figure 3–29 RK3399Pro NPU USB Controller Power Anti-surge

- In order to avoid the damage caused by surge, need to series connect 2.2ohm resistance on OTG_DP/DM signal.

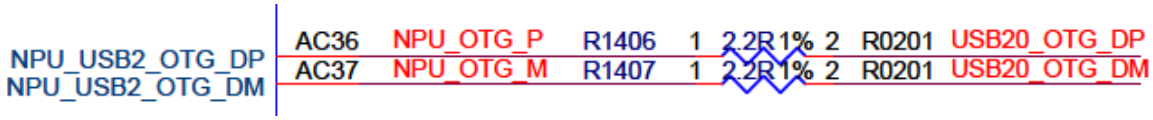



Figure 3–30 RK3399Pro NPU USB Reserved Common Mode Choke

- In order to improve USB performance, the decoupling capacitor of the controller power should be placed close to the pin.
- There should be coupling capacitor on TX/RX traces.

USB2.0 interface pull up/down and matching design are recommended in below table:

Table 3–8 RK3399Pro NPU USB2.0 Interface Design

| Name | Connection method | Description |
|---|---|---|
| NPU_USB2_OTG_DP/DM | Series connect 2.2ohm resistor | NPU USB2.0 OTG0 input/output, can compose Type-C0 interface with USB3.0 PHY0 |
| NPU_USB2_OTG_ID | Vacant | NPU USB2.0 OTG0 ID recognition, not used |
| NPU_USB2_OTG_VBUS | External pull up | NPU USB2.0 OTG0 connection detection |
| USB3_SSTXP/N | 100nF capacitor coupling connection | NPU USB3.0 SuperSpeed output data |
| USB3_SSRXP/N | 100nF capacitor coupling connection | NPU USB3.0 SuperSpeed input data |
| USB3_RBIAS | | USB2.0 PHY1 configuration reference resistor, 133ohm connected to GND, valid for HOST1 and OTG1 |

### 3.3.2 NPU PCIe Circuit

RK3399Pro NPU PCIe supports PCIe V2.1 protocol, and can be used to replace USB3.0 to communicate with CPU. It has below features:

- Support Root Complex（RC） and End Point（EP）
- Support 2x/1x mode, respectively have 2 pairs of TX and RX differential lines.
- Signal data channel supports signal transmission rate up to 2.5GT/s and 5.0GT/s, with 8b/10b form, so the maximum signal rate is 500MB/s.

The analog power NPU_PCIE_VCCA_0V9 and NPU_PCIE_VCCD_1V8&NPU_PCIE_VCCA_1V8 are RK3399Pro NPU PCIe controller's power supply. Recommend to power up PCIE_VCCA_0V9 first.

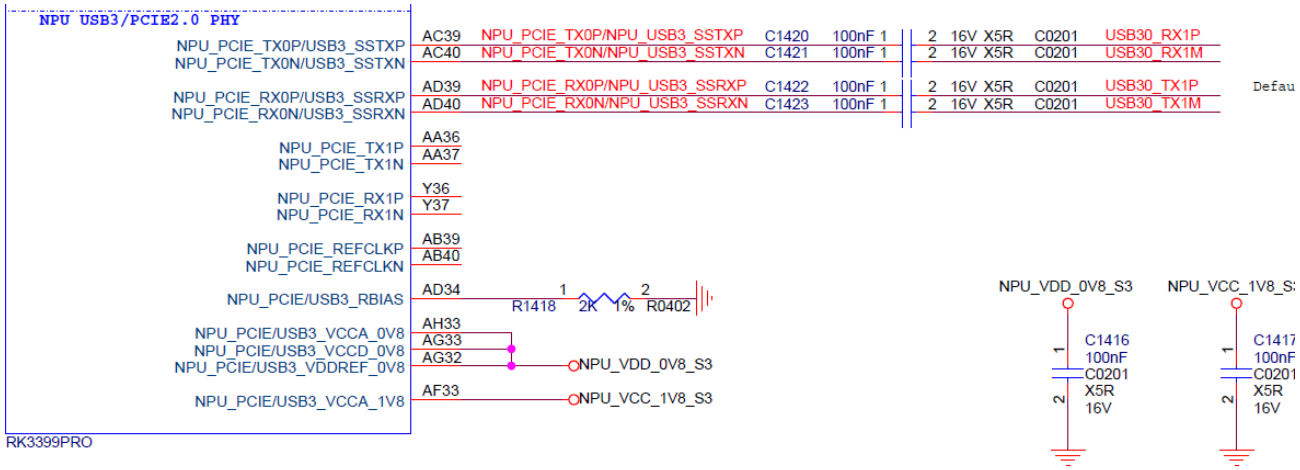



Figure 3–31 RK3399Pro NPU PCIe Module

### 3.3.3 NPU UART Circuit

RK3399Pro NPU supports to use UART for software debugging.

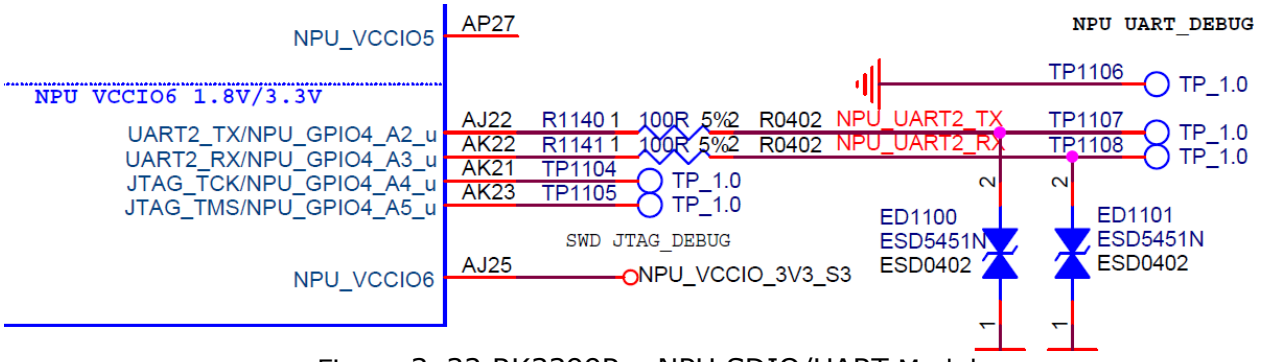



Figure 3–32 RK3399Pro NPU SDIO/UART Module

UART interface pull up/down and matching design are recommended as below table:

Table 3–9 RK3399Pro NPU UART Interface Design

| Name | Internal pull up/down | Connection method | Description (chip side) |
|---|---|---|---|
| UART2_RX | Pull up | Direct connection | UART2 data input |
| UART2_TX | Pull up | Direct connection | UART2 data output |

You can externally connect UART-to-USB conversion board for debugging when needed. Please select the port number of the board which is connected to PC, the baud rate selects 1.5M, and Flow control RTS/CTS doesn't need to select. If PC embedded DB-9 port doesn't support high speed mode, please use the USB-to-serial port conversion method.

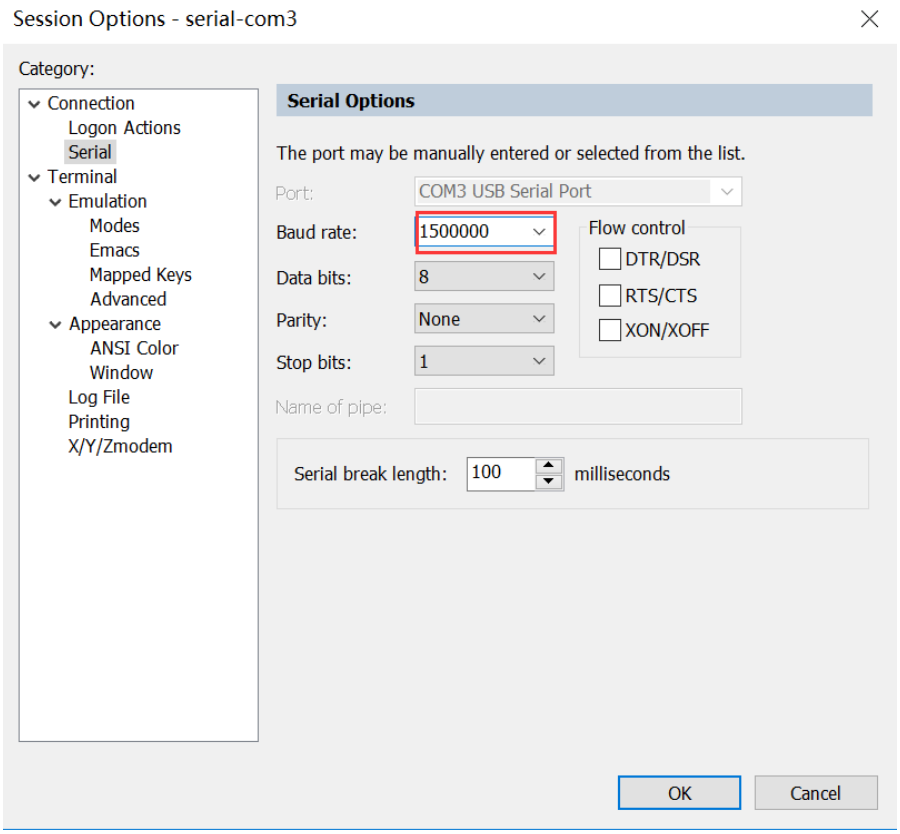



Figure 3–33 RK3399Pro NPU Serial Port Configuration

# 4 Thermal Design Recommendation

## 4.1 Thermal Simulation

For RK3399Pro TFBGA395L package, we can get the thermal simulation report using the Finite Element Modeling (FEM) method based on EVB 8-layer PCB. This report is based on the JEDEC JESD51-2 standard; the system design and environment for the application may be different from the JEDEC JESD51-2 standard and need to do analysis according to the application conditions.

Note

*Thermal resistance is the reference value of the PCB without the heat sink. The specific temperature is related to the board design, size, thickness, material and other physical factors.*

### 4.1.1 Result Summaries

The thermal simulation result is shown as below table:

Table 4–1 RK3399Pro Thermal Simulation Report

| Package (EHS-FCBGA) | Power(W) | $\theta_{JA}(℃/W)$ | $\theta_{JB}(℃/W)$ | $\theta_{JC}(℃/W)$ |
|---|---|---|---|---|
| EVB PCB | 8 | 20.71 | 10.66 | 1.94 |

### 4.1.2 PCB Description

PCB structure used for thermal simulation is shown as below table:

Table 4–2 RK3399Pro PCB Sturcture for Thermal Simulation

| | | |
|---|---|---|
| EVB PCB | PCB Dimension（L x W） | 201.8 x 137.8mm |
| | PCB Thickness | 1.6mm |
| | Number of Cu Layer | 8-layers |
| | Dielectric | FR4 |

### 4.1.3 Terminology

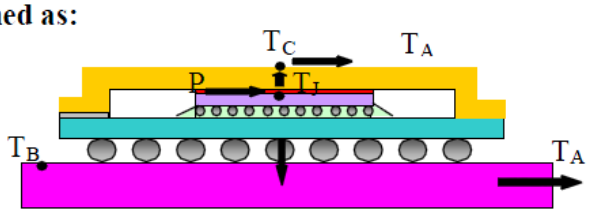
The terminologies in this chapter are explained as below:

- TJ: The maximum junction temperature;
- TA: The ambient or environment temperature;
- TC: The maximum compound surface temperature;
- TB: The maximum surface temperature of PCB bottom;
- P: Total input power

The thermal parameter can be define as following

**1.** *Junction to ambient thermal resistance,* $\theta_{JA}$**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad ; \qquad (1)$$

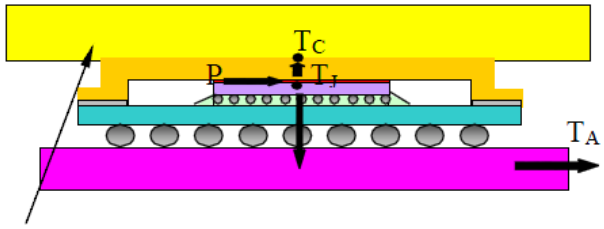



**Thermal Dissipation of EHS-FCBGA**

Figure 4–1 θJA Definition

**2.** *Junction to case thermal resistance,* $\theta_{JC}$**, defined as:**

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad ; \qquad (2)$$

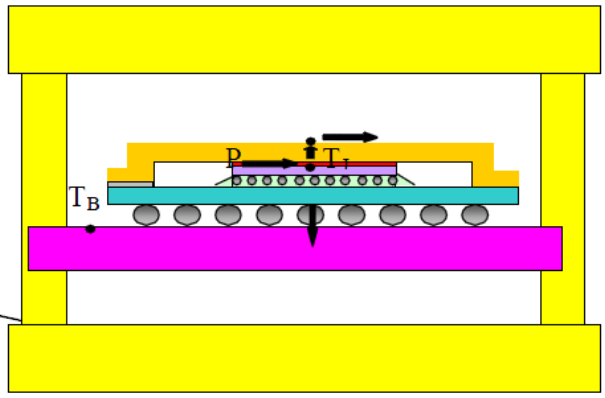



**Attach a block with constant temperature onto package.**

Figure 4–2 θJC Definition

**3.** *Junction to board thermal resistance,* $\theta_{JB}$**, defined as:**

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad ; \qquad (3)$$




**Attach a block with constant temperature**

Figure 4–3 θJB Definition

## 4.2 SoC Internal Thermal Control Method

### 4.2.1 Thermal Control Strategy

In the Linux kernel, define a set of temperature control framework linux Generic Thermal System Drivers. It can control the temperature of the system through different strategies, and there are three currently commonly used strategies as below:

- Power-allocator: Introduce PID (proportional - integral - differential) control, according to current temperature, dynamically allocate power for the modules, and

convert power into frequency, so as to achieve the effect of limiting the frequency according to the temperature.

- Step-wise: According to current temperature, limit the frequency step by step
- Userspace:Do not limit the frequency.

RK3399Pro has embedded T-sensor to detect the chip temperature, the default policy is to use Power-allocator strategy, and the working state can be divided into the following cases:

- When the temperature exceeds the set value:
  - The temperature trend rises, start to decrease the frequency.
  - The temperature trend drops, start to increase the frequency.
- When the temperature drops to the set value:
  - The temperature trend rises, the frequency does not change.
  - The temperature trend drops, start to increase the frequency.
- When the frequency rises to the highest, but the temperature is still under the set value, CPU frequency is no longer limited by thermal control, and changed to be controlled by system load.
- When the frequency is down, the chip is still over-temperature (such as poor heat dissipation) more than 95 degrees then the software will trigger a restart; If failure to restart due to deadlock or other reasons makes the chip temperature more than 100 ℃, it will trigger the chip internal OTP_OUT signal to PMIC for direct shutdown. Refer to Section 2.2.5.1 for specific actions.

Note

*The temperature trend is obtained by comparing the two temperatures collected continuously. When the device temperature does not exceed the threshold, collect the temperature once every second. When the device temperature exceeds the threshold, collect the temperature once every 20ms and limit the frequency.*

### 4.2.2 Thermal Control Configuration

RK3399Pro SDK can respectively provide temperature control strategy for CPU and GPU. For the specific configuration, please refer to "Rockchip Thermal Development Guide" released by Rockchip.

# 5 ESD/EMI Protection Design

## 5.1 Overview

The chapter gives recommendations for ESD / EMI protection design in the RK3399Pro product design to help customers improve the anti-static and anti-electromagnetic interference levels of their products.

## 5.2 Terminology

The terminologies in this chapter are explained as below:

- ESD: Electro-Static Discharge
- EMI: Electro Magnetic Interference

## 5.3 ESD Protection

- To ensure a reasonable mold design; need to reserve ESD components for port and connector parts.
- PCB layout should do a good job in the protection and isolation for sensitive parts.
- PCB layout should try to place RK3399Pro and the core components in the middle of the PCB, if it can not be placed in the middle of the PCB ,need to ensure that the shield is away from the PCB edge at least more than 2MM and can be reliably connected to GND.
- PCB layout should be designed according to the function module and the signal flow, the sensitive parts should be independent from each other, and the parts which are easy to be interfered should be isolated.
- Require to reasonably place ESD components, generally place them at the source, that is, ESD components should be placed in the position of interfaces or the electrostatic discharge area.
- The parts need to be placed away from the edge of the PCB and keep a certain distance from the connectors.
- The PCB surface must have a good GND loop, and the connectors must have a good GND connection loop on the surface layer. The shield should be connected with the surface GND, and need to add as many vias as possible to GND in the position of the shield cover welding. In order to do this, there should be no traces of connectors routing in the surface layer, and do not appear a wide range trace cutting off the copper.
- The PCB surface edge should have no traces and have as many vias as possible to GND.
- When it is necessary, do a good isolation between the signal and GND.
- Expose as much copper as possible, in order to enhance the electrostatic discharging effect, or add conductive cotton and other remedial measures.

## 5.4 EMI Protection

- There are three elements of electromagnetic interference: interference source, coupling channel and sensitive equipment. We can not deal with the sensitive equipment; so we can only deal with EMI through the interference source and the coupling channel. To solve the EMI problem, the best way is to eliminate the interference source, if it can not be eliminated, find the way to cut off the coupling channel or avoid the antenna effect.
- The PCB interference source is generally difficult to be completely eliminated, and can be dealt with through filter, ground, balance, impedance control or improve the signal quality (such as termination) and other methods. Generally various methods will be used synthetically, but good grounding is the most basic requirement.
- The commonly used material to deal with EMI includes the shielding cover, special filters, resistors, capacitors, inductors, beads, common mode inductance / magnetic

ring, absorbing materials, spread spectrum parts and so on.

- The filter selection principle: If the load (receiver) is high impedance (generally the single-ended signal interface is high impedance, such as SDIO, RBG, CIF, etc.), then select the capacitive filter parallel connected into the trace; if the load (receiver) is low impedance (such as power output interface), then select the inductive filter component series connected into the trace. The use of the filter should not make the signal quality beyond its SI permissible range. Differential interfaces usually use common mode choke to suppress EMI.
- The PCB shielding measures should be well-grounded otherwise it may cause radiation leakage or shielding measures to form the antenna effect. The connector shield should meet the relevant technical standards.
- RK3399Pro can use spread spectrum function by modules. The degree of the spread spectrum depends on the signal requirements of the relevant part. Refer to RK3399Pro spread spectrum description for the specific measures.
- The LAYOUT requirements of EMI are highly consistent with ESD. The above-mentioned layout requirements of ESD are mostly applicable for EMI protection. Besides, add the following requirements:
  - Ensure the signal integrity as much as possible.
  - The differential signal should do the isometric and tight coupling to ensure the differential signal symmetry; try to minimize the differential signal and the clock dislocation, to avoid conversion to the common mode signal which will cause EMI issues.
  - Plug-in electrolytic capacitors and other components with metal shell should avoid coupling the interference signal to produce radiation. Also need to avoid the interference signal of the components coupling from the shell to other signals.

# 6 Welding Process

## 6.1 Overview

RK3399Pro is the ROHS directive certification products, that is, Lead-free products. This chapter regulates the RK3399Pro SMT basic settings of the temperature for customers. It mainly introduces the process control when customers use RK3399Pro to do the re-flow solder: mainly lead-free process and mixed process.

## 6.2 Terminology

The terminologies in this chapter are explained as below:

- Lead-free: Lead-free process.
- Pb-free: Lead-free process; all components (mainboard, all IC, resistance, capacitors, etc.) are lead-free components, and use pure lead-free process with the lead-free solder paste.
- Reflow profile: Reflow soldering temperature curve.
- ROHS: Restriction of Hazardous Substances.
- SMT: Surface Mount Technology.
- Sn-Pb: Tin-lead mixed process; means to use lead solder paste and have both lead-free BGA and lead IC hybrid welding process.

## 6.3 Re-flow Solder Requirement

### 6.3.1 Solder Paste Ingredient Requirement

The proportion of solder alloy and flux is 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerated temperature is 2 ~ 10 ℃, and should be put in room temperature to recover the temperature before using. It will take 3 ~ 4 hours to recover and need to make a record.

The solder paste needs to be stirred before brushing the board. Manually stir for 3-5 minutes or mechanically stir for 3 minutes. After stirring, it will present a natural vertical flow shape.

### 6.3.2 SMT Re-flow Profile

As RK3399Pro chip uses environmental protection material, recommend to use Pb-Free process. The reflow profile below is only the recommended value required by the JEDEC J-STD-020D process. Customers need to adjust according to the actual production situation.

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | <br>100 °C<br>150 °C<br>60-120 seconds | <br>150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_p$) | 3 °C/second max. | 3 °C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body temperature ($T_p$)* | See classification temp in Table 4.1 | See classification temp in Table 4.2 |
| Time ($t_p$)** within 5 °C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25 °C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Figure 6–1 Reflow Profile Classification

| Package Thickness | Volume mm³ <350 | Volume mm³ 350 - 2000 | Volume mm³ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm - 2.5 mm | 260 °C | 250 °C | 245 °C |
| >2.5 mm | 250 °C | 245 °C | 245 °C |

Figure 6–2 Lead-free Process Component Package Heat-resistant Standard

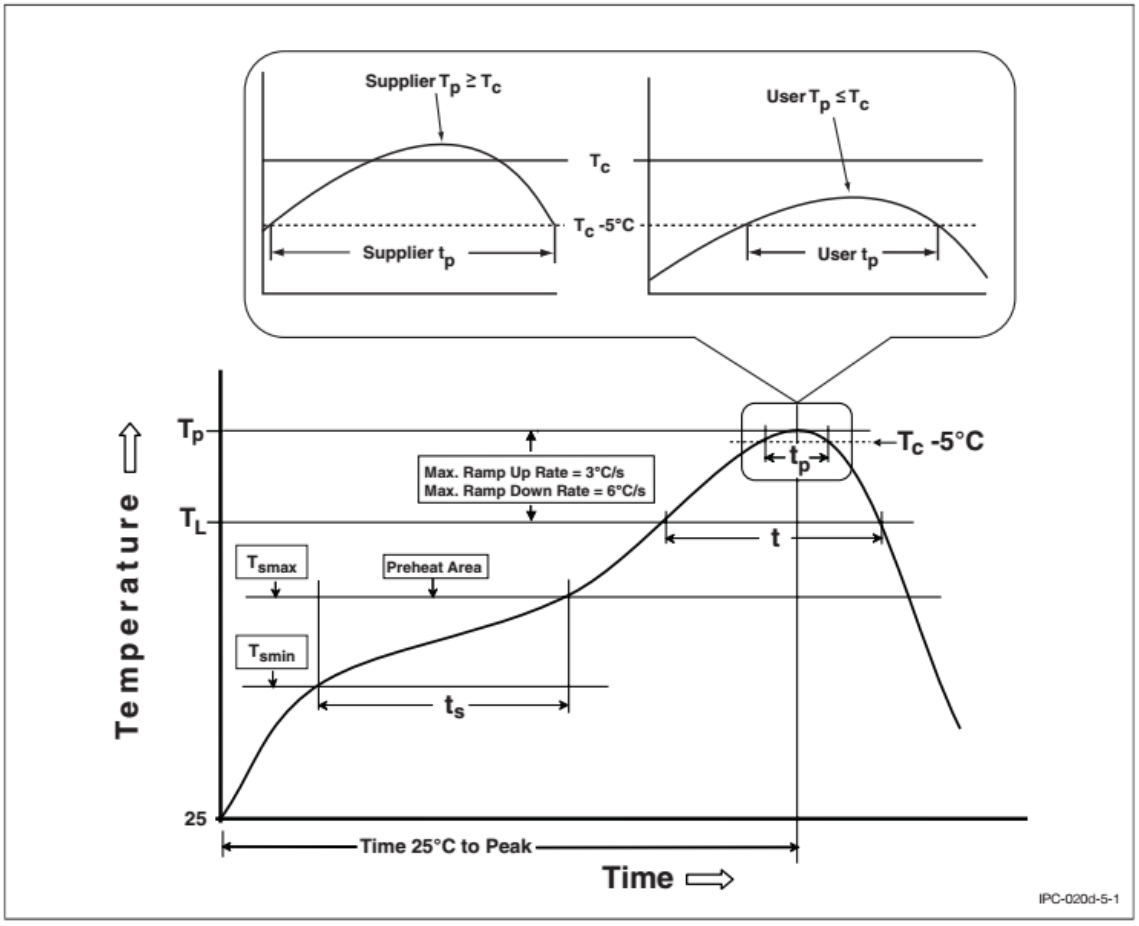



Figure 6–3 Pb-free Reflow Profile

### 6.3.3 SMT Recommended Reflow Profile

Rockchip recommended SMT reflow profile is shown as below:

| Step 1 Board Preheat | Step 2 Soak Time | Step 3 Peak Reflow & Time Above 220 °C | Step 4 Cool Down |
|---|---|---|---|
| Start with solder joint temp ≤ 40°C | After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer) | Solder Joint Temp 230 – 250°C Above ≥217°C 60 – 90 sec Max delta-t of solder joint temperature at peak reflow ≤10°C | Substrate MAX Temperature ≤260°C Die Peak Temperature ≤300°C |
| Rising Ramp Rate 0.5 – 2.5° C/ Sec. | Solder Joint Temp: 200 to 220°C | | Cooling Ramp Rate -0.5 to – 2.0°C/sec |
| Board Preheat Solder Joint Temp: 125 – 150°C | Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec. | Peak Temp Range, and Time Above ≥217°C spec's met. | PCB land/pad temperature needs to be at 100 – 130°C ±5°C when removing board from rework machine bottom heater at end of component removal operation or ≤80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation. |
| Preheat with bottom heater, before nozzle is lowered | Nozzle has lowered to reflow component | Nozzle is down during peak reflow | Nozzle raises to home position when solder joint reaches peak temp range |

Figure 6–4 Pb-free Reflow Profile Recommended Parameter

# 7 Packaging and Storage Condition

## 7.1 Overview

The chapter regulates RK3399Pro storage and usage specification to ensure the safety and correct usage of the product.

## 7.2 Terminology

The terminologies in this chapter are explained as below:

- Desiccant: A material used to adsorb moisture.
- Floor life: The longest time allowing the product exposed in the environment, from unpacking the moisture barrier bag to SMT.
- HIC: Humidity Indicator Card.
- MSL: Moisture Sensitivity Level.
- MBB: Moisture Barrier Bag
- Rebake: Bake again.
- Solder Reflow
- Shell Life: The storage expiration.
- Storage environment

## 7.3 Dry Vacuum Packaging

The dry vacuum packaging material of the product is as below:

- Desiccant
- HIC
- MBB, aluminum foil, silver opaque logo with moisture sensitivity level.
-


Figure 7–1 RK3399Pro Dry Vacuum Packaging

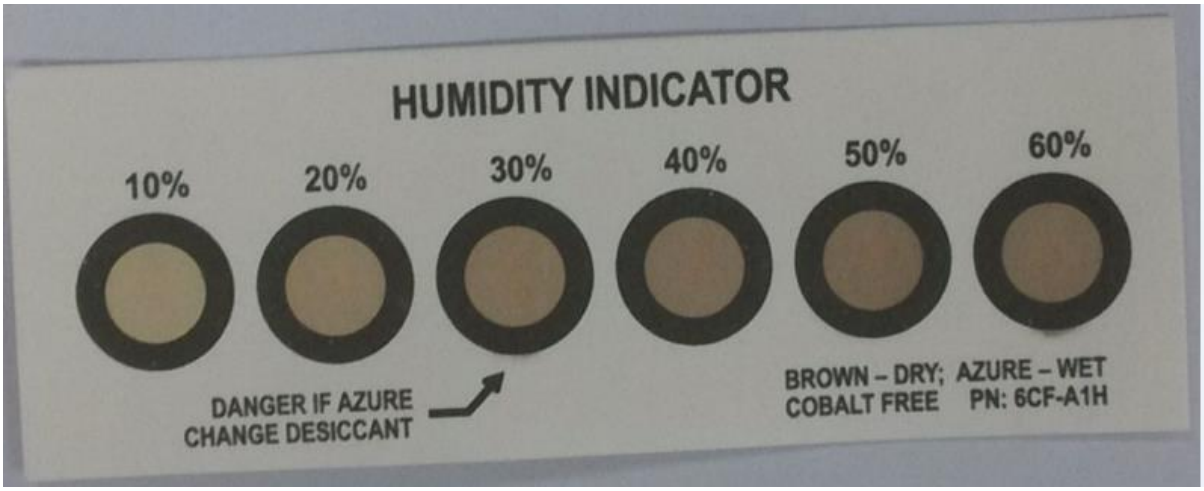



Figure 7–2 Humidity Indicator Card

## 7.4 Product Storage

### 7.4.1 Storage Environment

Product is vacuum packaged, and can be stored up to 12 months with environment temperature ≤ 40 ℃ and relative humidity ＜90%.

### 7.4.2 Exposure Time

Under ambient conditions <30 ° C and relative humidity 60%, please refer to below table:

RK3399Pro MSL level is 3, very sensitive to humidity. If the chip is not used for a long time after unpacking, and directly used in SMT without bake, chip failure will be likely to appear.

Table 7–1 Exposure Time Reference Table (MSL)

| MSL Level | Exposure Time<br>Factory environmental conditions:≦30 ℃ /60 ％RH |
|---|---|
| 1 | Unlimited at ≤300 ℃/85 ％RH |
| 2 | 1 year |
| 2a | 4 weeks |
| 3 | 168 hours |
| 4 | 72 hours |
| 5 | 48 hours |
| 5a | 24 hours |
| 6 | Mandatory bake before use, and must be reflowed within the time limit specified on the label. |

## 7.5 Moisture Sensitive Product Usage

The RK3399Pro must be baked after unpacking in the following cases:

- Continuous or accumulative exposure time is less than 168 hours, and the factory environment ≦ 30 ℃ / 60% RH.
- Stored in the <10% RH environment.

In below cases, RK3399Pro must be baked to eliminate the internal moisture to avoid the delamination and popcorn issues during reflow solder:

- The points > 10% of humidity indicator card already discolor at 23 ± 5 ℃. (Please refer to the humidity indicator card for color change).
- Not meet 2a or 2b standard.

Please refer to the following table for RK3399Pro re-baking time:

Table 7–2 RK3399Pro Re-bake Reference Table

| Package Body | MSL | High Temp Bake @125℃ +10/-0℃ | | Medium Temp Bake @90℃+8/-0℃ | | Low Temp Bake @40℃ +5/-0℃ | |
|---|---|---|---|---|---|---|---|
| | | Exceeding Floor Life by > 72h | Exceeding Floor Life by ≤ 72h | Exceeding Floor Life by > 72h | Exceeding Floor Life by ≤ 72h | Exceeding Floor Life by > 72h | Exceeding Floor Life by ≤ 72h |
| Thickness ≤1.4mm | 3 | 9 hours | 7 hours | 33 hours | 23 hours | 13 days | 9 days |

**Note**

*The table shows the minimum baking time required after damp.*
*Re-base prefers to use low-temperature baking.*