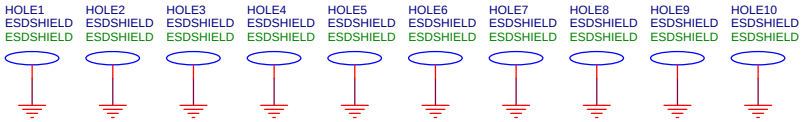
# RK3328 BOX Ref

## Content Indexing






## Bill of Materials

### Header:

**Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption**

### Combined property string:

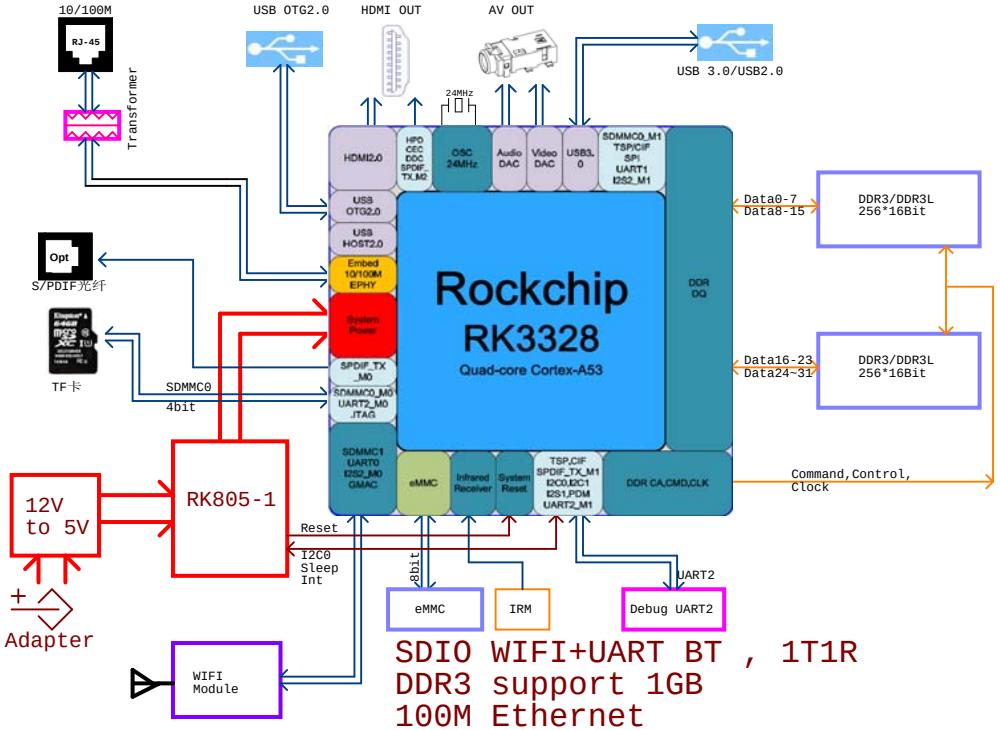
**{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}**

**Note：**
**Component parameter description**
**1. DNP stands for component not mounted temporarily**
**2. If Value or option is DNP, which means the area is reserved without being mounted**

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | Index | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 1 of 29 |

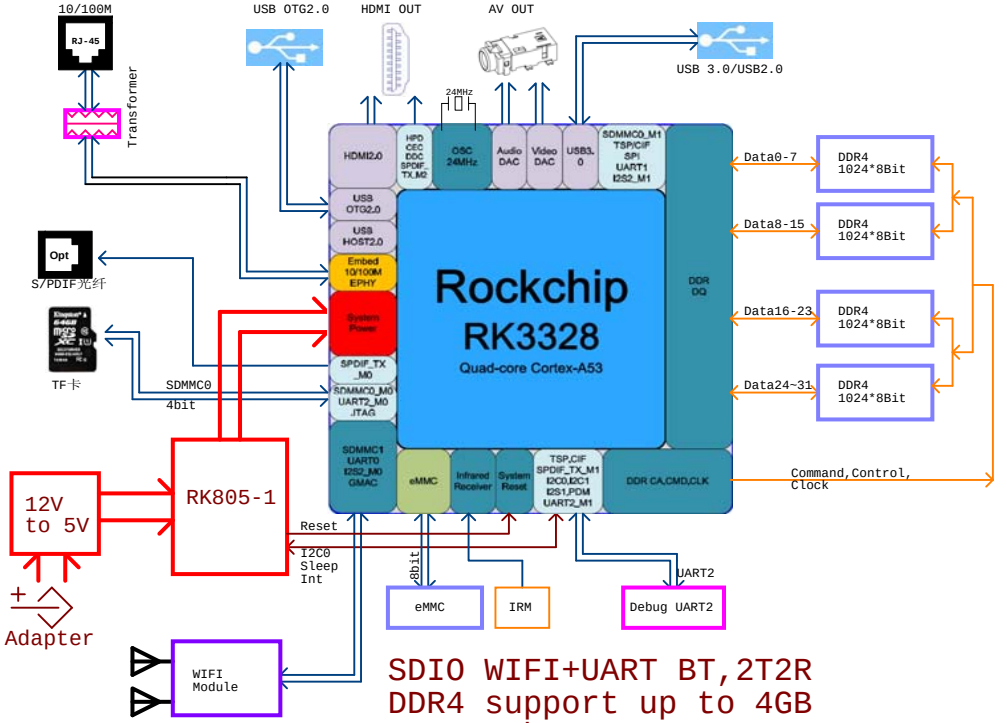
| Version | Date | Author | Change Note | Approved |
|---|---|---|---|---|
| V1.0 | 20170224 | ZDZ | First edictor | |

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics | | | |
| Project: | RK3328_BOX_REF | | |
| File: | Change List | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 2 of 29 |



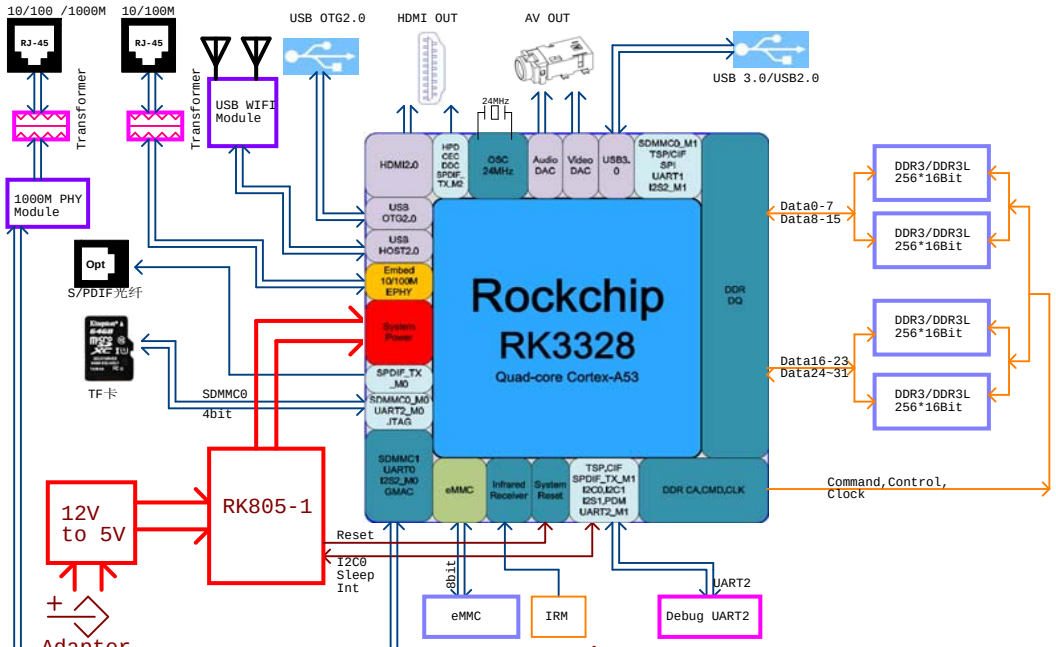

SDIO WIFI+UART BT , 1T1R
DDR3 support 1GB
100M Ethernet

Default config



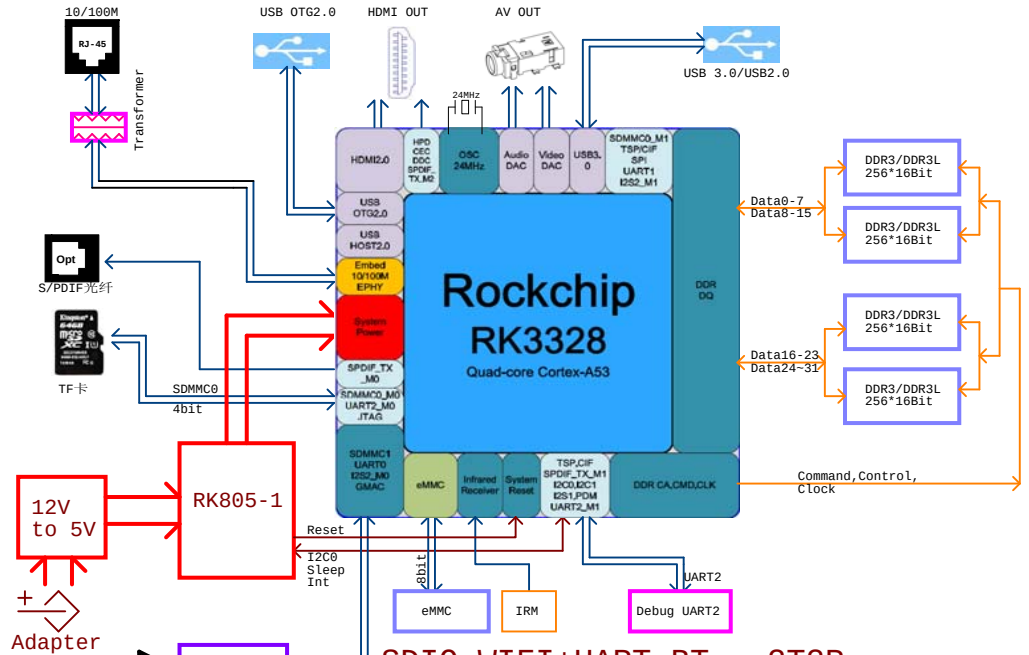

SDIO WIFI+UART BT,2T2R
DDR4 support up to 4GB
100M Ethernet

Config4




USB WIFI/BT ,
DDR3 support up to 2GB
100M+1000M Ethernet

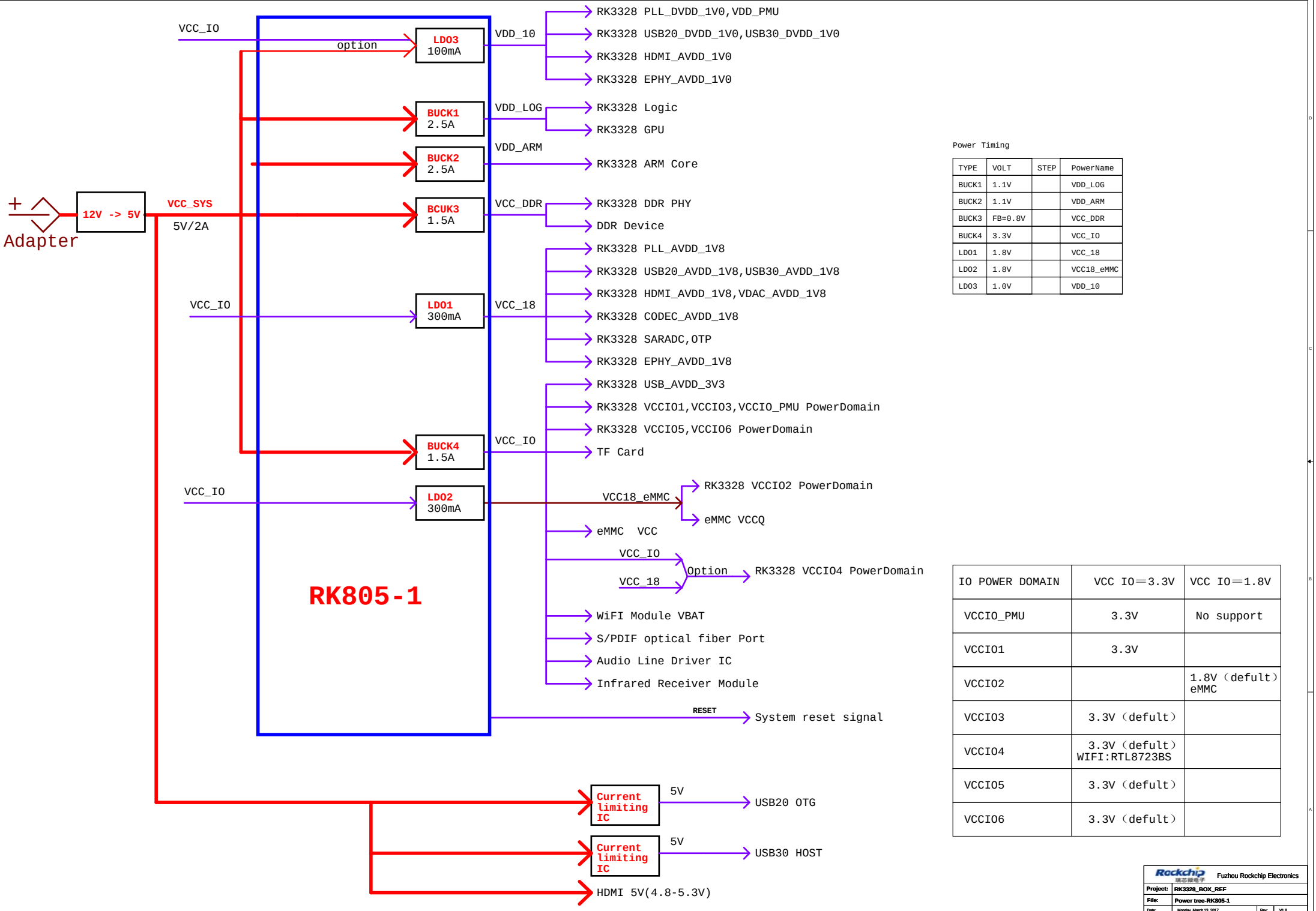
Config2




SDIO WIFI+UART BT , 2T2R
DDR3 support up to 2GB
100M Ethernet

Config3

| | |
|---|---|
| Rockchip | Fuzhou Rockchip Electronics |
| Project: | RK3328_BOX_REF |
| File: | Block Diagram |
| Date: | Friday, February 24, 2017 |
| Designed by: | Joseph |
| Rev: | V1.0 |
| Sheet: | 3 of 29 |

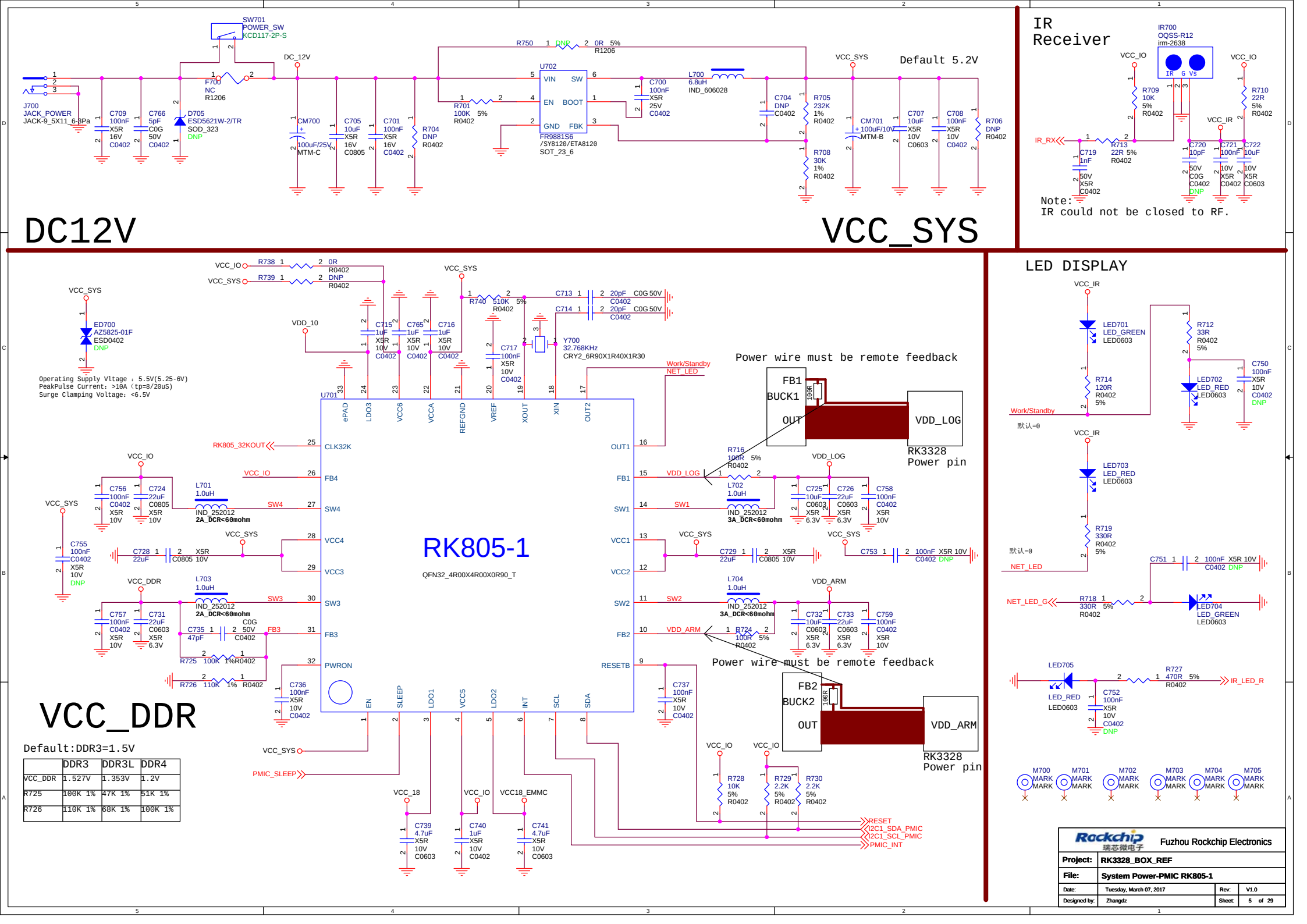



Power Timing

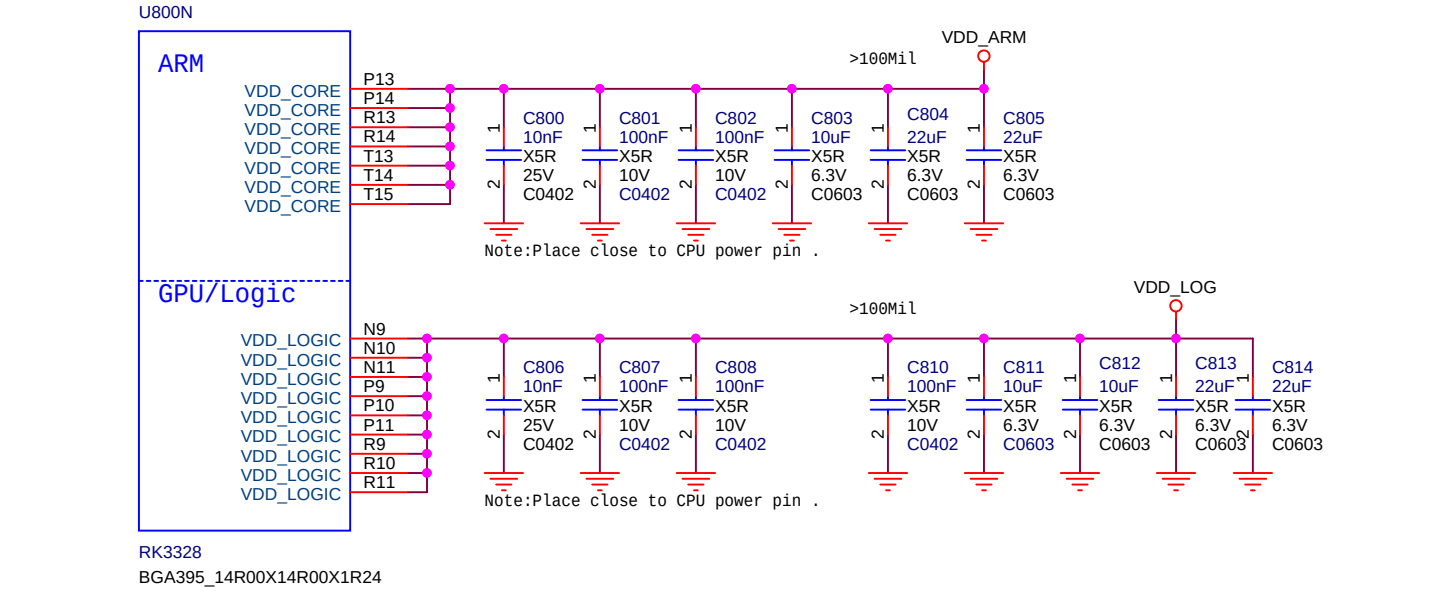
| TYPE | VOLT | STEP | PowerName |
|---|---|---|---|
| BUCK1 | 1.1V | | VDD_LOG |
| BUCK2 | 1.1V | | VDD_ARM |
| BUCK3 | FB=0.8V | | VCC_DDR |
| BUCK4 | 3.3V | | VCC_IO |
| LDO1 | 1.8V | | VCC_18 |
| LDO2 | 1.8V | | VCC18_eMMC |
| LDO3 | 1.0V | | VDD_10 |

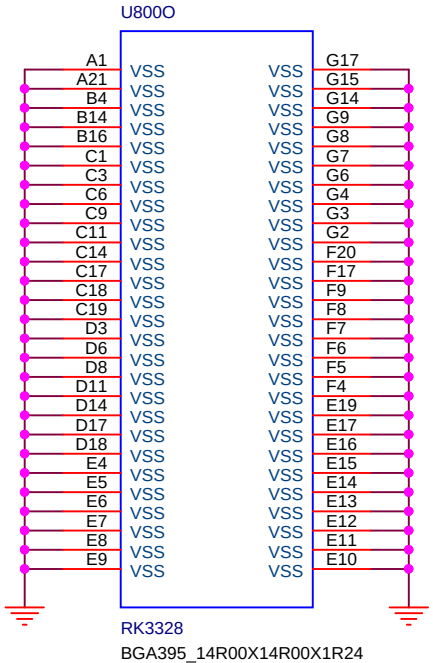
| IO POWER DOMAIN | VCC IO=3.3V | VCC IO=1.8V |
|---|---|---|
| VCCIO_PMU | 3.3V | No support |
| VCCIO1 | 3.3V | |
| VCCIO2 | | 1.8V（defult）<br>eMMC |
| VCCIO3 | 3.3V（defult） | |
| VCCIO4 | 3.3V（defult）<br>WIFI:RTL8723BS | |
| VCCIO5 | 3.3V（defult） | |
| VCCIO6 | 3.3V（defult） | |

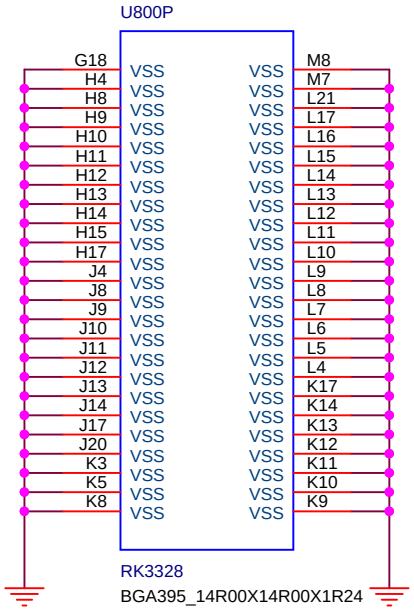
| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | Power tree-RK805-1 | | |
| Date: | Monday, March 13, 2017 | Rev: | V1.0 |
| Designed by: | Zhangqb | Sheet: | 4 of 29 |

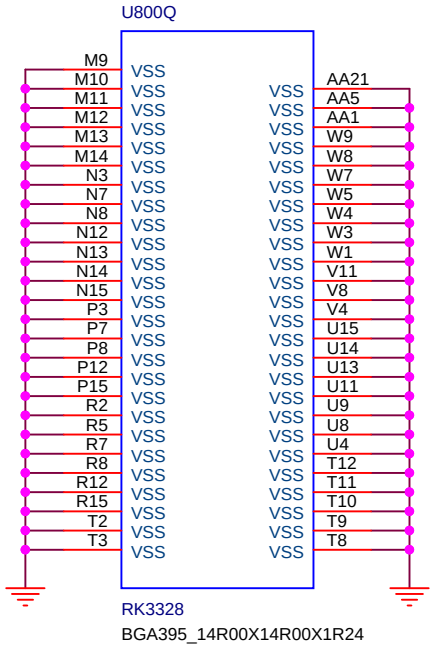



| | DDR3 | DDR3L | DDR4 |
|---|---|---|---|
| VCC_DDR | 1.527V | 1.353V | 1.2V |
| R725 | 100K 1% | 47K 1% | 51K 1% |
| R726 | 110K 1% | 68K 1% | 100K 1% |

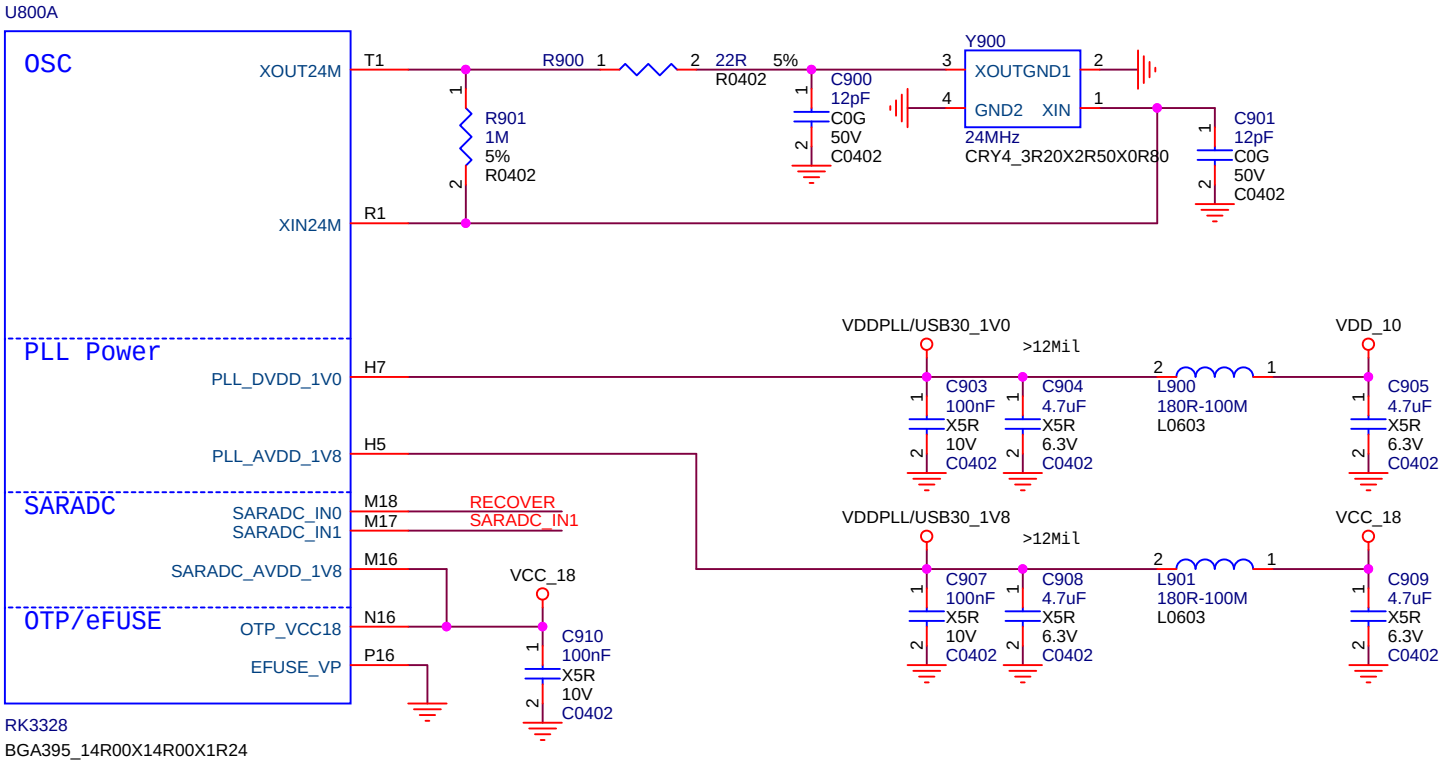


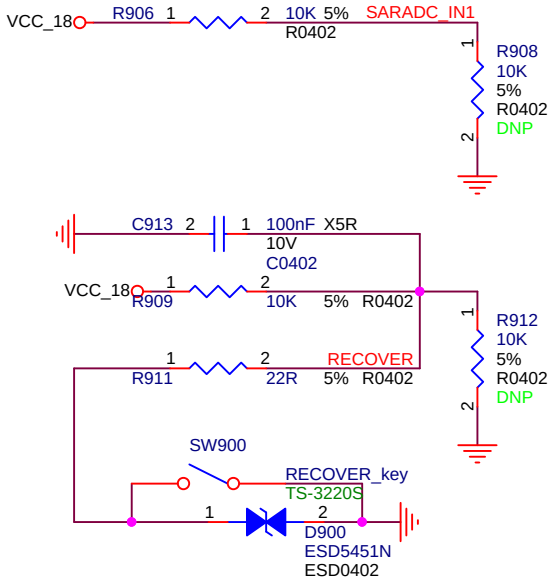



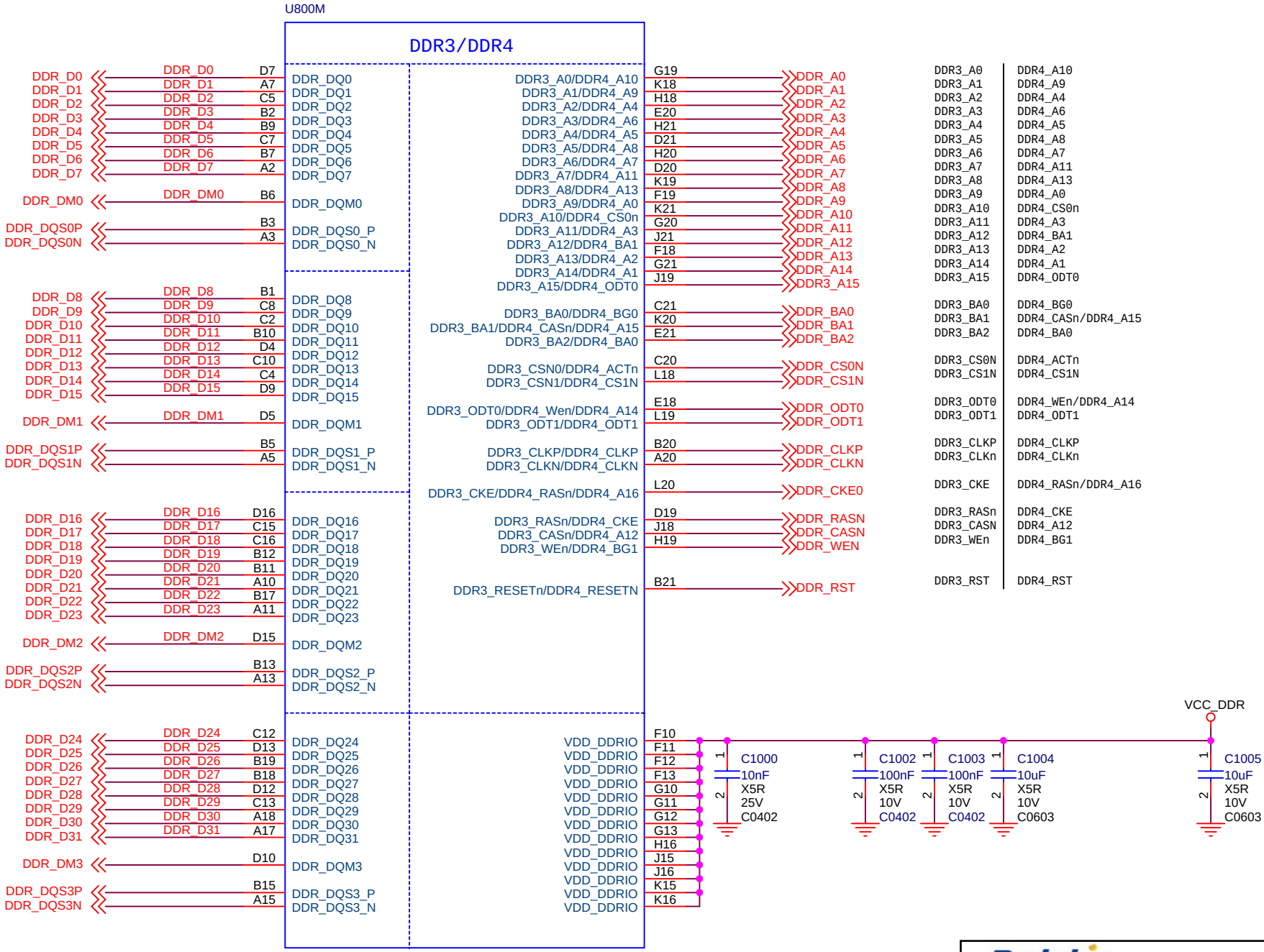

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | RK3328 Power | | |
| Date: | Tuesday, March 07, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 6 of 29 |



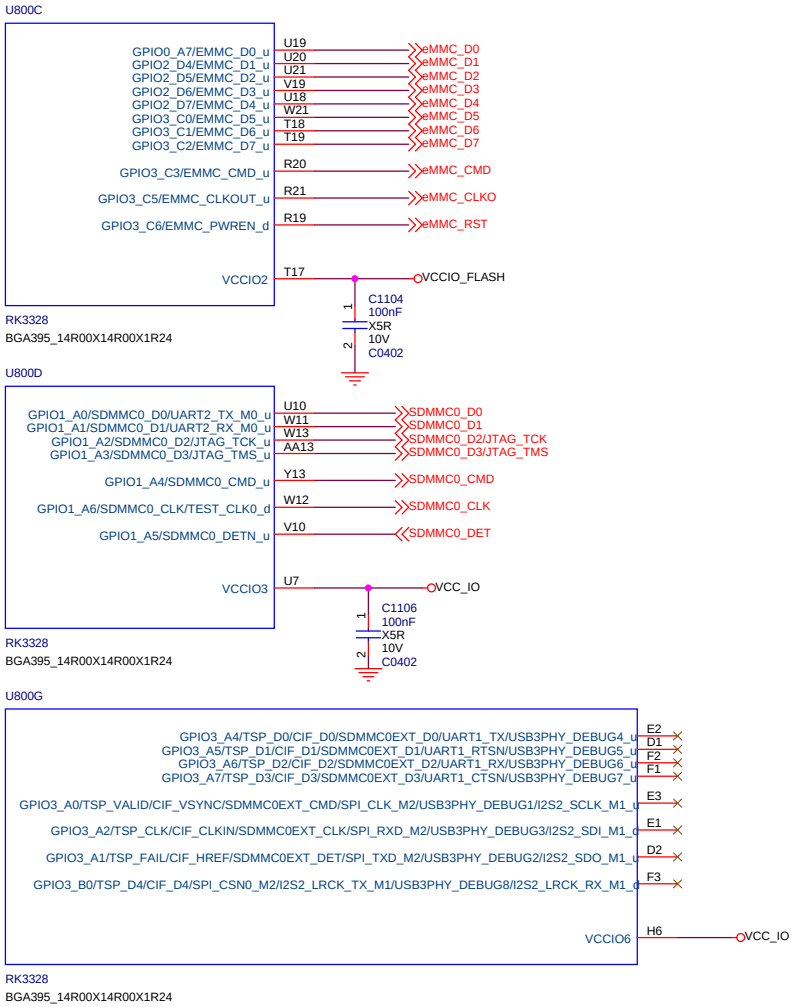




| SARADC_IN0 BOM Ver.. | SARADC_IN1 PCB Ver.. | Pull up | Pull down | |
|---|---|---|---|---|
| Recover | | DNP | 10K | |
| BOM1 | | 110K | 10K | |
| BOM2 | | 100K | 20K | |
| BOM3 | | 100K | 33K | |
| BOM4 | | 36K | 18K | |
| BOM5 | | 51K | 36K | |
| BOM6 | | 51K | 51K | |
| BOM7 | | 36K | 51K | |
| BOM8 | | 18K | 36K | |
| BOM9 | | 33K | 100K | |
| BOM10 | | 20K | 100K | |
| BOM11 | | 10K | 110K | |
| BOM12 | | 10K | DNP | |

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | RK3328 OSC/PLL/OTP/SARADC | | |
| Date: | Tuesday, March 07, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 7 of 29 |




| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | RK3328 DDR Controler | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 8 of 29 |

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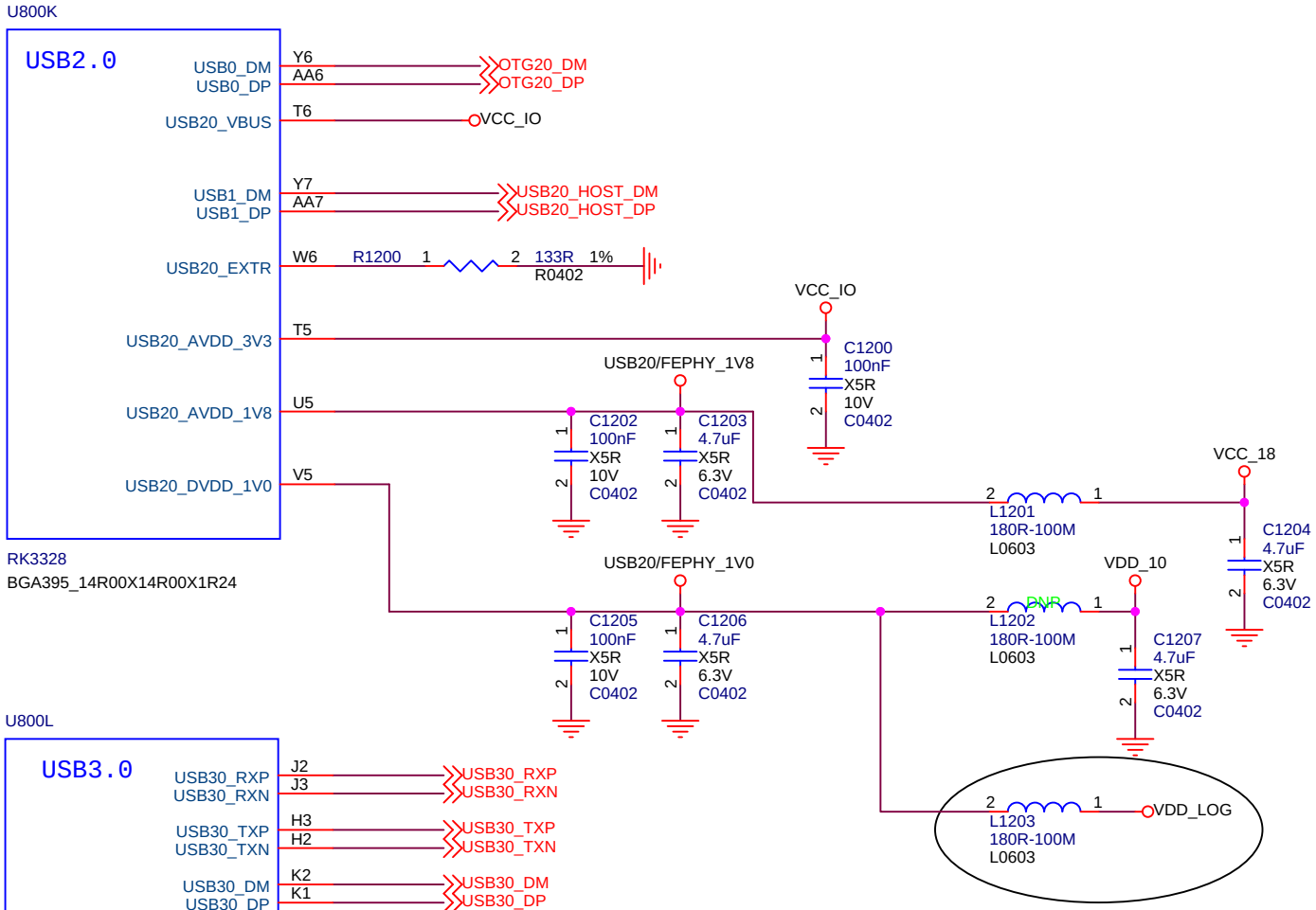
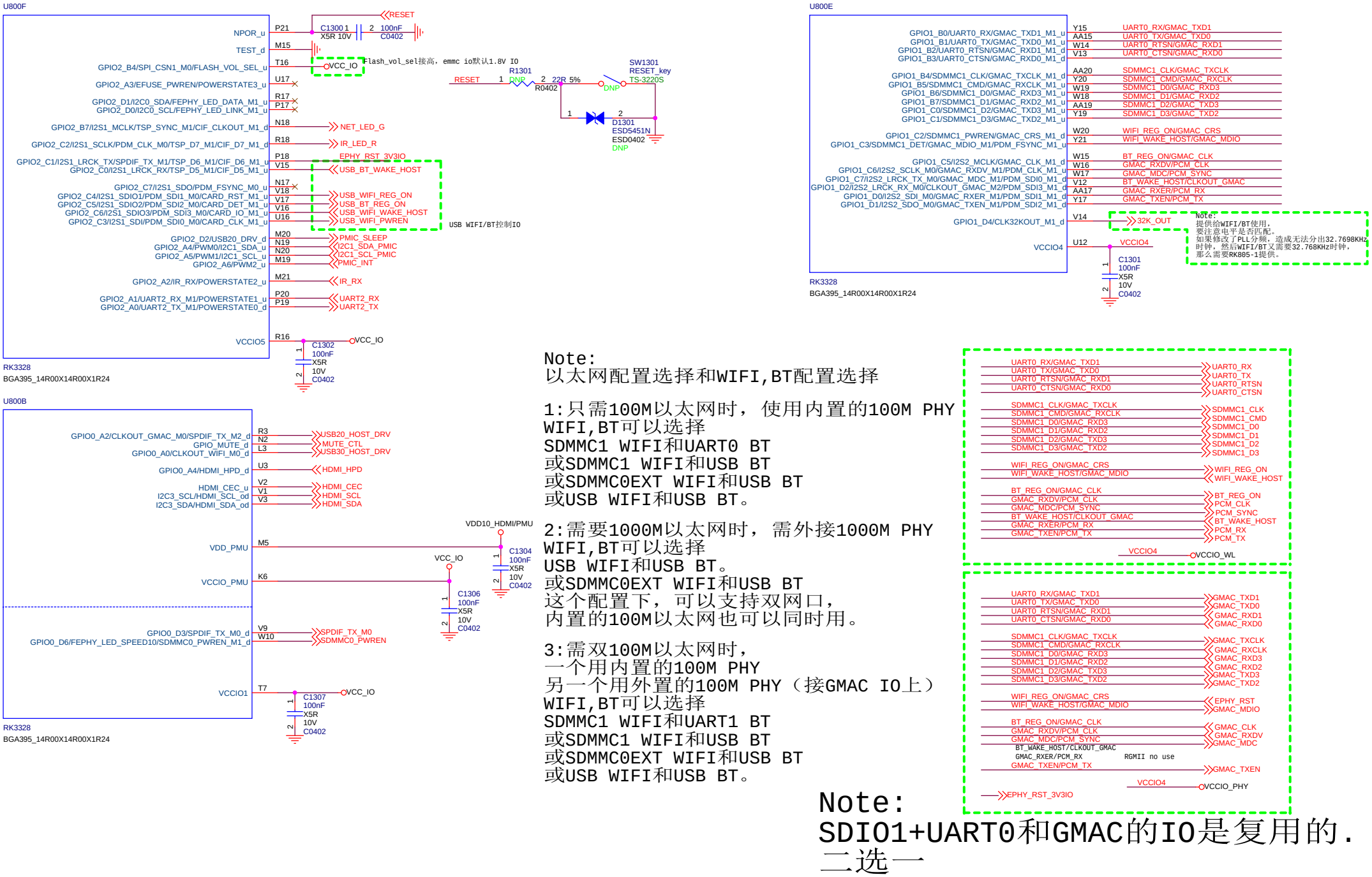
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | RK3328 eMMC Controler/TF | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 9 of 29 |




| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | RK3328 USB2 PHY/USB3 PHY | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 10 of 29 |




Note:
以太网配置选择和WIFI,BT配置选择

1:只需100M以太网时，使用内置的100M PHY
WIFI,BT可以选择
SDMMC1 WIFI和UART0 BT
或SDMMC1 WIFI和USB BT
或SDMMC0EXT WIFI和USB BT
或USB WIFI和USB BT。

2:需要1000M以太网时，需外接1000M PHY
WIFI,BT可以选择
USB WIFI和USB BT。
或SDMMC0EXT WIFI和USB BT
这个配置下，可以支持双网口，
内置的100M以太网也可以同时用。

3:需双100M以太网时，
一个用内置的100M PHY
另一个用外置的100M PHY（接GMAC IO上）
WIFI,BT可以选择
SDMMC1 WIFI和UART1 BT
或SDMMC1 WIFI和USB BT
或SDMMC0EXT WIFI和USB BT
或USB WIFI和USB BT。




Note:
SDIO1+UART0和GMAC的IO是复用的.
二选一

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | RK3328 SDIO/UART/I2C/I2S/IR | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
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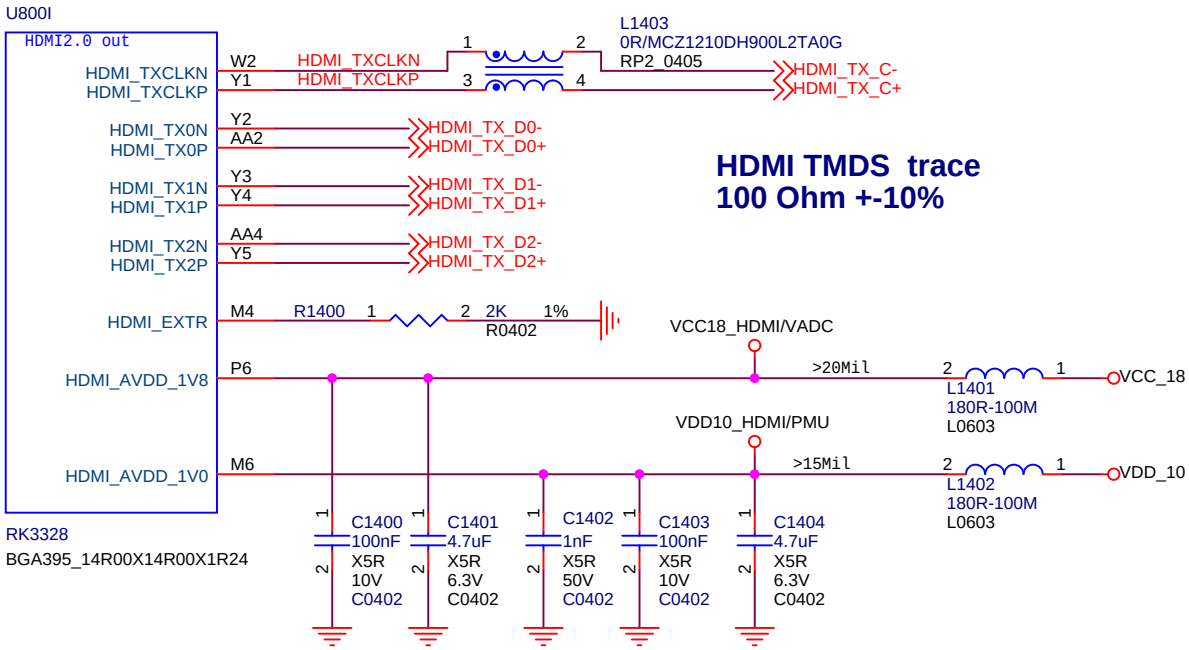
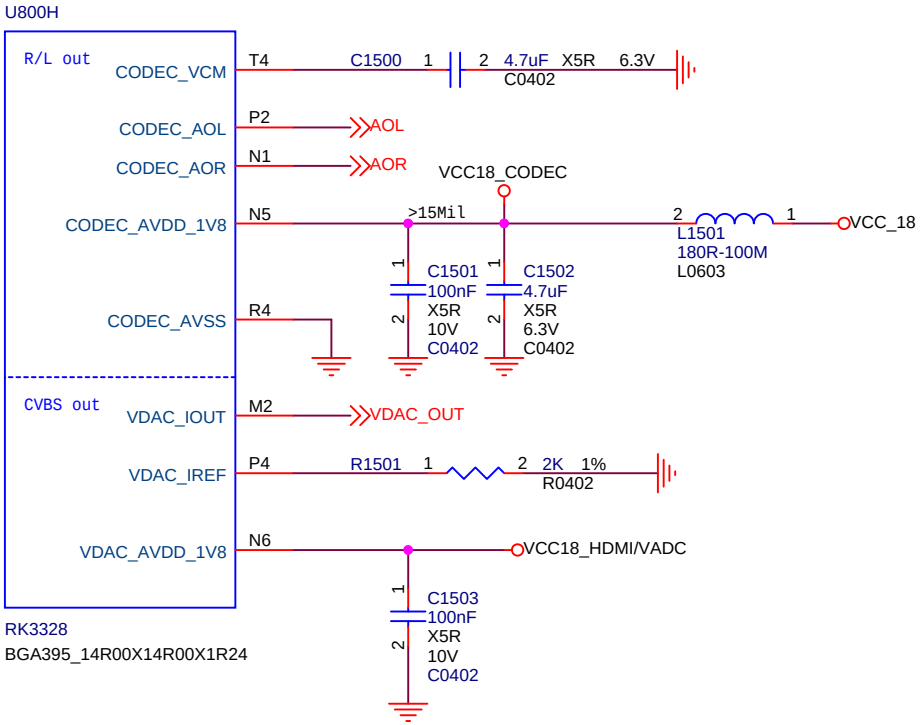
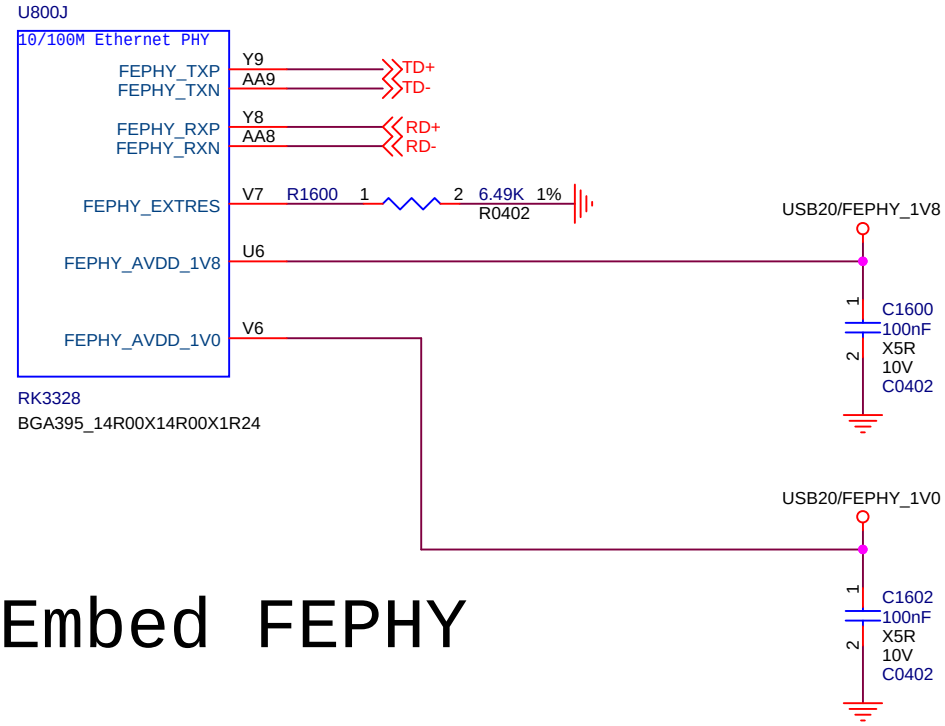



**HDMI TMDS trace**
**100 Ohm +-10%**

| | | | |
|---|---|---|---|
| Fuzhou Rockchip Electronics | | | |
| Project: | RK3328_BOX_REF | | |
| File: | RK3328 HDMI PHY | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 12 of 29 |

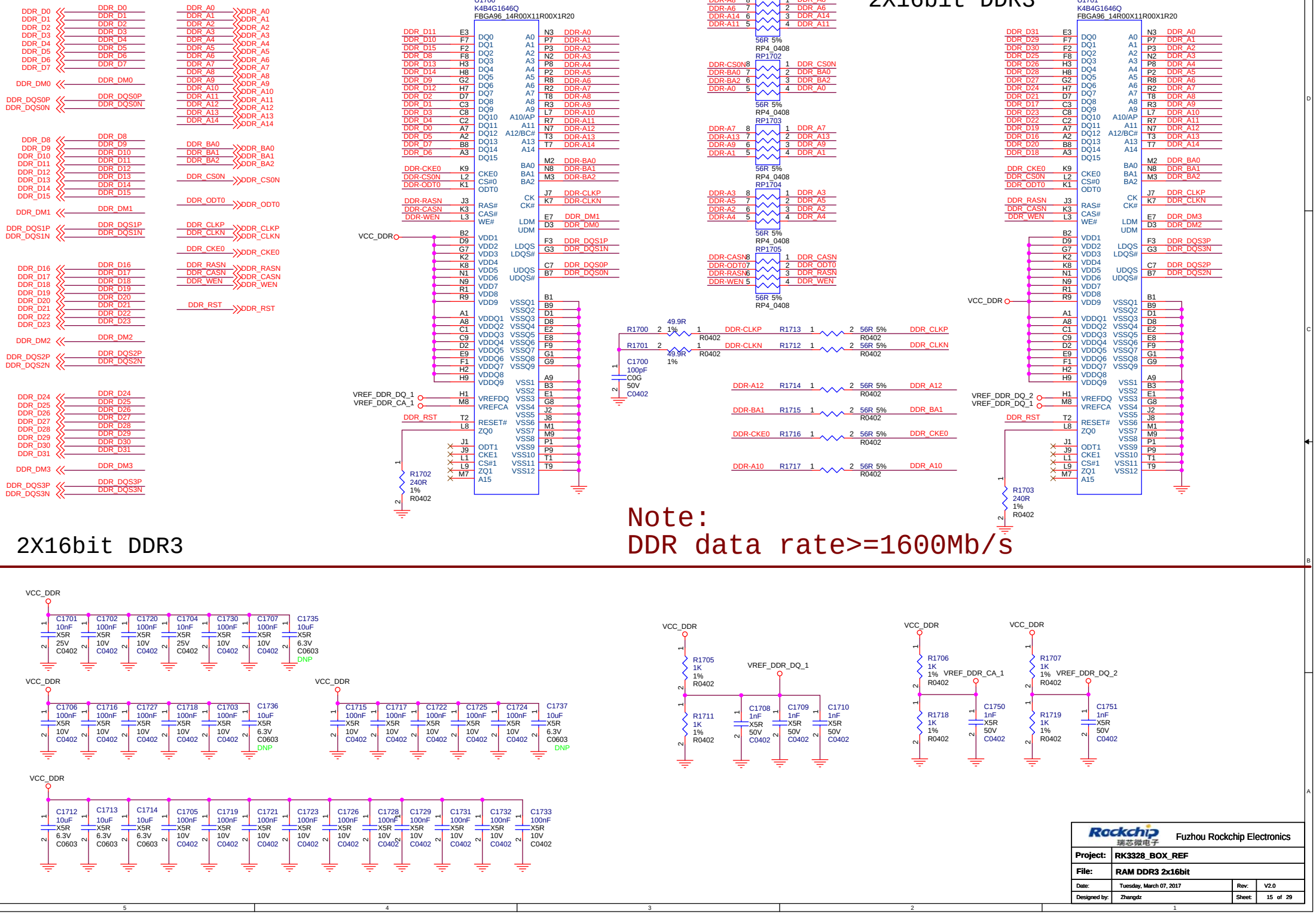



| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| **Project:** | **RK3328_BOX_REF** | | |
| **File:** | **RK3328 AV Interface** | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 13 of 29 |




# Embed FEPHY

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | RK3328 FEPHY | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 14 of 29 |


2X16bit DDR3
U1700
K4B4G1646Q
FBGA96_14R00X11R00X1R20
U1701
K4B4G1646Q
FBGA96_14R00X11R00X1R20
RP1701
RP1702
RP1703
RP1704
RP1705
RP4_0408
56R 5%
DDR_D0
DDR_D1
DDR_D2
DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D7
DDR_DM0
DDR_DQS0P
DDR_DQS0N
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_A14
DDR_D8
DDR_D9
DDR_D10
DDR_D11
DDR_D12
DDR_D13
DDR_D14
DDR_D15
DDR_DM1
DDR_DQS1P
DDR_DQS1N
DDR_BA0
DDR_BA1
DDR_BA2
DDR_CS0N
DDR_ODT0
DDR_CLKP
DDR_CLKN
DDR_CKE0
DDR_RASN
DDR_CASN
DDR_WEN
DDR_RST
DDR_D16
DDR_D17
DDR_D18
DDR_D19
DDR_D20
DDR_D21
DDR_D22
DDR_D23
DDR_DM2
DDR_DQS2P
DDR_DQS2N
DDR_D24
DDR_D25
DDR_D26
DDR_D27
DDR_D28
DDR_D29
DDR_D30
DDR_D31
DDR_DM3
DDR_DQS3P
DDR_DQS3N
VCC_DDR
VREF_DDR_DQ_1
VREF_DDR_CA_1
VREF_DDR_DQ_2
R1700 49.9R 1% R0402
R1701 49.9R 1% R0402
C1700 100pF C0G 50V C0402
R1702 240R 1% R0402
R1703 240R 1% R0402
Note:
DDR data rate>=1600Mb/s
2X16bit DDR3
C1701 10nF X5R 25V C0402
C1702 100nF X5R 10V C0402
C1720 100nF X5R 10V C0402
C1704 10nF X5R 25V C0402
C1730 100nF X5R 10V C0402
C1707 100nF X5R 10V C0402
C1735 10uF X5R 6.3V C0603 DNP
C1706 100nF X5R 10V C0402
C1716 100nF X5R 10V C0402
C1727 100nF X5R 10V C0402
C1718 100nF X5R 10V C0402
C1703 100nF X5R 10V C0402
C1736 10uF X5R 6.3V C0603 DNP
C1715 100nF X5R 10V C0402
C1717 100nF X5R 10V C0402
C1722 100nF X5R 10V C0402
C1725 100nF X5R 10V C0402
C1724 100nF X5R 10V C0402
C1737 10uF X5R 6.3V C0603 DNP
C1712 10uF X5R 6.3V C0603
C1713 10uF X5R 6.3V C0603
C1714 10uF X5R 6.3V C0603
C1705 100nF X5R 10V C0402
C1719 100nF X5R 10V C0402
C1721 100nF X5R 10V C0402
C1723 100nF X5R 10V C0402
C1726 100nF X5R 10V C0402
C1728 100nF X5R 10V C0402
C1729 100nF X5R 10V C0402
C1731 100nF X5R 10V C0402
C1732 100nF X5R 10V C0402
C1733 100nF X5R 10V C0402
R1705 1K 1% R0402
R1711 1K 1% R0402
C1708 1nF X5R 50V C0402
C1709 1nF X5R 50V C0402
C1710 1nF X5R 50V C0402
R1706 1K 1% R0402
R1718 1K 1% R0402
C1750 1nF X5R 50V C0402
R1707 1K 1% R0402
R1719 1K 1% R0402
C1751 1nF X5R 50V C0402
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_REF
File: RAM DDR3 2x16bit
Date: Tuesday, March 07, 2017
Rev: V2.0
Designed by: Zhangdz
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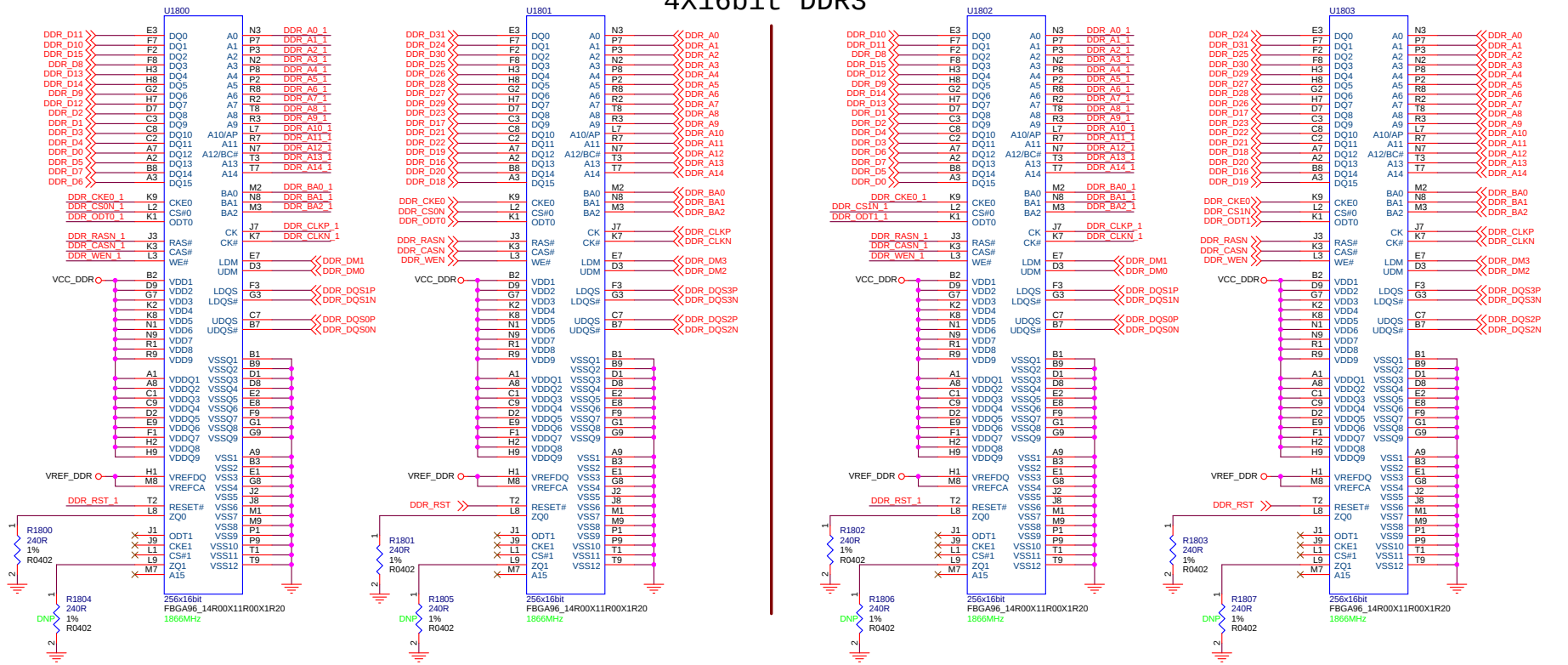
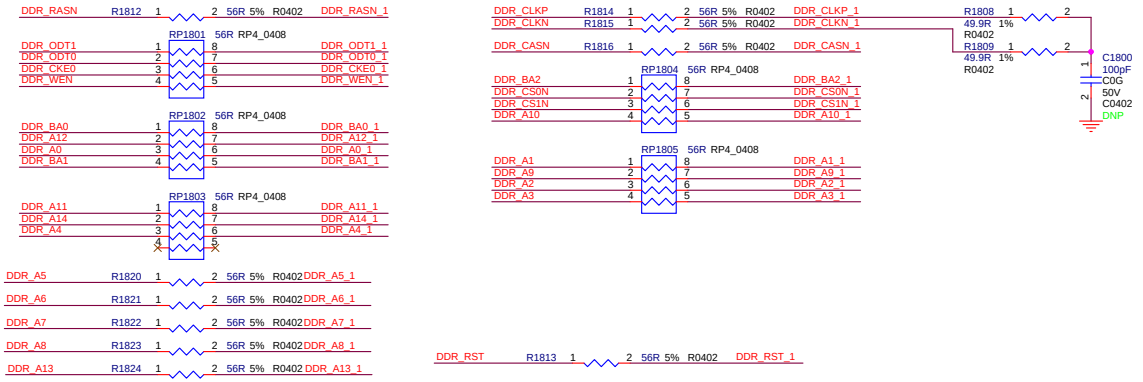
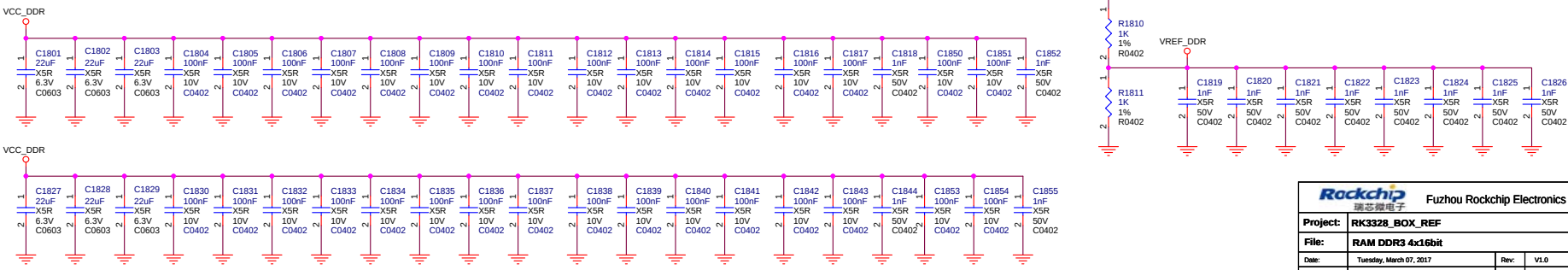
# 4X16bit DDR3




Note:
DDR data rate>=1600Mb/s

## DDR3 FILTER




| | |
|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics |
| Project: | RK3328_BOX_REF |
| File: | RAM DDR3 4x16bit |
| Date: | Tuesday, March 07, 2017 |
| Rev: | V1.0 |
| Designed by: | Zhangdz |
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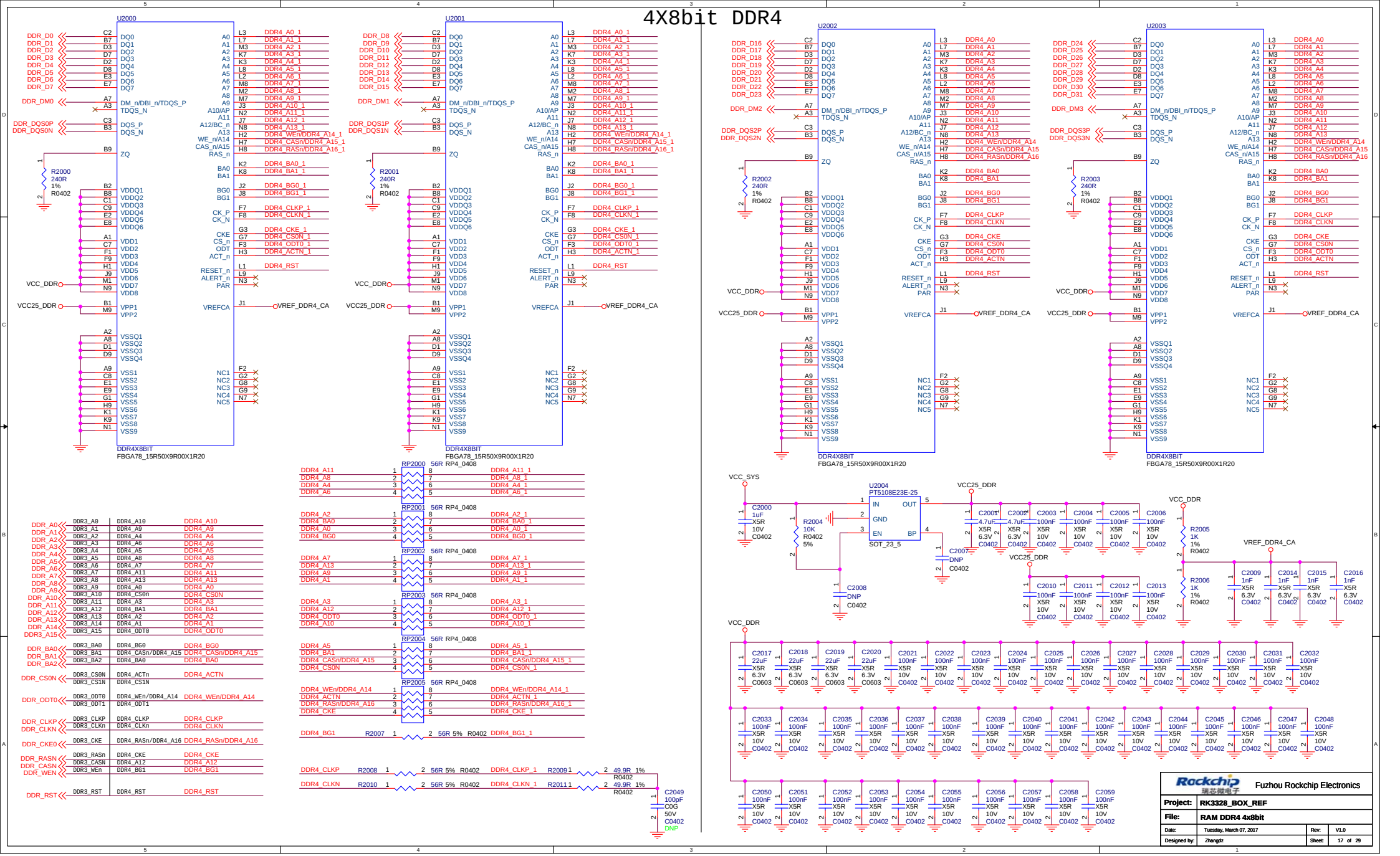
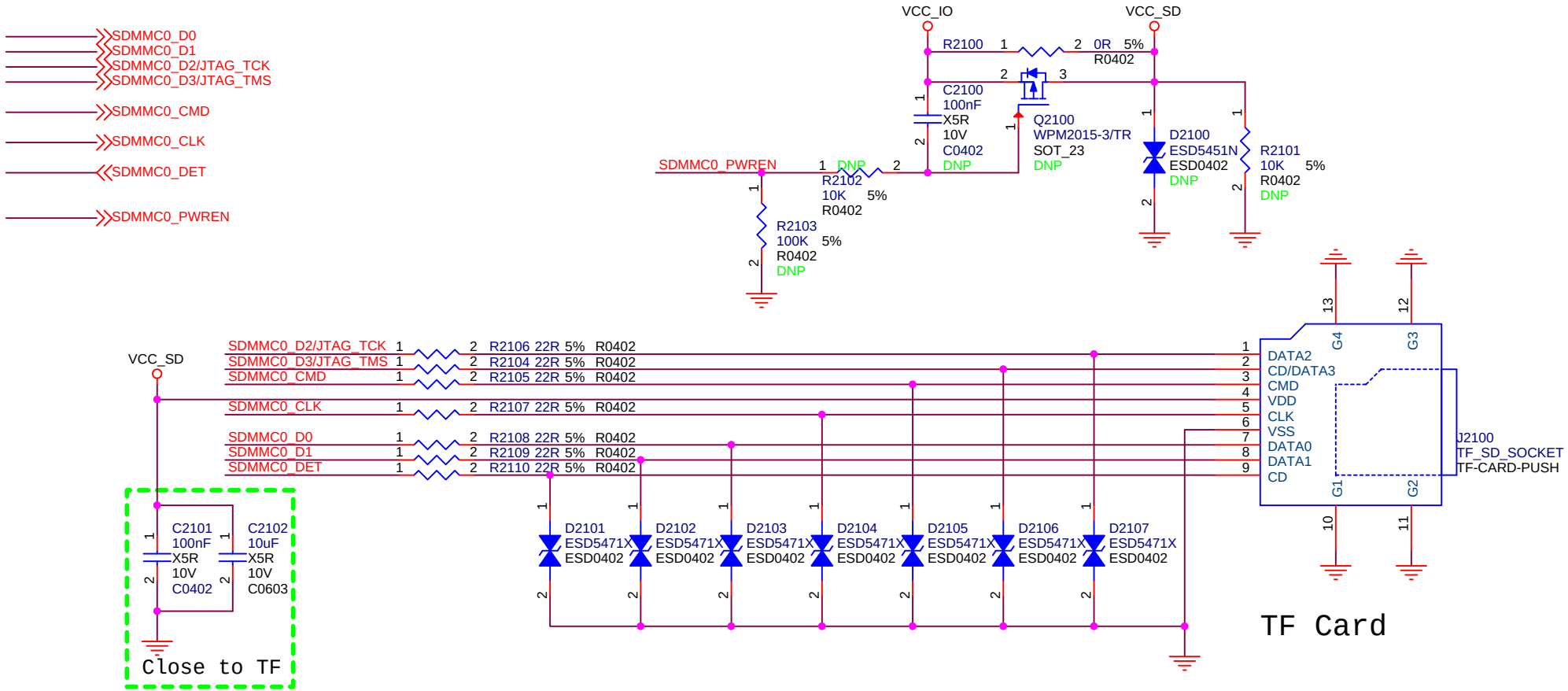
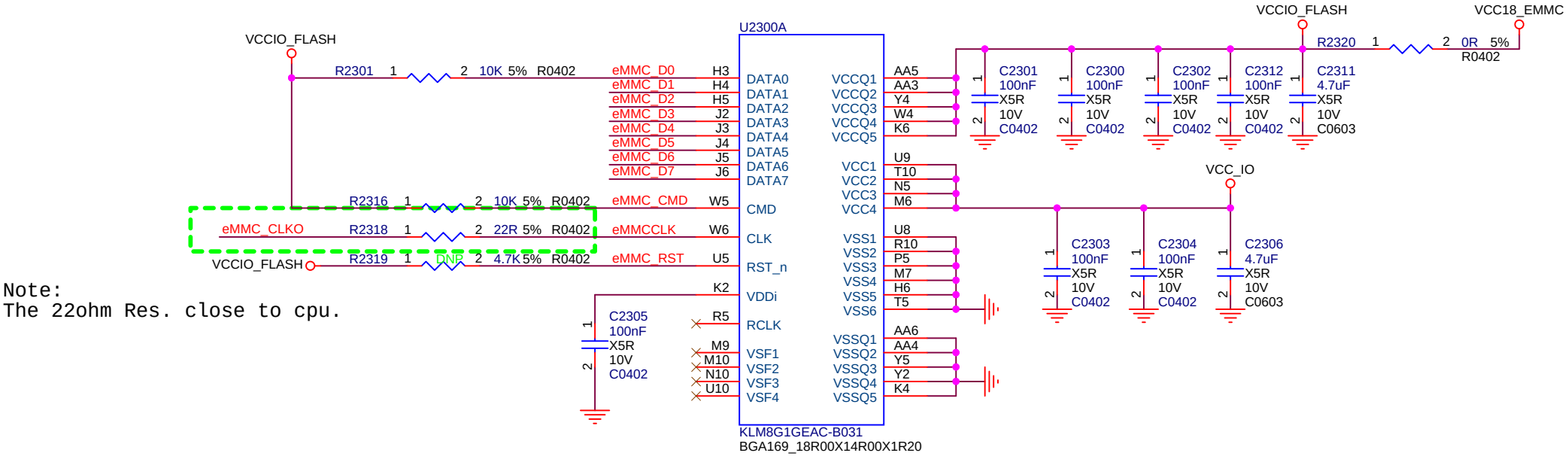
# 4X8bit DDR4

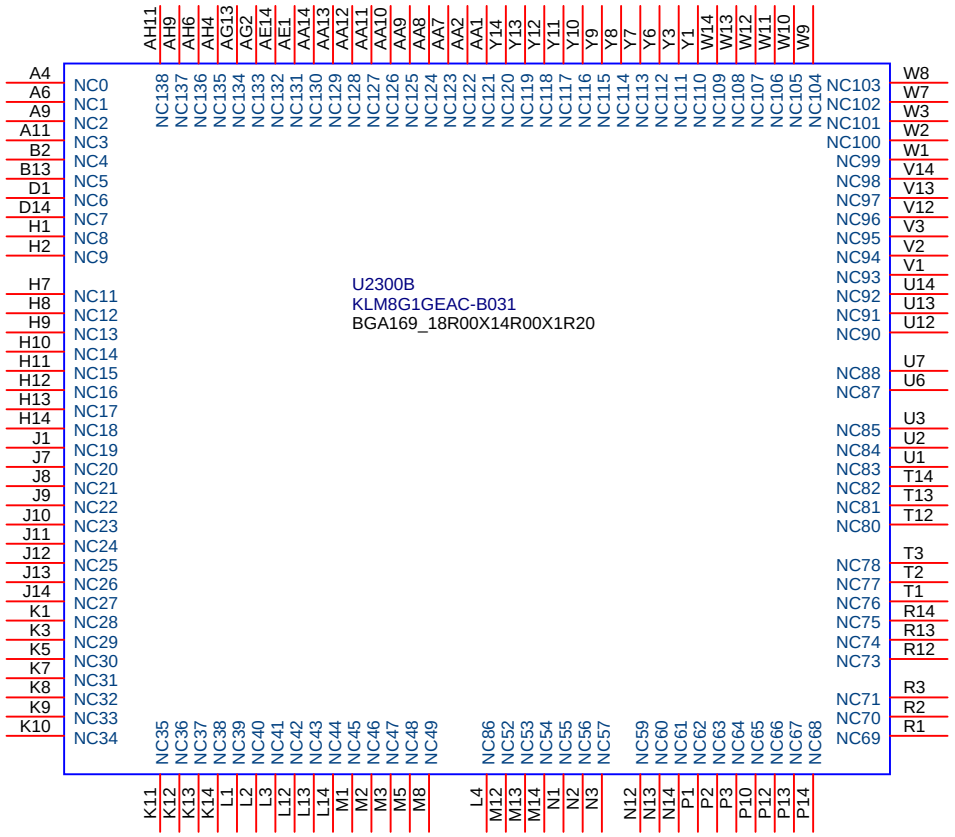

U2000
U2001
U2002
U2003
DDR4X8BIT
FBGA78_15R50X9R00X1R20
RP2000 56R RP4_0408
RP2001 56R RP4_0408
RP2002 56R RP4_0408
RP2003 56R RP4_0408
RP2004 56R RP4_0408
RP2005 56R RP4_0408
U2004
PT5108E23E-25
SOT_23_5
VCC_SYS
VCC25_DDR
VCC_DDR
VREF_DDR4_CA
Fuzhou Rockchip Electronics
Project: RK3328_BOX_REF
File: RAM DDR4 4x8bit
Date: Tuesday, March 07, 2017
Rev: V1.0
Designed by: Zhangdz
Sheet: 17 of 29

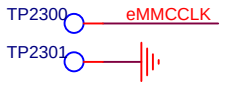



| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | TF/SD Card | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 18 of 29 |

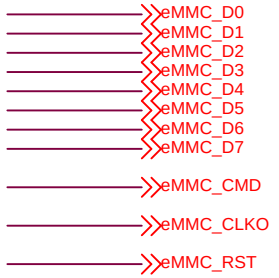



Note:
The 22ohm Res. close to cpu.

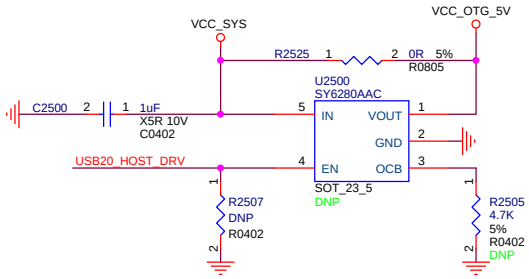


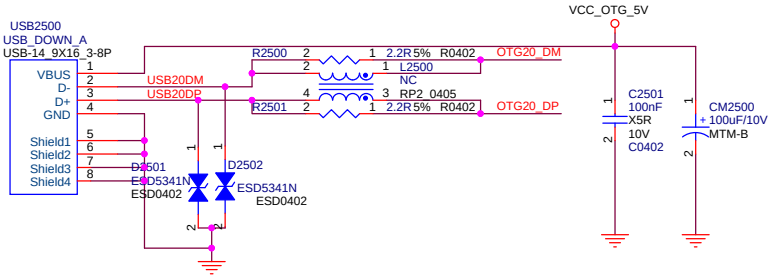




Note:
eMMC Update.

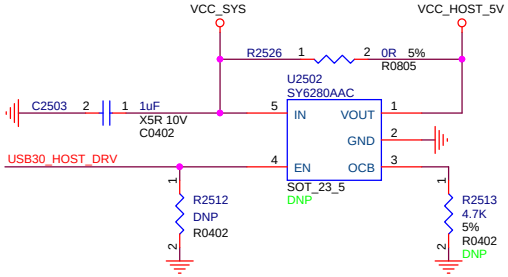


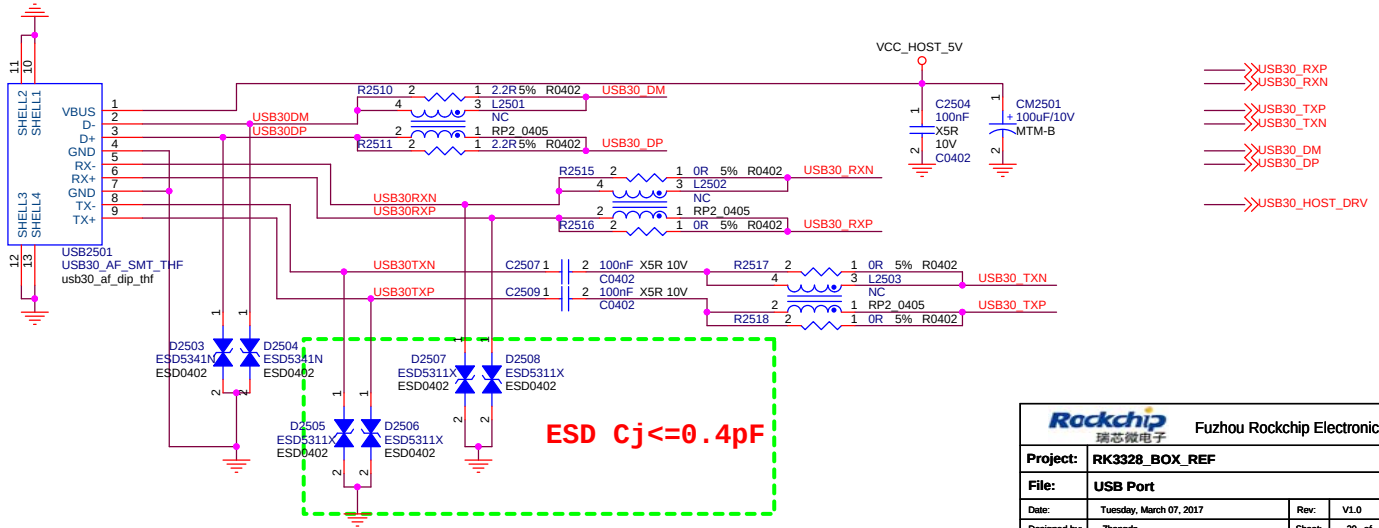

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | Flash-eMMC | | |
| Date: | Tuesday, March 07, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 19 of 29 |





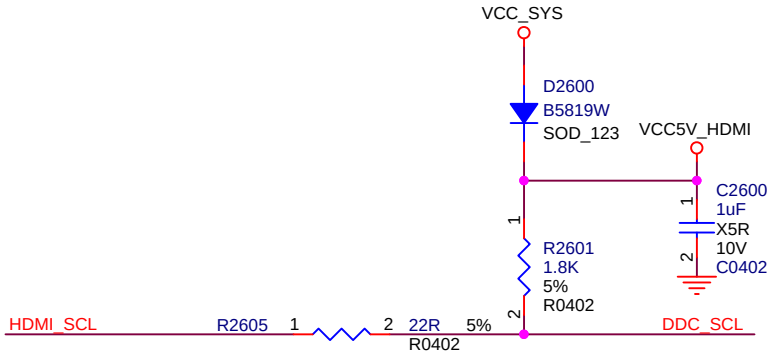


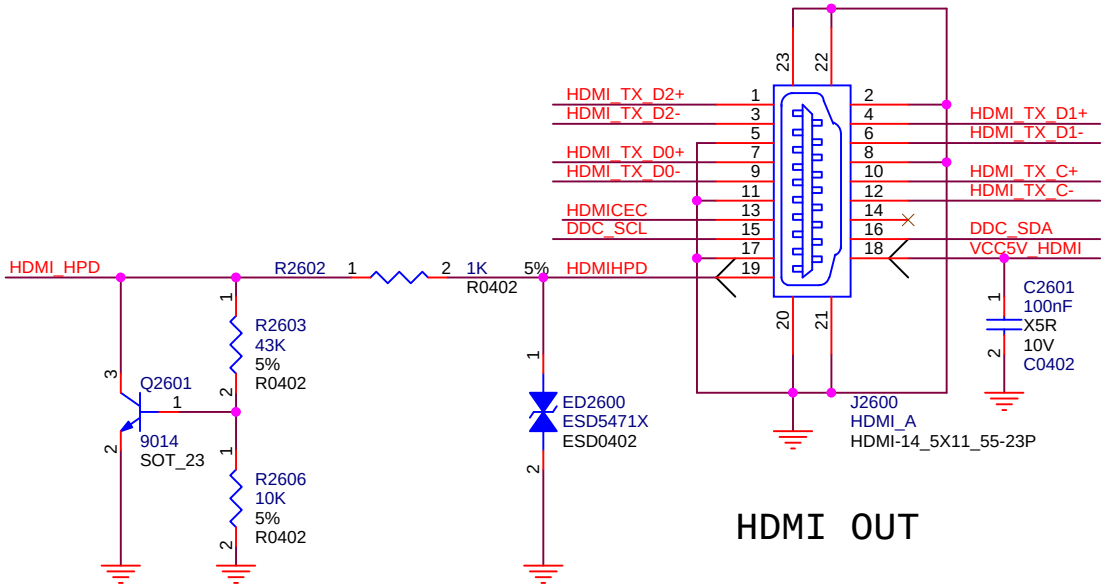





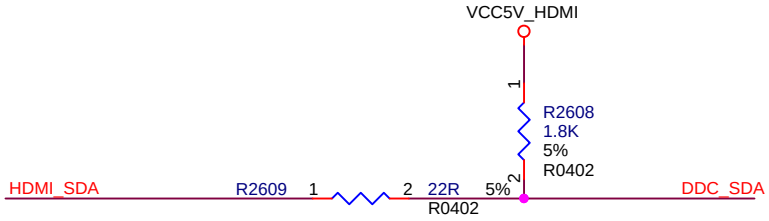


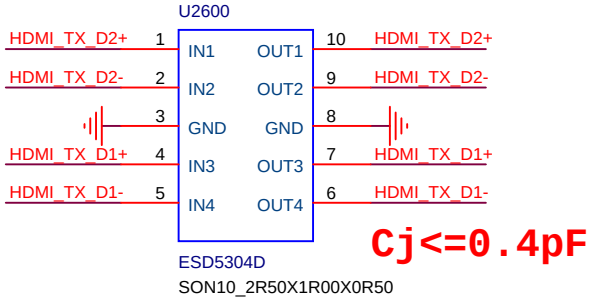
| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | USB Port | | |
| Date: | Tuesday, March 07, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 20 of 29 |



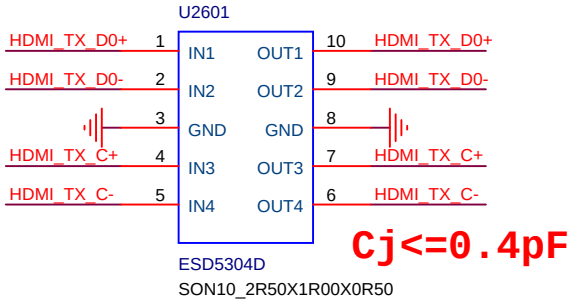




HDMI OUT

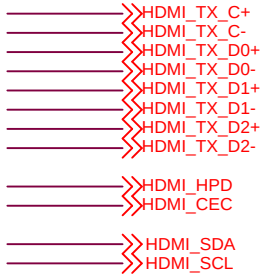


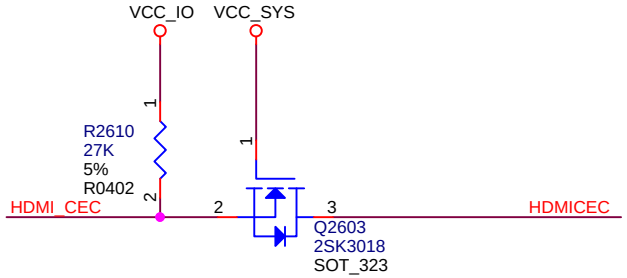



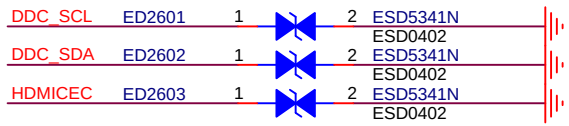

Cj<=0.4pF



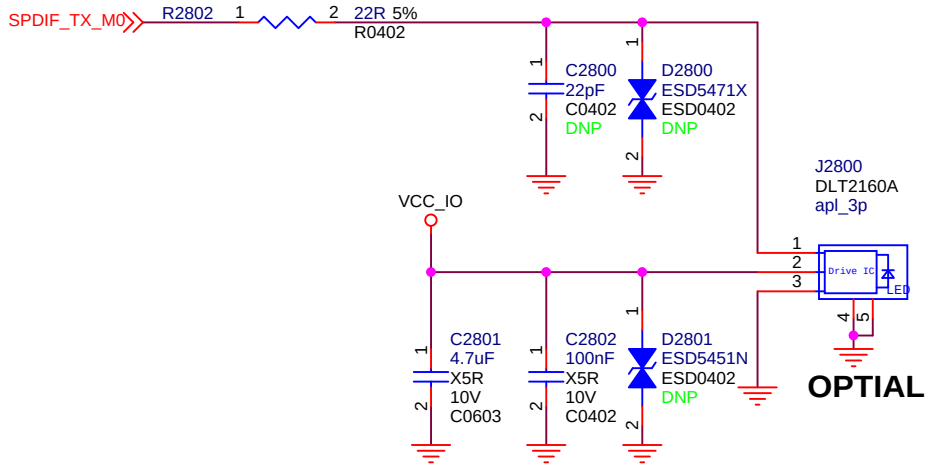

Cj<=0.4pF



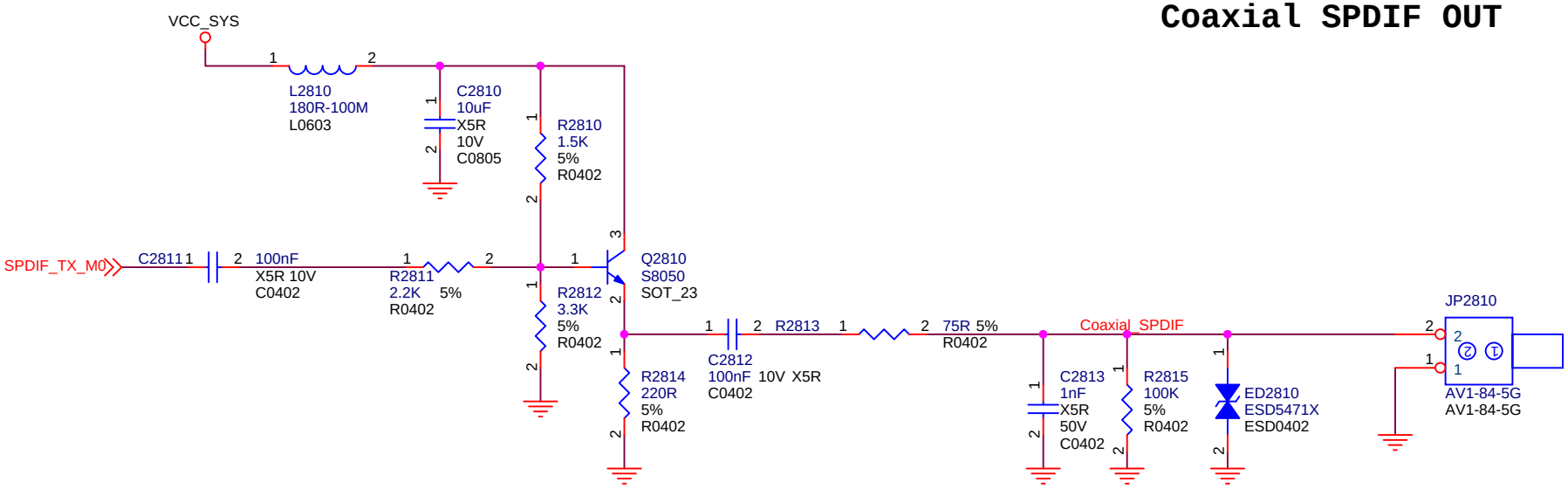




| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | HDMI OUT Port | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 21 of 29 |

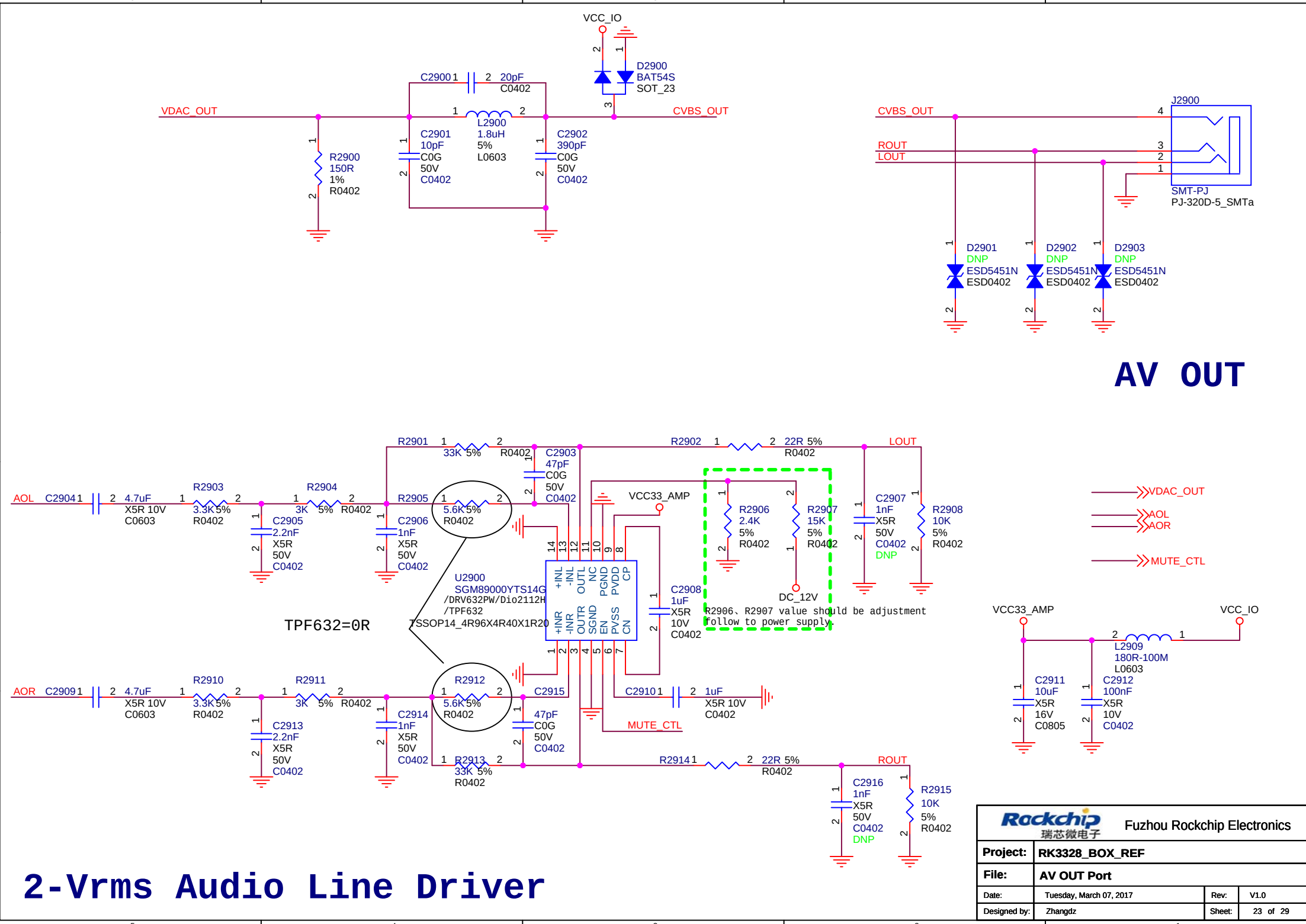


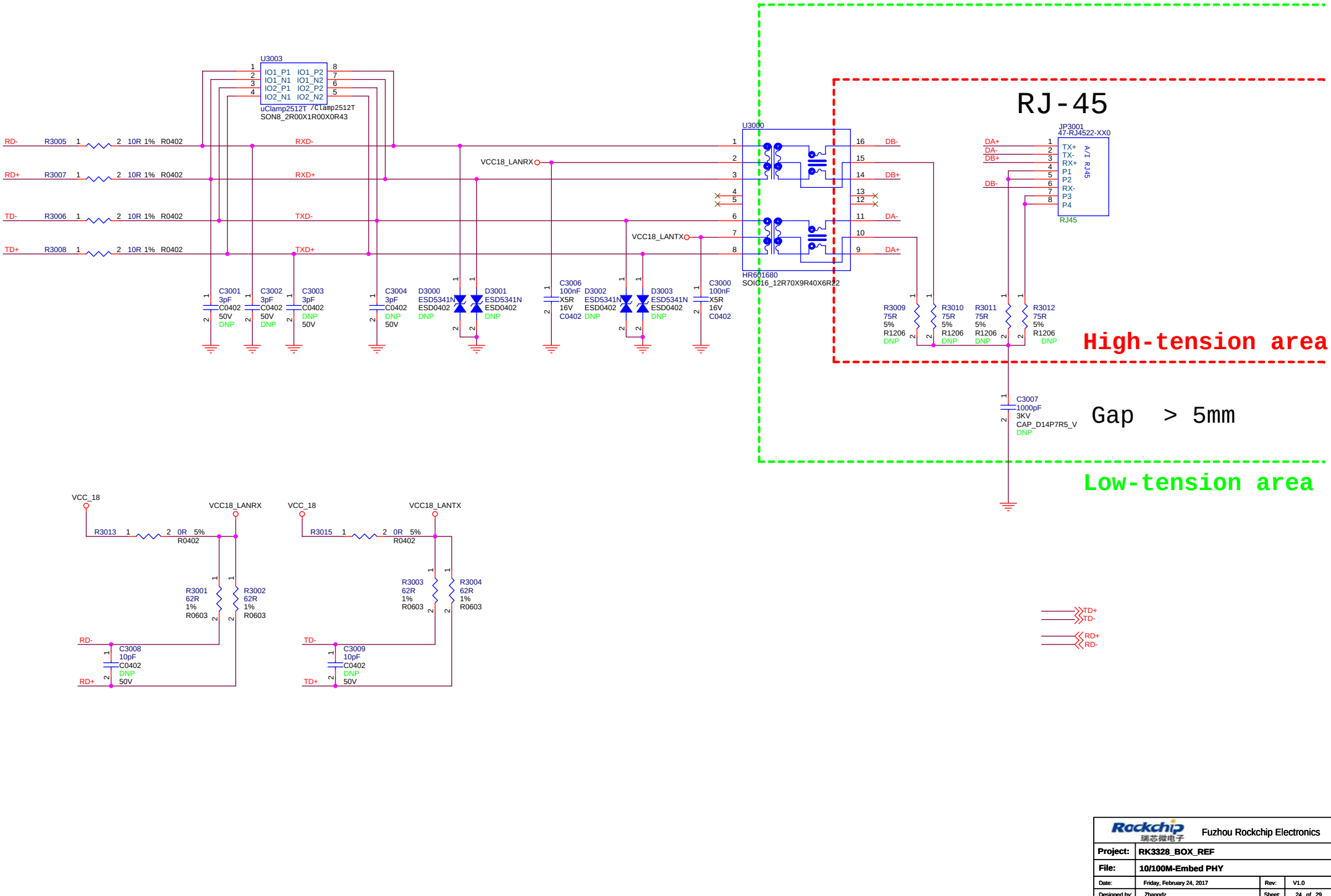

## Optical SPDIF OUT

## Coaxial SPDIF OUT

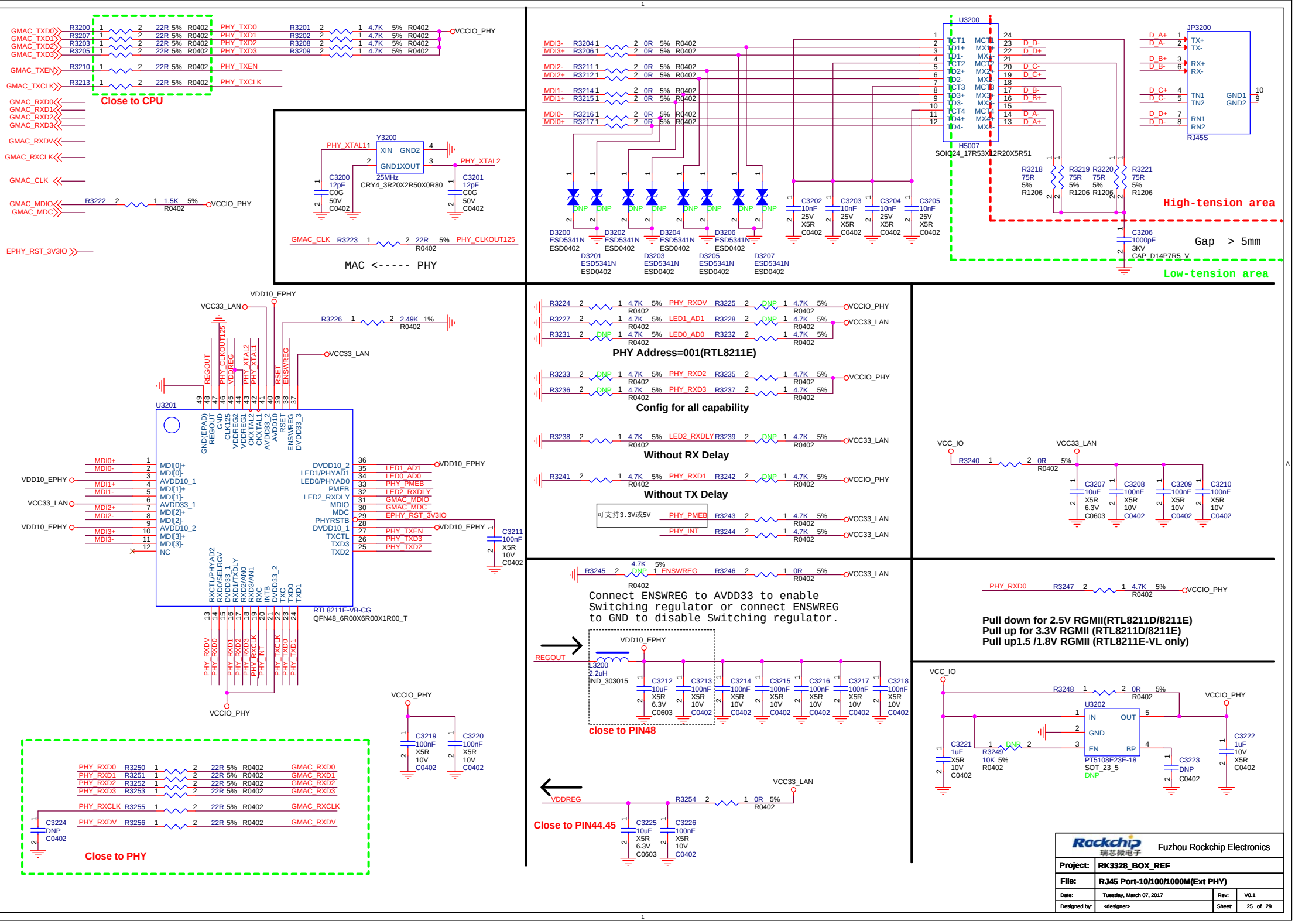


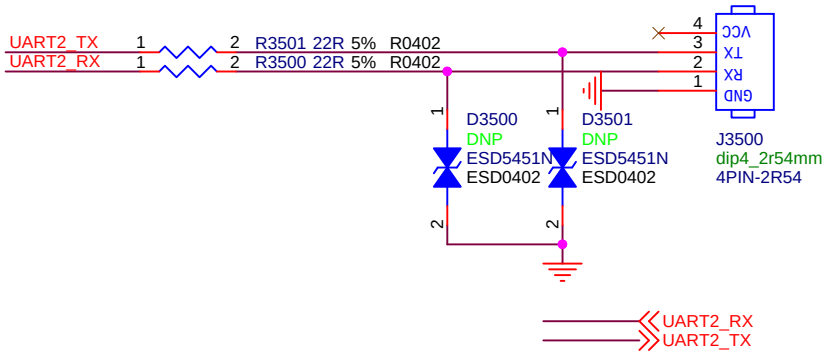

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | S/PDIF Port | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 22 of 29 |


VCC_IO
D2900
BAT54S
SOT_23
C2900 20pF
C0402
VDAC_OUT
CVBS_OUT
L2900
1.8uH
5%
L0603
R2900
150R
1%
R0402
C2901
10pF
C0G
50V
C0402
C2902
390pF
C0G
50V
C0402
CVBS_OUT
ROUT
LOUT
J2900
SMT-PJ
PJ-320D-5_SMTa
D2901
DNP
ESD5451N
ESD0402
D2902
DNP
ESD5451N
ESD0402
D2903
DNP
ESD5451N
ESD0402
AV OUT
AOL
C2904 4.7uF
X5R 10V
C0603
R2903
3.3K 5%
R0402
R2904
3K 5% R0402
C2905
2.2nF
X5R
50V
C0402
R2905
5.6K 5%
R0402
C2906
1nF
X5R
50V
C0402
R2901
33K 5%
R0402
C2903
47pF
C0G
50V
C0402
R2902
22R 5%
R0402
LOUT
VCC33_AMP
R2906
2.4K
5%
R0402
R2907
15K
5%
R0402
DC_12V
C2907
1nF
X5R
50V
C0402
DNP
R2908
10K
5%
R0402
U2900
SGM89000YTS14G
/DRV632PW/Dio2112H
/TPF632
TSSOP14_4R96X4R40X1R20
+INL
-INL
OUTL
NC
PGND
PVDD
CP
+INR
-INR
OUTR
SGND
EN
PVSS
CN
C2908
1uF
X5R
10V
C0402
R2906、R2907 value should be adjustment follow to power supply.
TPF632=0R
VDAC_OUT
AOL
AOR
MUTE_CTL
VCC33_AMP
VCC_IO
L2909
180R-100M
L0603
C2911
10uF
X5R
16V
C0805
C2912
100nF
X5R
10V
C0402
AOR
C2909 4.7uF
X5R 10V
C0603
R2910
3.3K 5%
R0402
R2911
3K 5% R0402
C2913
2.2nF
X5R
50V
C0402
R2912
5.6K 5%
R0402
C2914
1nF
X5R
50V
C0402
C2915
47pF
C0G
50V
C0402
C2910 1uF
X5R 10V
C0402
MUTE_CTL
R2913
33K 5%
R0402
R2914 22R 5%
R0402
ROUT
C2916
1nF
X5R
50V
C0402
DNP
R2915
10K
5%
R0402
2-Vrms Audio Line Driver
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3328_BOX_REF
File: AV OUT Port
Date: Tuesday, March 07, 2017
Rev: V1.0
Designed by: Zhangdz
Sheet: 23 of 29



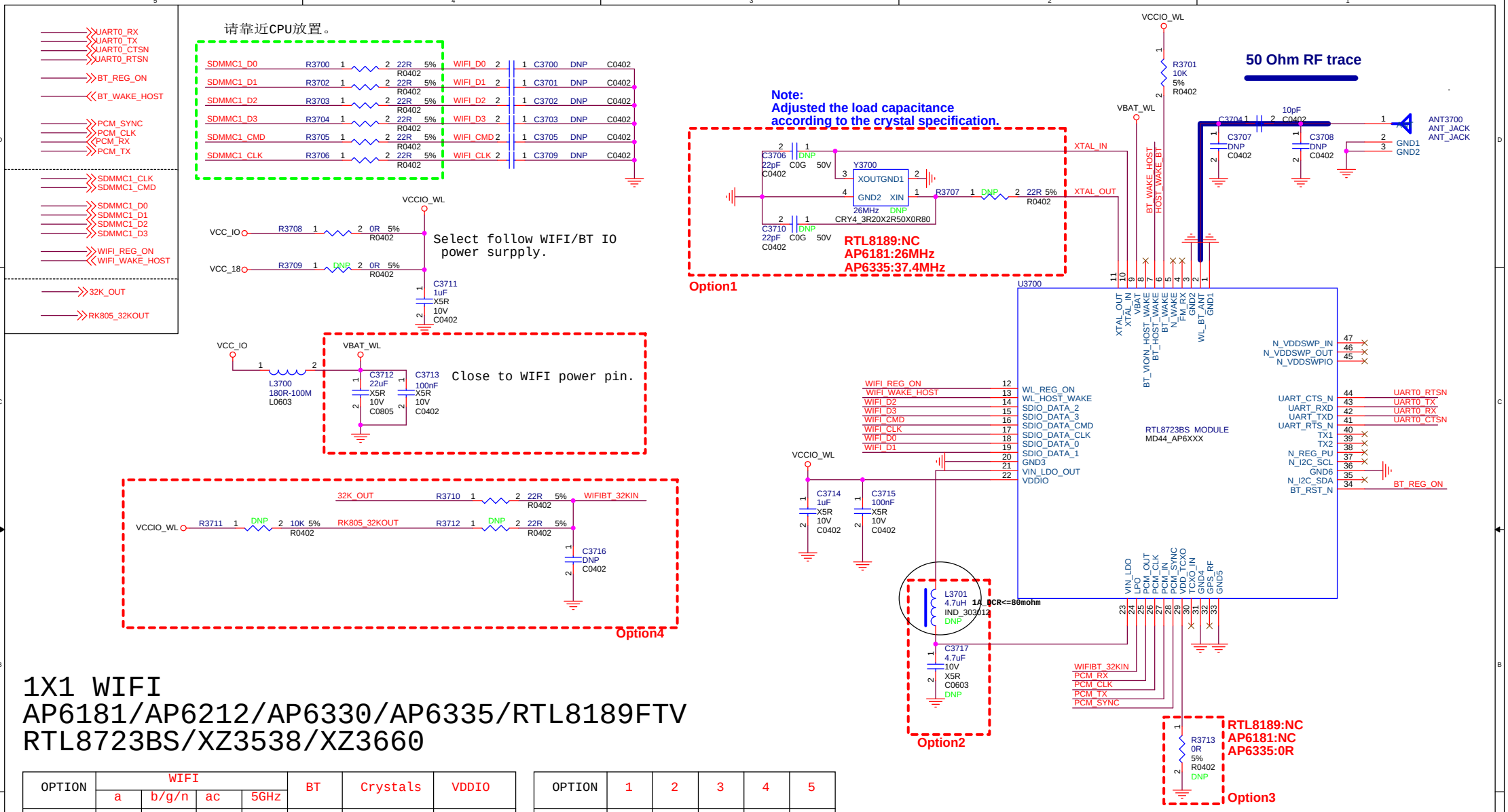

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | 10/100M-Embed PHY | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | Zhangdz | Sheet: | 24 of 29 |


Close to CPU
MAC <----- PHY
High-tension area
Low-tension area
Gap > 5mm
PHY Address=001(RTL8211E)
Config for all capability
Without RX Delay
Without TX Delay
Connect ENSWREG to AVDD33 to enable
Switching regulator or connect ENSWREG
to GND to disable Switching regulator.
close to PIN48
Close to PIN44.45
Close to PHY
Pull down for 2.5V RGMII(RTL8211D/8211E)
Pull up for 3.3V RGMII (RTL8211D/8211E)
Pull up1.5 /1.8V RGMII (RTL8211E-VL only)
RTL8211E-VB-CG
QFN48_6R00X6R00X1R00_T
Fuzhou Rockchip Electronics
Project: RK3328_BOX_REF
File: RJ45 Port-10/100/1000M(Ext PHY)
Date: Tuesday, March 07, 2017
Rev: V0.1
Designed by: <designer>
Sheet: 25 of 29




# Debug UART2

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | RK3328_BOX_REF | | |
| File: | Debug UART2/JTAG | | |
| Date: | Friday, February 24, 2017 | Rev: | V1.0 |
| Designed by: | <designer> | Sheet: | 26 of 29 |

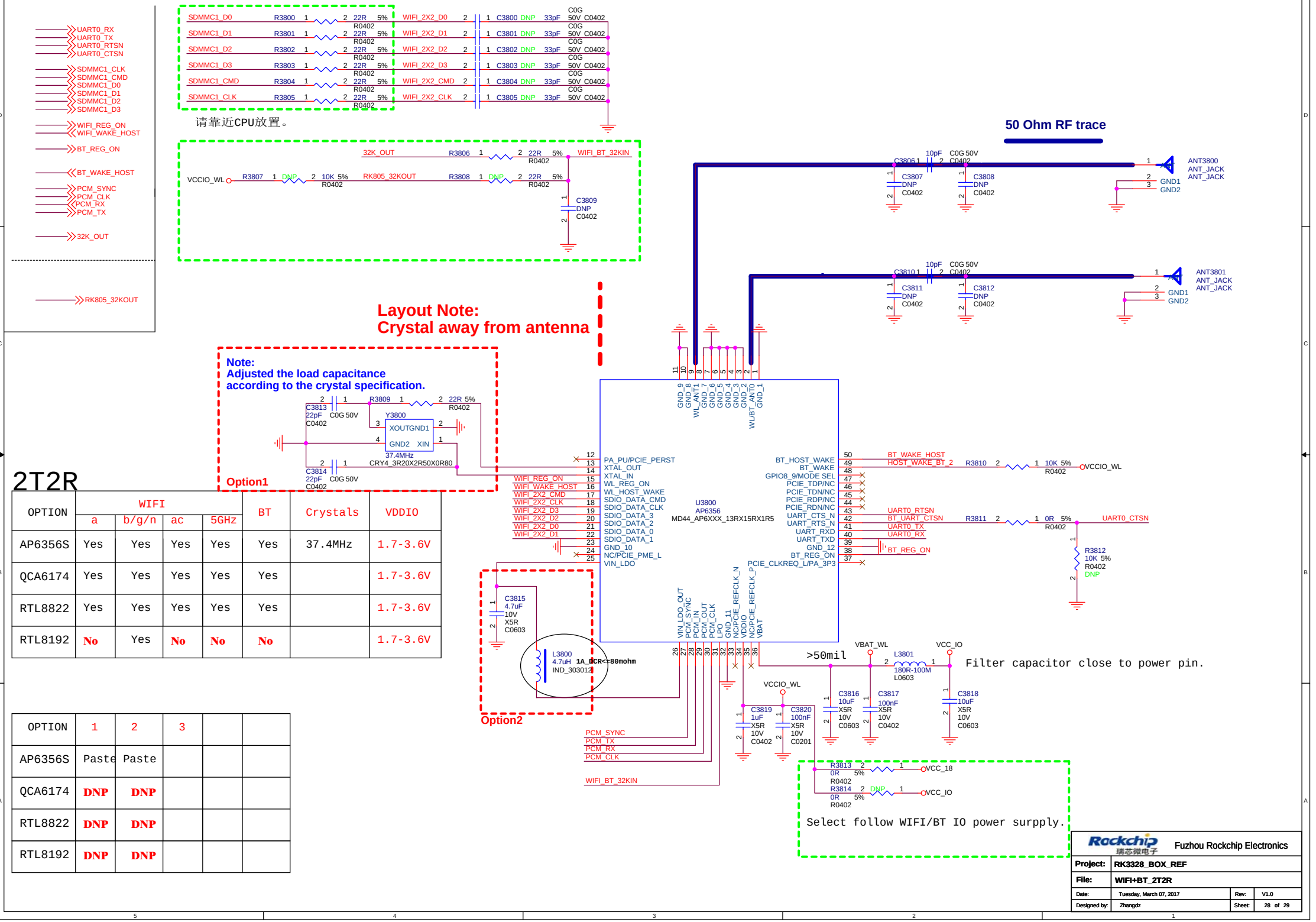



# 1X1 WIFI
# AP6181/AP6212/AP6330/AP6335/RTL8189FTV
# RTL8723BS/XZ3538/XZ3660

| OPTION | WIFI | | | | BT | Crystals | VDDIO |
|---|---|---|---|---|---|---|---|
| | a | b/g/n | ac | 5GHz | | | |
| AP6181 | No | Yes | No | No | No | 26MHz | 1.71-3.6V |
| AP6212<br>XZ3538 | No | Yes | No | No | Yes | 26MHz | 1.71-3.6V |
| AP6330<br>XZ3660 | Yes | Yes | No | Yes | Yes | 26MHz | 1.2-2.9V |
| AP6335 | Yes | Yes | Yes | Yes | Yes | 37.4MHz | 1.71-3.63V |
| RTL8189FTV MODULE | No | Yes | No | No | No | 40MHz On the module | 3.3V |
| RTL8723BS | No | Yes | No | No | Yes | | 1.71-3.63V |

| OPTION | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| AP6181 | Yes | Yes | No | Yes | |
| AP6212 | Yes | Yes | No | Yes | |
| AP6330 | Yes | Yes | No | Yes | |
| AP6335 | Yes | Yes | Yes | Yes | |
| RTL8189FTV MODULE | No | No | No | No | |
| RTL8723BS | No | No | No | Yes | |

| | |
|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics |
| Project: | RK3328_BOX_REF |
| File: | WIFI+BT_1T1R |
| Date: | Tuesday, March 07, 2017 |
| Rev: | V0.1 |
| Designed by: | Zhangdz |
| Sheet: | 27 of 29 |




# 2T2R

| OPTION | WIFI | | | | BT | Crystals | VDDIO |
|---|---|---|---|---|---|---|---|
| | a | b/g/n | ac | 5GHz | | | |
| AP6356S | Yes | Yes | Yes | Yes | Yes | 37.4MHz | 1.7-3.6V |
| QCA6174 | Yes | Yes | Yes | Yes | Yes | | 1.7-3.6V |
| RTL8822 | Yes | Yes | Yes | Yes | Yes | | 1.7-3.6V |
| RTL8192 | **No** | Yes | **No** | **No** | **No** | | 1.7-3.6V |

| OPTION | 1 | 2 | 3 | | |
|---|---|---|---|---|---|
| AP6356S | Paste | Paste | | | |
| QCA6174 | **DNP** | **DNP** | | | |
| RTL8822 | **DNP** | **DNP** | | | |
| RTL8192 | **DNP** | **DNP** | | | |

| | |
|---|---|
| Fuzhou Rockchip Electronics | |
| Project: | RK3328_BOX_REF |
| File: | WIFI+BT_2T2R |
| Date: | Tuesday, March 07, 2017 |
| Rev: | V1.0 |
| Designed by: | Zhangdz |
| Sheet: | 28 of 29 |