


# Schematics for RK3506G

## RK3506G\_REF

### Main Functions Introduction

- 1) POWER: DiscretePower or PMIC(RK801-1)
- 2) RAM: SIP (1 x DDR3L/DDR2 16bit)
- 3) ROM: 1 x SPI Nand/nor Flash  
1 x eMMC4.51(option)
- 4) Support: 1 x USB2.0 OTG0 + 1 x USB2.0 HOST
- 5) Support: 1 x 2Lanes MIPI DSI TX with Touch  
1 x RGB panel with Touch(option)
- 6) Support: 1 x DSMC Connector
- 7) Support: 1 x a/b/g/n/ac 1T1R SDIO WIFI + UART/PCM BT
- 8) Support: 2 x 10/100 Ethernet
- 9) Support: 1 x SPK + 2 x Analog MIC
- 10) Support: 1 x IR Receiver
- 11) Support: Array Key(MENU,VOL+,VOL-,ESC)
- 12) Support: 3 x SARADC + 1 x SARADC only for boot
- 13) Support: 1 x Debug UART/JTAG Connector
- 14) Support: 2 x CAN
- 15) Support: 2 x UART 485 +2 x UART

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Project:	RK3506G_REF		
File:	00.Cover Page		
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## Generate Bill of Materials

### Header:

Item\Part\Description\PCB Footprint\Reference\Quantity\Option

### Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

## Notes

### NOTE 1:


#### Component parameter description

1. NC stands for component not mounted temporarily
2. If Value or option is NC, which means the area is reserved without being mounted

### NOTE 2:

Please use our recommended components to avoid too many changes.  
For more informations about the second source,please refer to our AVL.

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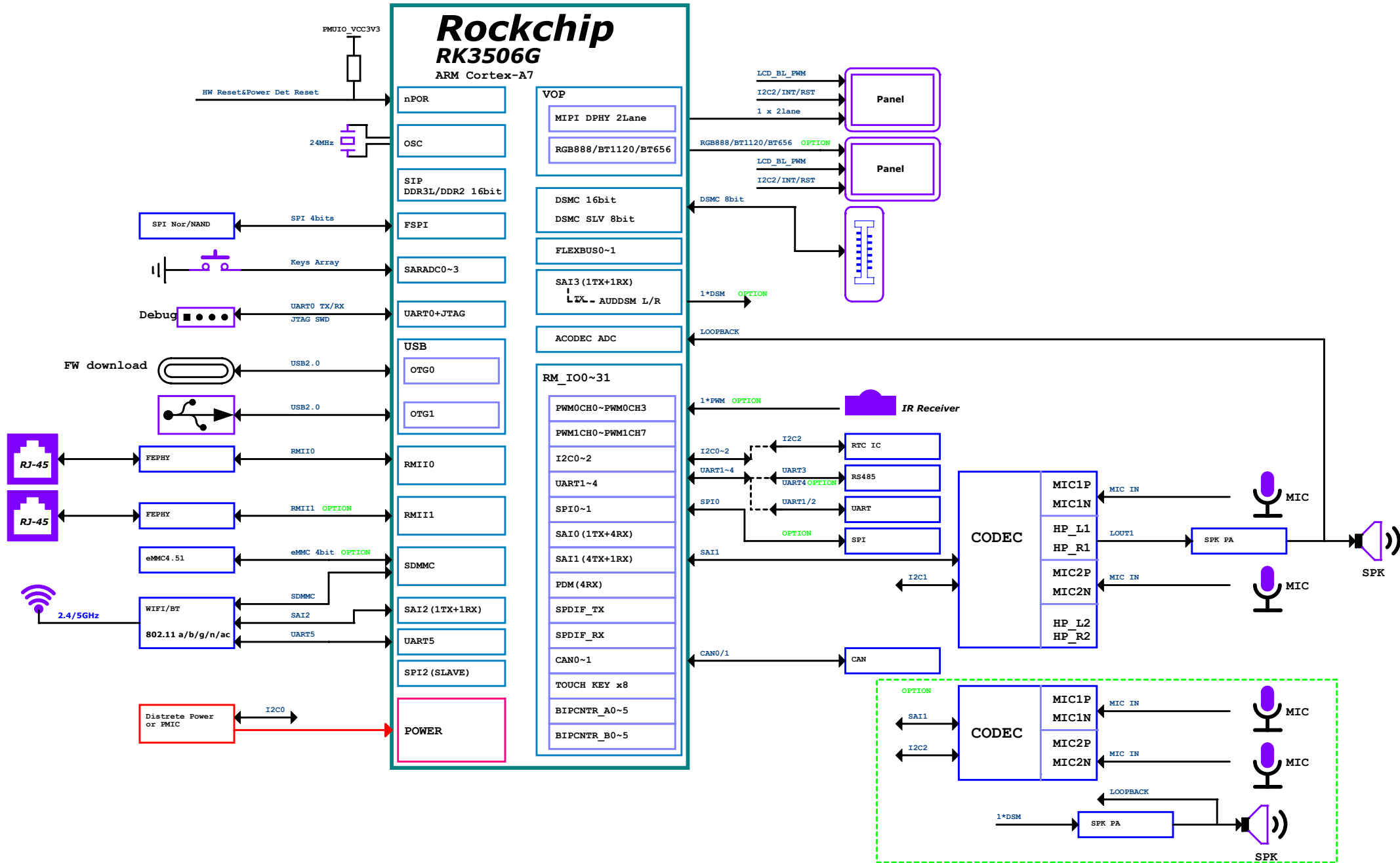
		Rockchip Electronics Co., Ltd	
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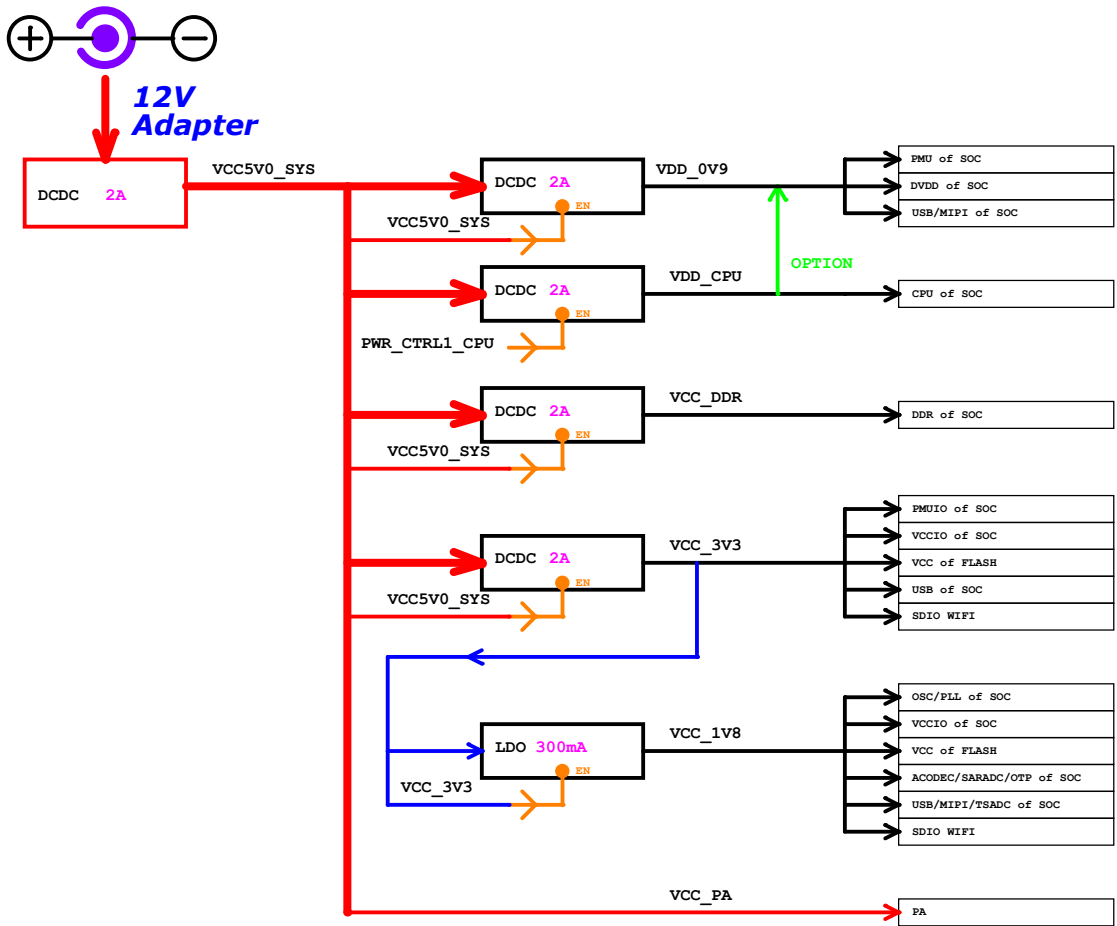
Version	Date	Author	Change Note	Approved
V1.0	2024.09.04	whb	First edition	
V1.1	2024.11.14	whb	1.Add PMIC power supply solution. 2.Circuit detail optimization.	



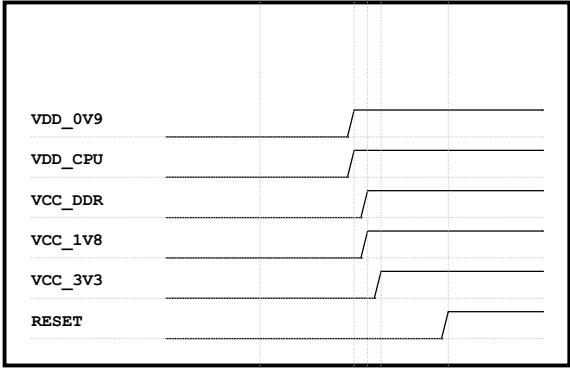




Power Diagram and Sequence



Power-on Sequence				
Power Name	PMIC Channel	Time Slot	Default voltage	Peak Current
VDD_0V9	DC-DC BUCK	Slot: 1	0.9V	
VDD_CPU	DC-DC BUCK	Slot: 1	0.95V	
VCC_DDR	DC-DC BUCK	Slot: 2	1.35V	
VCC_1V8	LDO	Slot: 2a	1.8V	
VCC_3V3	DC-DC BUCK	Slot: 3	3.3V	
RESET				
Finally, nPOR RESET 10ms after PMUIO VCC3V3 is ready				



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File: 04.Power Diagram-Disc

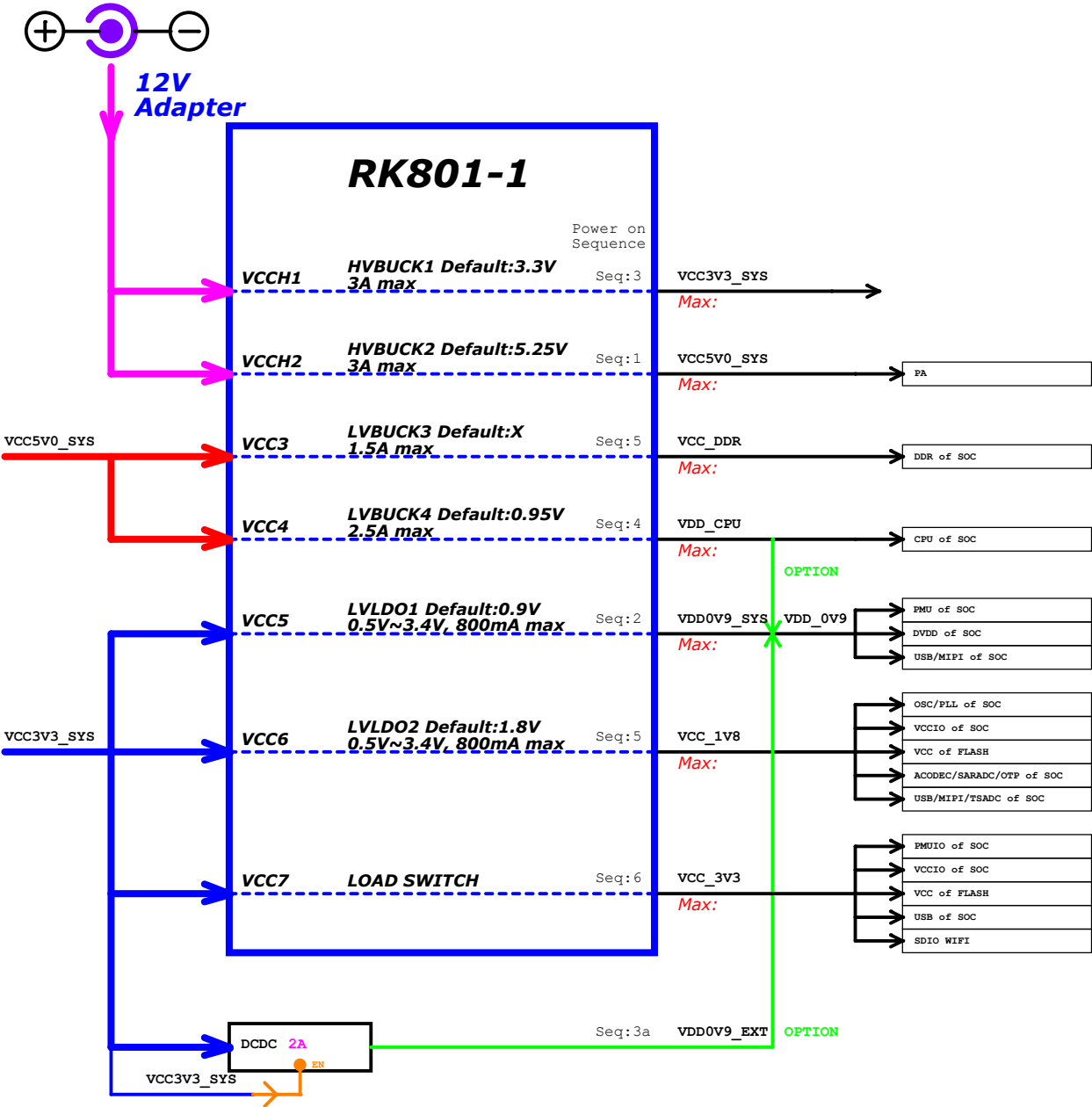
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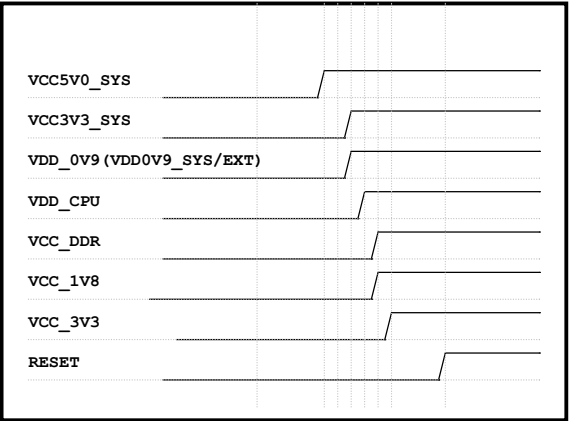


Power Diagram and Sequence

OPTION1:  
Normal power supply scheme.



Power-on Sequence				
Power Name	PMIC Channel	Time Slot	Default voltage	Peak Current
VCC5V0_SYS	RK801 HVBUCK2	Slot: 1	5.25V	
VCC3V3_SYS	RK801 HVBUCK1	Slot: 3	3.3V	
VDD0V9_SYS	RK801 LDO1	Slot: 3a	0.9V	
VDD_CPU	RK801 LVBUCK4	Slot: 4	0.95V	
VCC_DDR	RK801 LVBUCK3	Slot: 5	1.35V	
VCC_1V8	RK801 LDO2	Slot: 5	1.8V	
VCC_3V3	RK801 SWITCH	Slot: 6	3.3V	
VDD0V9_EXT	EXT BUCK	Slot: 3a	0.91V	
RESET				
Finally , nPOR RESET 10ms after PMUIO VCC3V3 is ready				



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File: 05.Power Diagram-PMIC

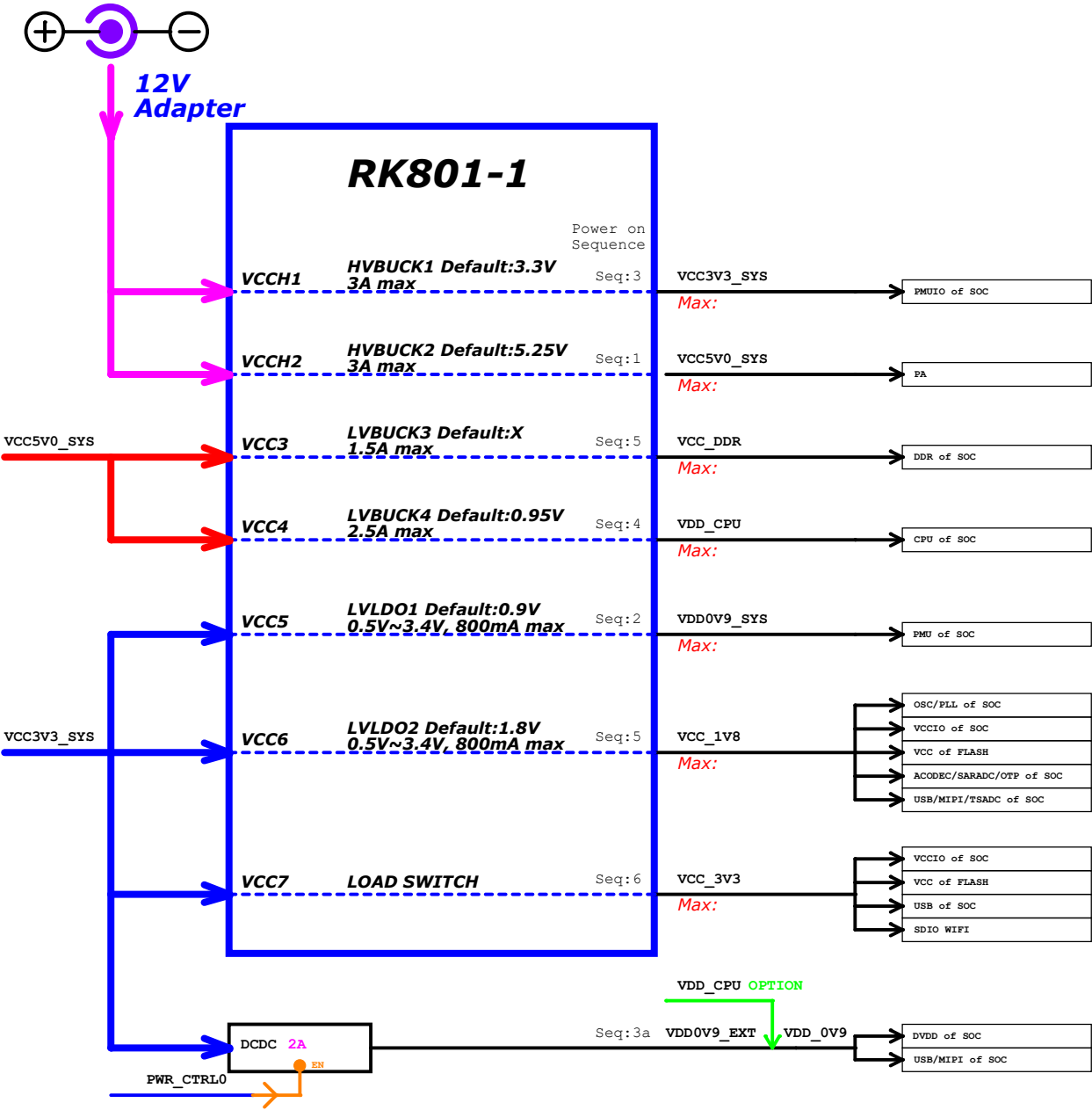
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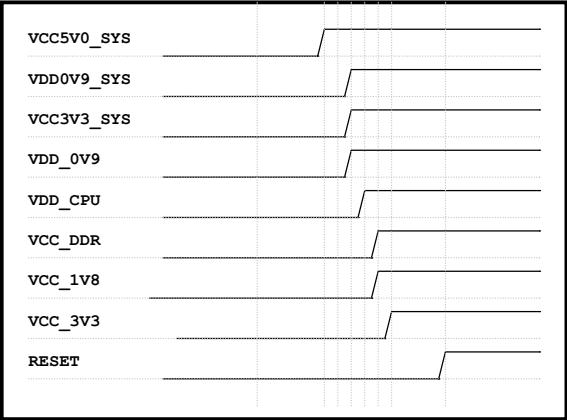


Power Diagram and Sequence

OPTION2:  
Standby scheme.



Power-on Sequence				
Power Name	PMIC Channel	Time Slot	Default voltage	Peak Current
VCC5V0_SYS	RK801 HVBUCK2	Slot: 1	5.25V	
VCC3V3_SYS	RK801 HVBUCK1	Slot: 3	3.3V	
VDD0V9_SYS	RK801 LDO1	Slot: 3a	0.9V	
VDD_CPU	RK801 LVBUCK4	Slot: 4	0.95V	
VCC_DDR	RK801 LVBUCK3	Slot: 5	1.35V	
VCC_1V8	RK801 LDO2	Slot: 5	1.8V	
VCC_3V3	RK801 SWITCH	Slot: 6	3.3V	
VDD_0V9	EXT BUCK	Slot: 3a	0.91V	
RESET				
Finally , nPOR RESET 10ms after PMU0 VCC3V3 is ready				



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File:	06.Power Diagram-PMIC sleep		
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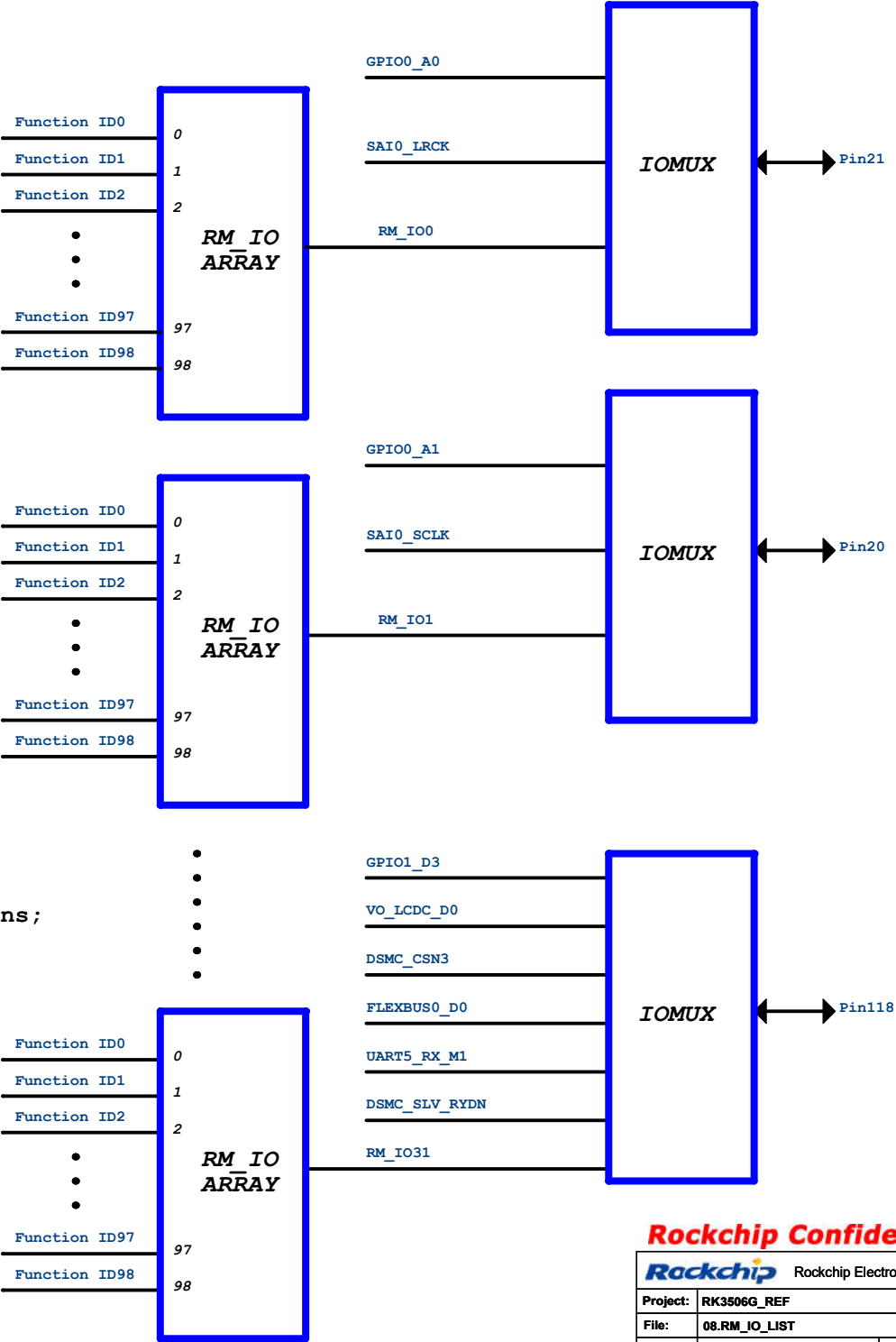
IO Power Domain Map

IO Domain	IO Group	Support of IO Voltage		Default Actual assigned IO Domain Voltage			Remark
		1.8V	3.3V	Net Name of Power Supply	Power Source	Voltage	
OSC/PLL	Group GPIO0_D	✓		VCC_1V8		1.8V	
PMUIO	Group GPIO0_ABC		✓	VCC_3V3		3.3V	
VCCIO1	Group GPIO1_ABCD	✓	✓	VCC_3V3		3.3V	
VCCIO2	Group GPIO2_A	✓	✓	VCCIO_FLASH		1.8/3.3V	
VCCIO3	Group GPIO2_BC	✓	✓	VCC_3V3		3.3V	
VCCIO4	Group GPIO3_AB	✓	✓	VCC_1V8		1.8V	



RM_IO List of optional function ID0~98							
ID	function	ID	function	ID	function	ID	function
0	NC	26	CAN1_TX	51	SAI0_MCLK	77	TSADC_CTRL
1	UART1_TX	27	CAN1_RX	52	SAI0_SCLK	78	PWR_CTRL0 (PMU_SLEEP)
2	UART1_RX	28	CAN0_TX	53	SAI0_LRCK	79	PWR_CTRL1 (CORE_POWER_OFF)
3	UART2_TX	29	CAN0_RX	54	SAI0_SDI0	80	SPDIF_TX
4	UART2_RX	30	PWM0_CH0	55	SAI0_SDI1	81	SPDIF_RX
5	UART3_TX	31	PWM0_CH1	56	SAI0_SDI2	82	BIPCNTR_A0
6	UART3_RX	32	PWM0_CH2	57	SAI0_SDI3	83	BIPCNTR_A1
7	UART3_CTSN	33	PWM0_CH3	58	SAI0_SDO	84	BIPCNTR_A2
8	UART3_RTSN	34	PWM1_CH0	59	SAI1_MCLK	85	BIPCNTR_A3
9	UART4_TX	35	PWM1_CH1	60	SAI1_SCLK	86	BIPCNTR_A4
10	UART4_RX	36	PWM1_CH2	61	SAI1_LRCK	87	BIPCNTR_A5
11	UART4_CTSN	37	PWM1_CH3	62	SAI1_SDI	88	BIPCNTR_B0
12	UART4_RTSN	38	PWM1_CH4	63	SAI1_SDO0	89	BIPCNTR_B1
13	MIPI_DPHY_DSI_TX_TE	39	PWM1_CH5	64	SAI1_SDO1	90	BIPCNTR_B2
14	CLK_32K	40	PWM1_CH6	65	SAI1_SDO2	91	BIPCNTR_B3
15	I2C0_SCL	41	PWM1_CH7	66	SAI1_SDO3	92	BIPCNTR_B4
16	I2C0_SDA	42	TOUCH_KEYDRIVE	67	SPI0_CLK	93	BIPCNTR_B5
17	I2C1_SCL	43	TOUCH_KEY_IN0	68	SPI0_MOSI	94	PDM_CLK1
18	I2C1_SDA	44	TOUCH_KEY_IN1	69	SPI0_MISO	95	ETH_RMII0_PPSCCLK
19	I2C2_SCL	45	TOUCH_KEY_IN2	70	SPI0_CSN0	96	ETH_RMII0_PPSTRIG
20	I2C2_SDA	46	TOUCH_KEY_IN3	71	SPI0_CSN1	97	ETH_RMII1_PPSCCLK
21	PDM_CLK0	47	TOUCH_KEY_IN4	72	SPI1_CLK	98	ETH_RMII1_PPSTRIG
22	PDM_SDI0	48	TOUCH_KEY_IN5	73	SPI1_MOSI		
23	PDM_SDI1	49	TOUCH_KEY_IN6	74	SPI1_MISO		
24	PDM_SDI2	50	TOUCH_KEY_IN7	75	SPI1_CSN0		
25	PDM_SDI3			76	SPI1_CSN1		

NOTE:  
(1)RM\_IOX(X=0~31) can select functions from function ID0~ID98;  
(2)RM\_IOX(X=0~31) cannot repeatedly select the function ID0~ID98;  
(3)SAI、PDM、SPI signals should not cross the PMUIO and VCCIO domains;  
(4)The signal of the same function in RM\_IO is used across PMUIO and VCCIO domains, and the operating level needs to be consistent



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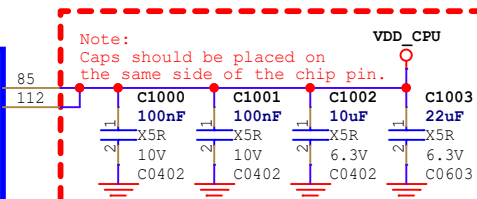
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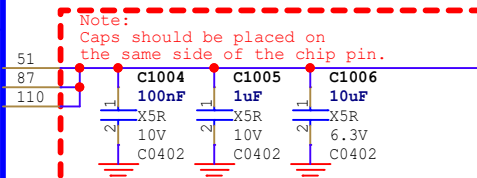
U1000G

CPU

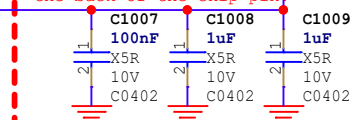
CPU\_DVDD\_0  
CPU\_DVDD\_1

Note:  
10u+100n:close to pin112;  
22u+100n:close to pin85;

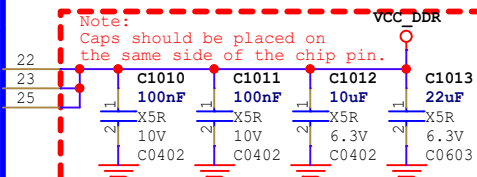
LOGIC

LOGIC\_DVDD\_0  
LOGIC\_DVDD\_1  
LOGIC\_DVDD\_2

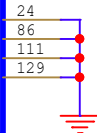
Note:  
Caps should be placed on the back of the chip pin.



DDR\_VDDQ

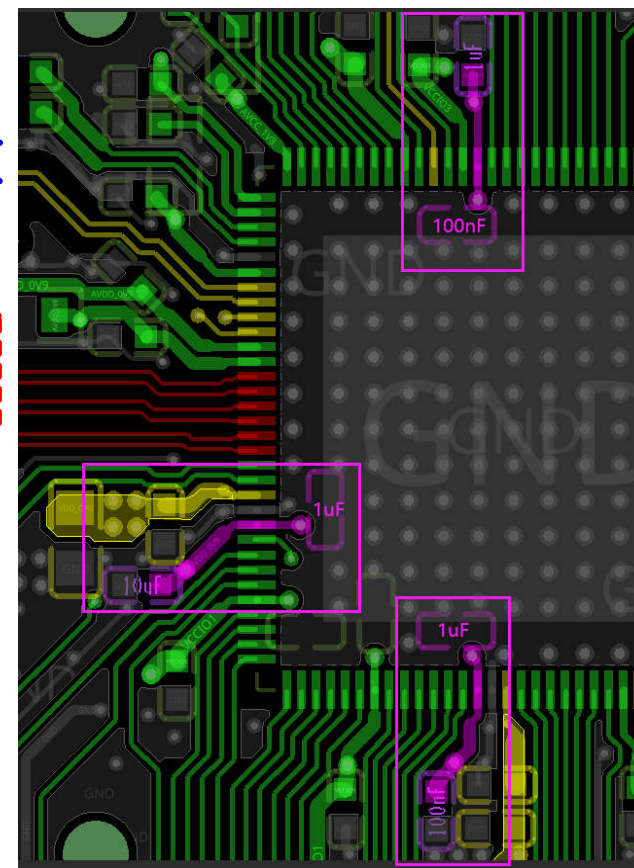
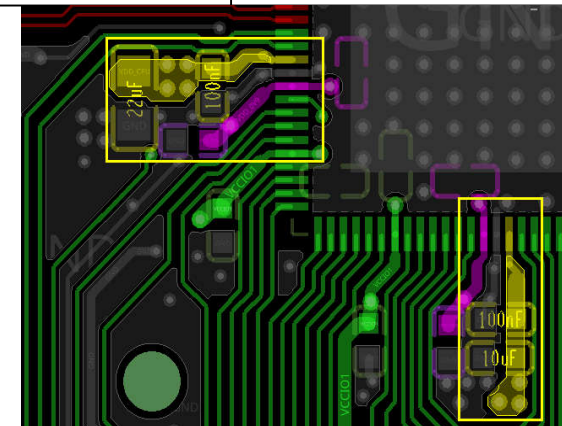
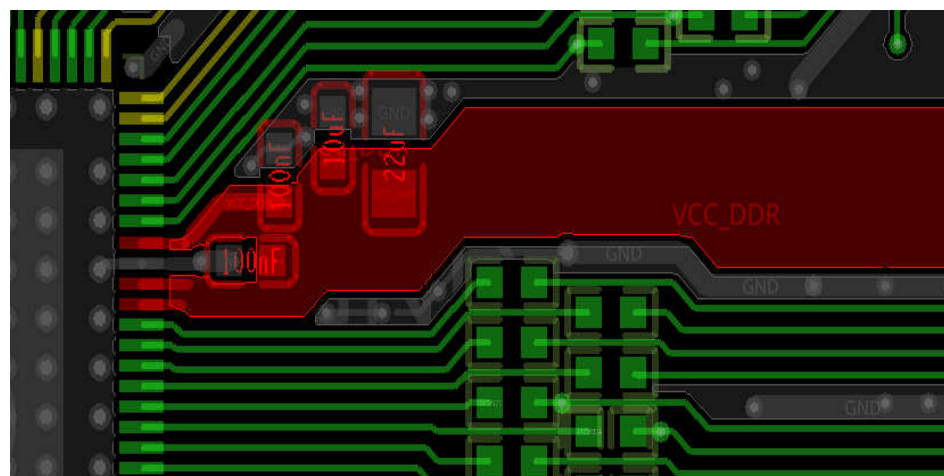
DDR\_VDDQ\_0  
DDR\_VDDQ\_1  
DDR\_VDDQ\_2

VSS

VSS\_0  
VSS\_1  
VSS\_2  
EPAD

RK3506G

QFN128\_12r3x12r3x0r90\_t9r10

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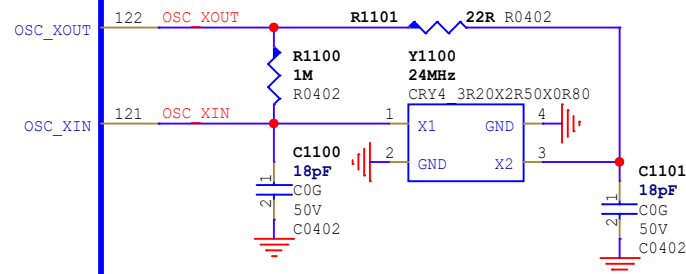
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Project:	RK3506G_REF		
File:	10.SOC-POWER/GND		
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U1000A

## OSC/PLL

Operating Voltage=1.8V Only



## PMUIO Domain

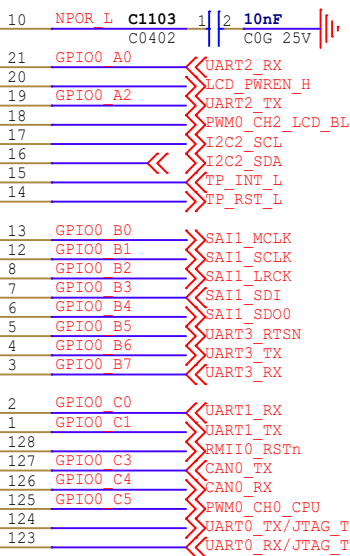
Operating Voltage=3.3V Only

RM_IO0	--	SAI0_LRCK	GPIO0_A0_u
RM_IO1	--	SAI0_SCLK	GPIO0_A1_d
RM_IO2	--	SAI0_MCLK	GPIO0_A2_u
RM_IO3	--	SAI0_SDO	GPIO0_A3_d
RM_IO4	--	SAI0_SDI0	GPIO0_A4_d
RM_IO5	--	SAI0_SDI1	GPIO0_A5_d
RM_IO6	--	SAI0_SDI2	GPIO0_A6_d
RM_IO7	SPI1_CSN1	SAI0_SDI3	GPIO0_A7_d
RM_IO8	SPI1_CLK	SAI1_MCLK	GPIO0_B0_d
RM_IO9	SPI1_MOSI	SAI1_SCLK	GPIO0_B1_d
RM_IO10	SPI1_MISO	SAI1_LRCK	GPIO0_B2_d
RM_IO11	--	SAI1_SDI	GPIO0_B3_d
RM_IO12	--	SAI1_SDO0	GPIO0_B4_d
RM_IO13	--	SAI1_SDO1	GPIO0_B5_d
RM_IO14	SPI1_CSN0	SAI1_SDO2	GPIO0_B6_d
RM_IO15	SPI0_CSN1	SAI1_SDO3	GPIO0_B7_d
RM_IO16	SPI0_CLK	--	GPIO0_C0_d
RM_IO17	SPI0_MOSI	--	GPIO0_C1_d
RM_IO18	SPI0_MISO	REF_CLK1_OUT	GPIO0_C2_d
RM_IO19	SPI0_CSN0	ETH_CLK1_25M_OUT	GPIO0_C3_d
RM_IO20	AUPLL_CLK_IN	ETH_CLK0_25M_OUT	GPIO0_C4_d
RM_IO21	--	CPU_AVS	GPIO0_C5_z
RM_IO22	JTAG_TCK_M1	UART0_TX	GPIO0_C6_u
RM_IO23	JTAG_TMS_M1	UART0_RX	GPIO0_C7_u

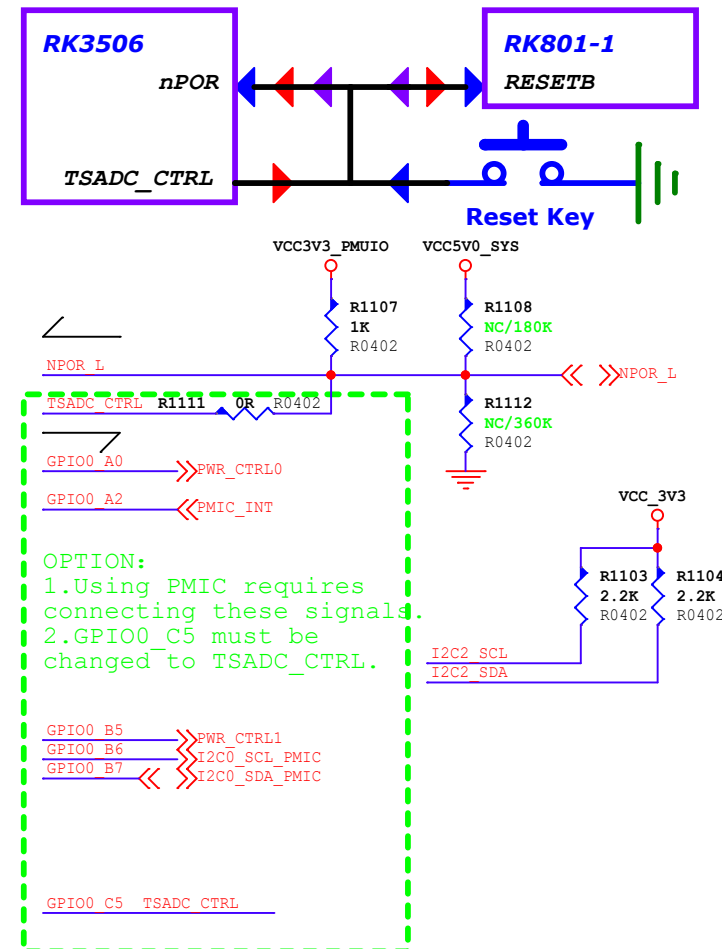
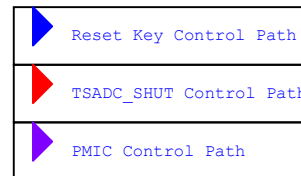
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PMUIO\_VCC3V3

RK3506G


QFN128\_12r3x12r3x0r90\_t9r10



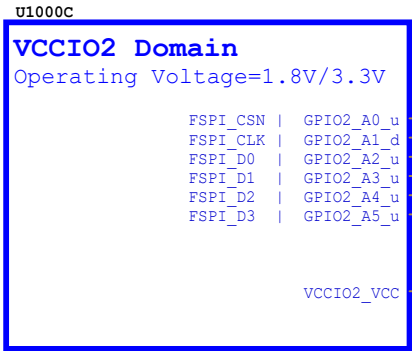
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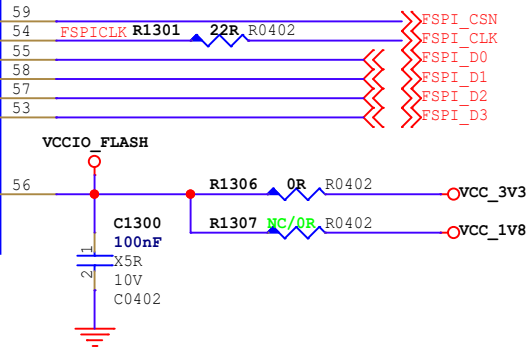
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RK3506G

QFN128\_12r3x12r3x0r90\_t9r10



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U1000P

## MIPI

Operating Voltage=1.8V  
GPO is output only

MIPI_DPHY_DSI_TX_D0N	GPO4_A0_z
MIPI_DPHY_DSI_TX_D0P	GPO4_A1_z
MIPI_DPHY_DSI_TX_D1N	GPO4_A2_z
MIPI_DPHY_DSI_TX_D1P	GPO4_A3_z
MIPI_DPHY_DSI_TX_CLKN	GPO4_A4_z
MIPI_DPHY_DSI_TX_CLKP	GPO4_A5_z

## USB2.0 OTG0

HS/FS/LS  
(Download Port)

USB20_OTG0_DP	72
USB20_OTG0_DM	71

## USB2.0 OTG1

HS/FS/LS

USB20_OTG1_DP	74
USB20_OTG1_DM	73

## SARADC

Operating Voltage=1.8V

SARADC_IN0	GPI04_B0_z
SARADC_IN1	GPI04_B1_z
SARADC_IN2	GPI04_B2_z
SARADC_IN3	GPI04_B3_z

## ACODEC

ACODEC\_ADC\_INP

ACODEC\_ADC\_INN

ACODEC\_ADC\_AVDD1V6

ACODEC\_ADC\_VCM

ACODEC\_ADC\_AVSS

## Power

These power must be powered

USB20_OTG	AVDD_0V9
MIPI_DPHY	

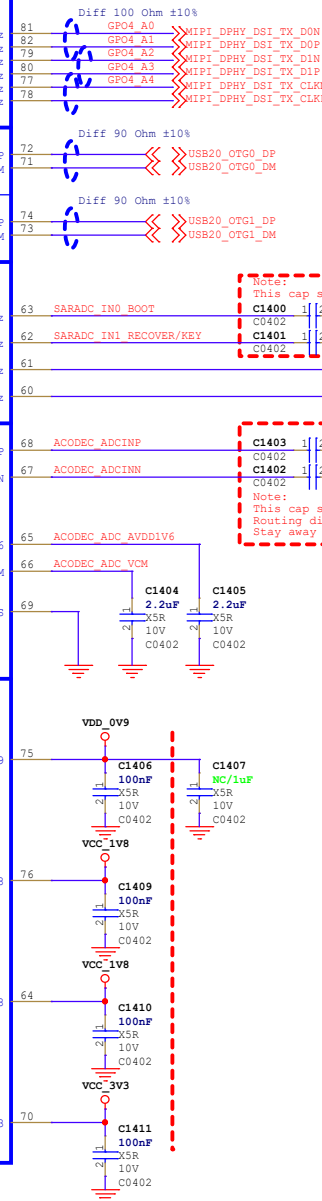
USB20_OTG	AVDD_1V8
MIPI_DPHY	
TSADC	

ACODEC_ADC	AVCC_1V8
SARADC	
OTP	

USB20\_OTG\_AVDD3V3

RK3506G

QFN128\_12x3x12x3x0r90\_t9r10



## OPTION

NOTE:  
If you use an mipi screen, can put these functions into the VCCIOL.

GPO4_A0	»»USB20_OTG0_DRV_H
GPO4_A1	»»MIPI_REG_ON_H
GPO4_A2	»»SPK_CTRL
GPO4_A3	»»SMI11_RSTn
GPO4_A4	»»USB20_OTG1_DRV_H
GPO4_A5	»»MIPI_DPHY_DSI_TX_CLKN

Note:  
This cap should be placed close to SOC.

C1400	1	2	1nF	»»
C0402			COG 50V	
C1401	1	2	1nF	»»
C0402			COG 50V	

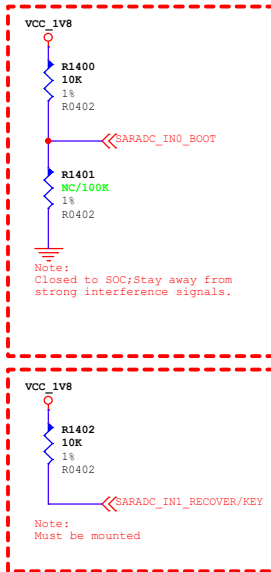
»»HOST\_WAKE\_BT\_H

»»BT\_WAKE\_HOST\_H

Note:  
This cap should be placed close to SOC;  
Routing difference,package GND processing;  
Stay away from strong interference signals;

C1403	1	2	1uF	»»ACODEC_ADC_INP
C0402			X5R 10V	
C1402	1	2	1uF	»»ACODEC_ADC_INN
C0402			X5R 10V	

C1404	2.2uF	C1405	2.2uF
X5R		X5R	
10V		10V	
C0402		C0402	



## SARADC IN0 BOOT TABLE

Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	10K	0	USB (Maskrom mode)/SPI2APB
LEVEL2	100K	12K	110	SPI2APB
LEVEL3	100K	27K	217	FSPI--USB/SPI2APB
LEVEL4	100K	51K	345	
LEVEL5	100K	82K	461	
LEVEL6	10K	12K	558	SDMMC(eMMC/SD Card)--USB/SPI2APB
LEVEL7	10K	20K	682	
LEVEL8	10K	33K	785	
LEVEL9	10K	82K	912	
LEVEL10	10K	DNP	1023	FSPI--SDMMC(eMMC/SD Card)--USB/SPI2APB

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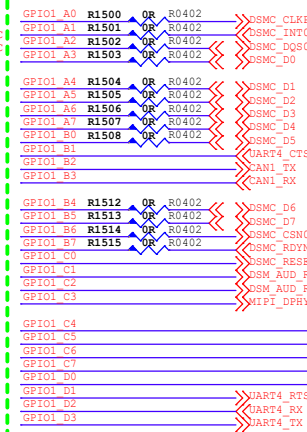
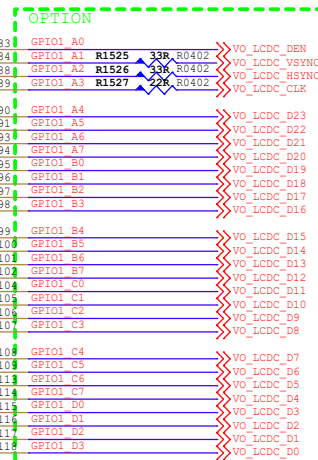
Project:	RK3506G_REF		
File:	14.SOC-USB/ACODEC/SARADC/MIPI		
Date:	Friday, November 15, 2024	Rev:	V1.1
Designed by:	whb	Reviewed by:	Default



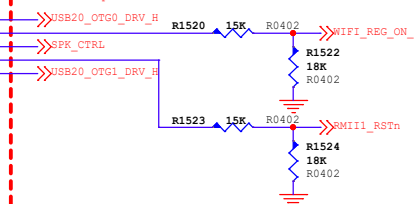
## VCCIO1 Domain

Operating Voltage=1.8V/3.3V

DSMC_SLV_INT	--	--	--	--	--	FLEXBUS1_D0	DSMC_CLKP	VO_LCDC_DEN	GPIO1_A0_d
--	--	--	--	--	--	FLEXBUS1_D1	DSMC_CLKN	VO_LCDC_VSYNC	GPIO1_A1_d
--	--	--	--	--	--	FLEXBUS1_D2	DSMC_DQ80	VO_LCDC_HSYNC	GPIO1_A2_d
--	--	--	--	--	--	FLEXBUS1_D3	DSMC_D0	VO_LCDC_CLK	GPIO1_A3_d
--	--	--	--	--	--	FLEXBUS1_D4	DSMC_D1	VO_LCDC_D23	GPIO1_A4_d
--	--	--	--	--	--	FLEXBUS1_D5	DSMC_D2	VO_LCDC_D22	GPIO1_A5_d
--	--	--	--	--	--	FLEXBUS1_D6	DSMC_D3	VO_LCDC_D21	GPIO1_A6_d
--	--	--	--	--	--	FLEXBUS1_D7	DSMC_D4	VO_LCDC_D20	GPIO1_A7_d
--	--	--	--	--	--	FLEXBUS1_D8	DSMC_D5	VO_LCDC_D19	GPIO1_B0_d
--	RM_I024	UART5_CTSN_M1	FLEXBUS0_CSN_M0	--	--	FLEXBUS1_D9	DSMC_CSN1	VO_LCDC_D18	GPIO1_B1_d
--	RM_I025	SAI2_SCLK_M1	FLEXBUS0_CSN_M1	FLEXBUS0_D15	FLEXBUS1_D10	DSMC_INT2	VO_LCDC_D17	VO_LCDC_D17	GPIO1_B2_d
--	RM_I026	SAI2_LCKK_M1	FLEXBUS1_CSN_M1	FLEXBUS0_D14	FLEXBUS1_D11	DSMC_INT3	VO_LCDC_D16	VO_LCDC_D16	GPIO1_B3_d
--	--	--	--	--	--	--	--	--	--
--	--	--	--	--	--	FLEXBUS0_CSN_M2	FLEXBUS0_D13	FLEXBUS1_D12	DSMC_D6
--	--	--	--	--	--	FLEXBUS1_CSN_M2	FLEXBUS0_D12	DSMC_D7	VO_LCDC_D15
--	--	--	--	--	--	FLEXBUS0_CSN_M3	FLEXBUS0_D11	FLEXBUS1_D14	DSMC_CSN0
--	--	--	--	--	--	FLEXBUS1_CSN_M3	FLEXBUS0_D10	FLEXBUS1_D15	DSMC_RDYN
DSMC_SLV_CLK	--	--	--	--	--	DSMC_INT1	FLEXBUS1_CLK	DSMC_RESETN	VO_LCDC_D11
DSMC_SLV_DQ80	--	SAI2_MCLK_M1	FLEXBUS1_CSN_M4	DSMC_INT1	FLEXBUS0_CLK	DSMC_D8	VO_LCDC_D10	GPIO1_C1_d	GPIO1_C1_d
DSMC_SLV_D0	RM_I027	SAI2_SDI_M1	FLEXBUS1_CSN_M4	DSM_AUD_RN_M0	FLEXBUS0_D9	DSMC_D9	VO_LCDC_D9	GPIO1_C2_d	GPIO1_C2_d
DSMC_SLV_D1	RM_I028	SAI2_SDO_M1	FLEXBUS1_CSN_M5	--	FLEXBUS0_D8	DSMC_D10	VO_LCDC_D8	GPIO1_C3_d	GPIO1_C3_d
--	--	--	--	--	--	--	--	--	--
DSMC_SLV_D2	--	--	--	--	--	FLEXBUS0_D7	DSMC_D11	VO_LCDC_D7	GPIO1_C4_d
DSMC_SLV_D3	--	--	--	--	--	FLEXBUS0_D6	DSMC_D12	VO_LCDC_D6	GPIO1_C5_d
DSMC_SLV_D4	--	--	--	--	--	DSMC_D13	DSMC_D13	VO_LCDC_D5	GPIO1_C6_d
DSMC_SLV_D5	--	--	--	--	--	FLEXBUS0_D4	DSMC_D14	VO_LCDC_D4	GPIO1_C7_d
DSMC_SLV_D6	--	--	--	--	--	FLEXBUS0_D3	DSMC_D15	VO_LCDC_D3	GPIO1_D0_d
DSMC_SLV_D7	RM_I029	UART5_RTSN_M1	--	--	--	FLEXBUS0_D2	DSMC_DQ81	VO_LCDC_D2	GPIO1_D1_d
DSMC_SLV_CSN0	RM_I030	UART5_TX_M1	--	--	--	FLEXBUS0_D1	DSMC_CSN2	VO_LCDC_D1	GPIO1_D2_d
DSMC_SLV_RDYN	RM_I031	UART5_RX_M1	--	--	--	FLEXBUS0_D0	DSMC_CSN3	VO_LCDC_D0	GPIO1_D3_d

VCCIO1\_VCC\_0  
VCCIO1\_VCC\_1

NOTE:  
If you use an RGB screen, can put these functions  
into the mipi interface.



RK3506G

QFN128\_12r3x12r3x0r90\_t9r10

Mode	RGB					BT1120		BT656		MCU			
	24bit	18bit	16bit	8bit	6bit	16bit	8bit	24bit	18bit	16bit	8bit	6bit	
LCDC_DEN	DEN	DEN	DEN	DEN	DEN	--	--	RDN	RDN	RDN	RDN	RDN	
LCDC_VSYNC	VSYN	VSYN	VSYN	VSYN	VSYN	--	--	CSN	CSN	CSN	CSN	CSN	
LCDC_HSYNC	HSYN	HSYN	HSYN	HSYN	HSYN	--	--	WRN	WRN	WRN	WRN	WRN	
LCDC_CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	RS	RS	RS	RS	RS	
LCDC_D23	D23	D17	D15	D7_m1	D5_m1	D15	D7_m1	D23	D17	D15	D7_m1	D5_m1	
LCDC_D22	D22	D16	D14	D6_m1	D4_m1	D14	D6_m1	D22	D16	D14	D6_m1	D4_m1	
LCDC_D21	D21	D15	D13	D5_m1	D3_m1	D13	D5_m1	D21	D15	D13	D5_m1	D3_m1	
LCDC_D20	D20	D14	D12	D4_m1	D2_m1	D12	D4_m1	D20	D14	D12	D4_m1	D2_m1	
LCDC_D19	D19	D13	D11	D3_m1	D1_m1	D11	D3_m1	D19	D13	D11	D3_m1	D1_m1	
LCDC_D18	D18	D12	--	--	--	--	--	D18	D12	--	--	--	
LCDC_D17	D17	--	--	--	--	--	--	D17	--	--	--	--	
LCDC_D16	D16	--	--	--	--	--	--	D16	--	--	--	--	
LCDC_D15	D15	D11	D10	D2_m1	D0_m1	D10	D2_m1	D15	D11	D10	D2_m1	D0_m1	
LCDC_D14	D14	D10	D9	D1_m1	--	D9	D1_m1	D14	D10	D9	D1_m1	--	
LCDC_D13	D13	D9	D8	D0_m1	--	D8	D0_m1	D13	D9	D8	D0_m1	--	
LCDC_D12	D12	D8	D7	D7_m0	D5_m0	D7	D7_m0	D12	D8	D7	D7_m0	D5_m0	
LCDC_D11	D11	D7	D6	D6_m0	D4_m0	D6	D6_m0	D11	D7	D6	D6_m0	D4_m0	
LCDC_D10	D10	D6	D5	D5_m0	D3_m0	D5	D5_m0	D10	D6	D5	D5_m0	D3_m0	
LCDC_D9	D9	--	--	--	--	--	--	D9	--	--	--	--	
LCDC_D8	D8	--	--	--	--	--	--	D8	--	--	--	--	
LCDC_D7	D7	D5	D4	D4_m0	D2_m0	D4	D4_m0	D7	D5	D4	D4_m0	D2_m0	
LCDC_D6	D6	D4	D3	D3_m0	D1_m0	D3	D3_m0	D6	D4	D3	D3_m0	D1_m0	
LCDC_D5	D5	D3	D2	D2_m0	D0_m0	D2	D2_m0	D5	D3	D2	D2_m0	D0_m0	
LCDC_D4	D4	D2	D1	D1_m0	--	D1	D1_m0	D4	D2	D1	D1_m0	--	
LCDC_D3	D3	D1	D0	D0_m0	--	D0	D0_m0	D3	D1	D0	D0_m0	--	
LCDC_D2	D2	D0	--	--	--	--	--	D2	D0	--	--	--	
LCDC_D1	D1	--	--	--	--	--	--	D1	--	--	--	--	
LCDC_D0	D0	--	--	--	--	--	--	D0	--	--	--	--	

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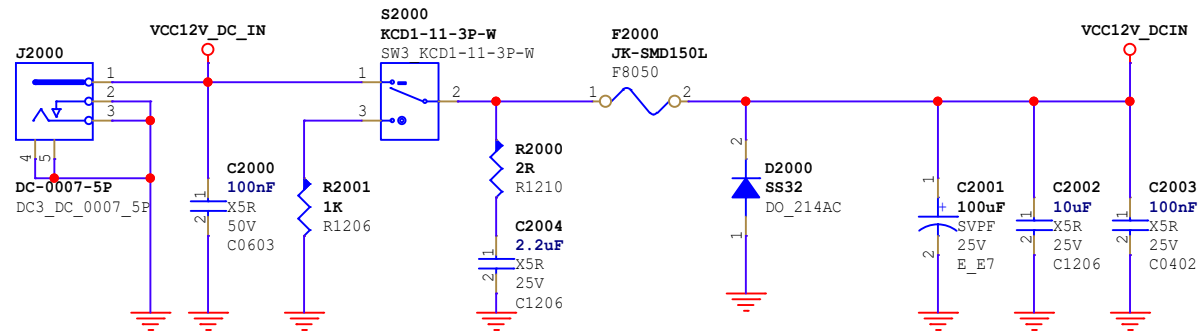
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File:	15.SOC-VO Interface/GPIO		
Date:	Friday, November 15, 2024	Rev:	V1.1
Designed by:	whb	Reviewed by:	Default
Sheet:	14	of	40



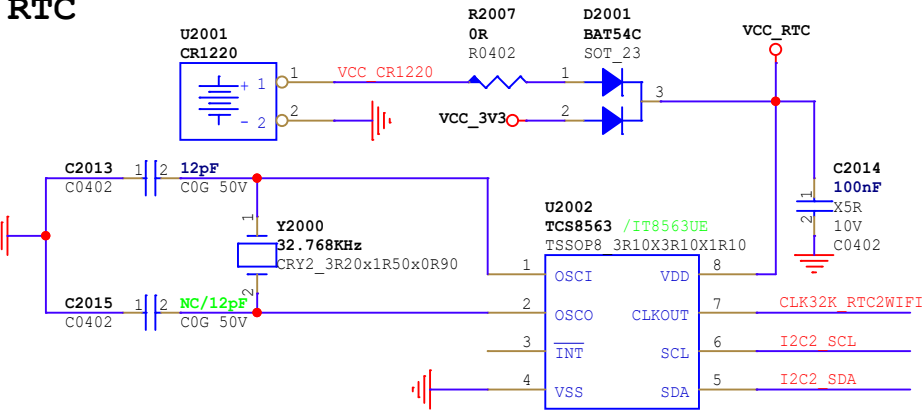
Sheet:	15 of 40
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12V/1A DCIN



RTC



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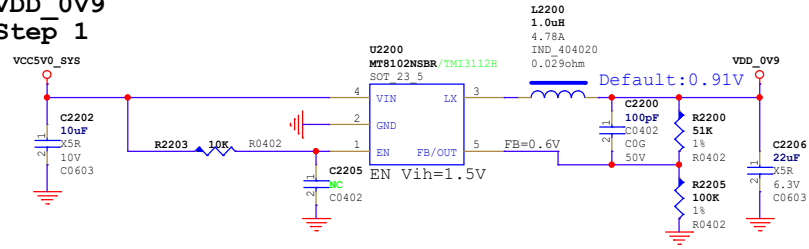


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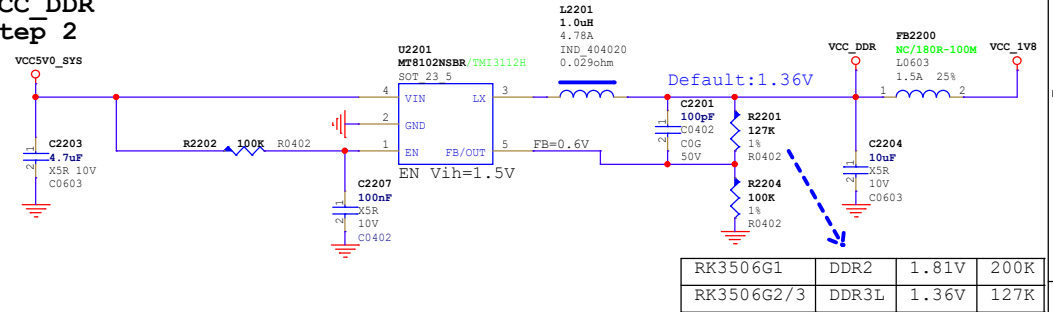
Project:	RK3506G_REF		
File:	20.Power-DC IN		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by: Default	Sheet: 16 of 40



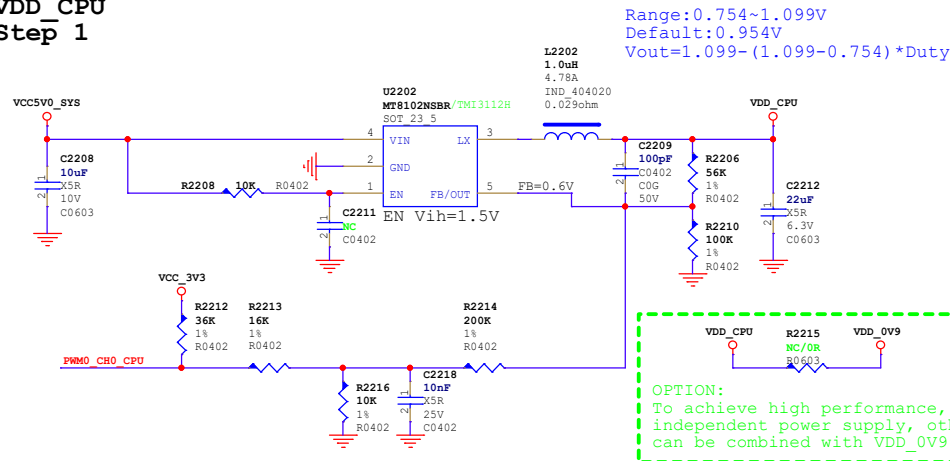
## VDD\_0V9 Step 1



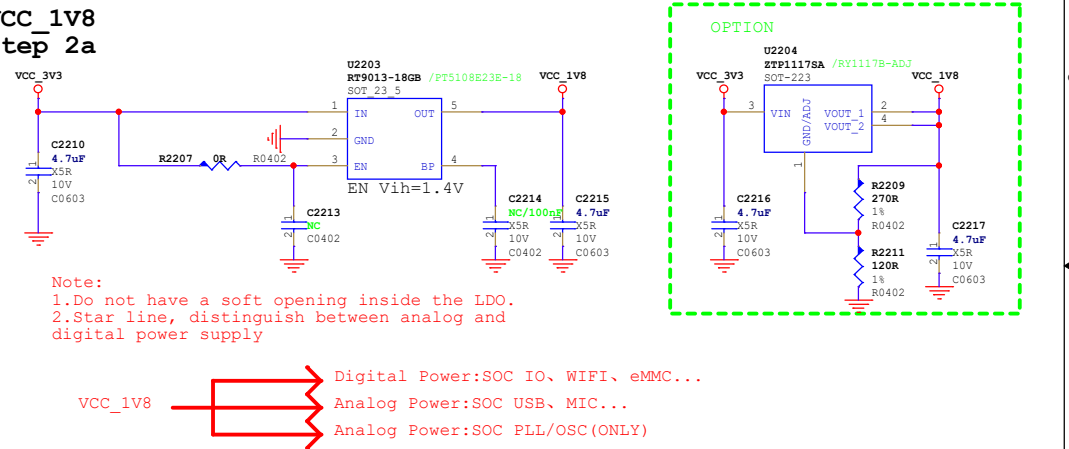
## VCC\_DDR Step 2



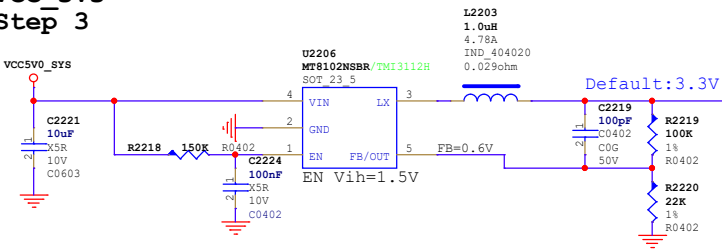
## VDD\_CPU Step 1



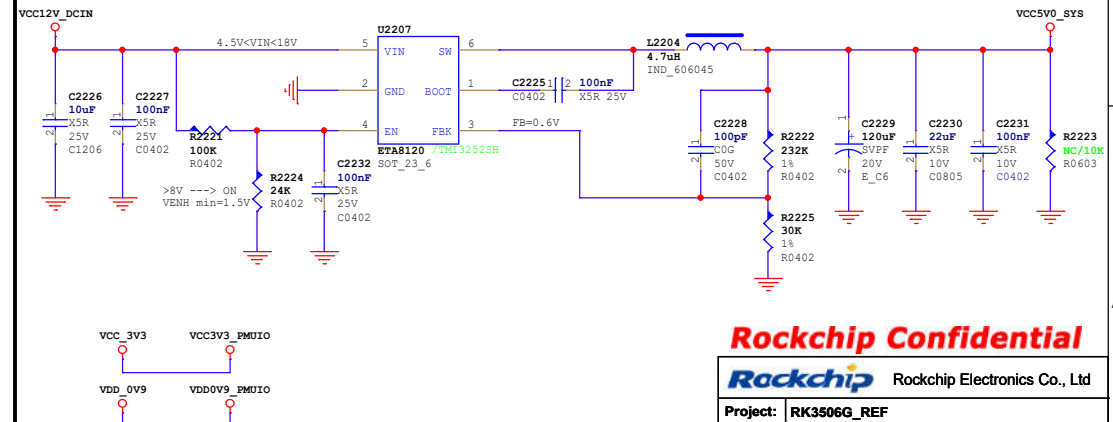
## VCC\_1V8 Step 2a



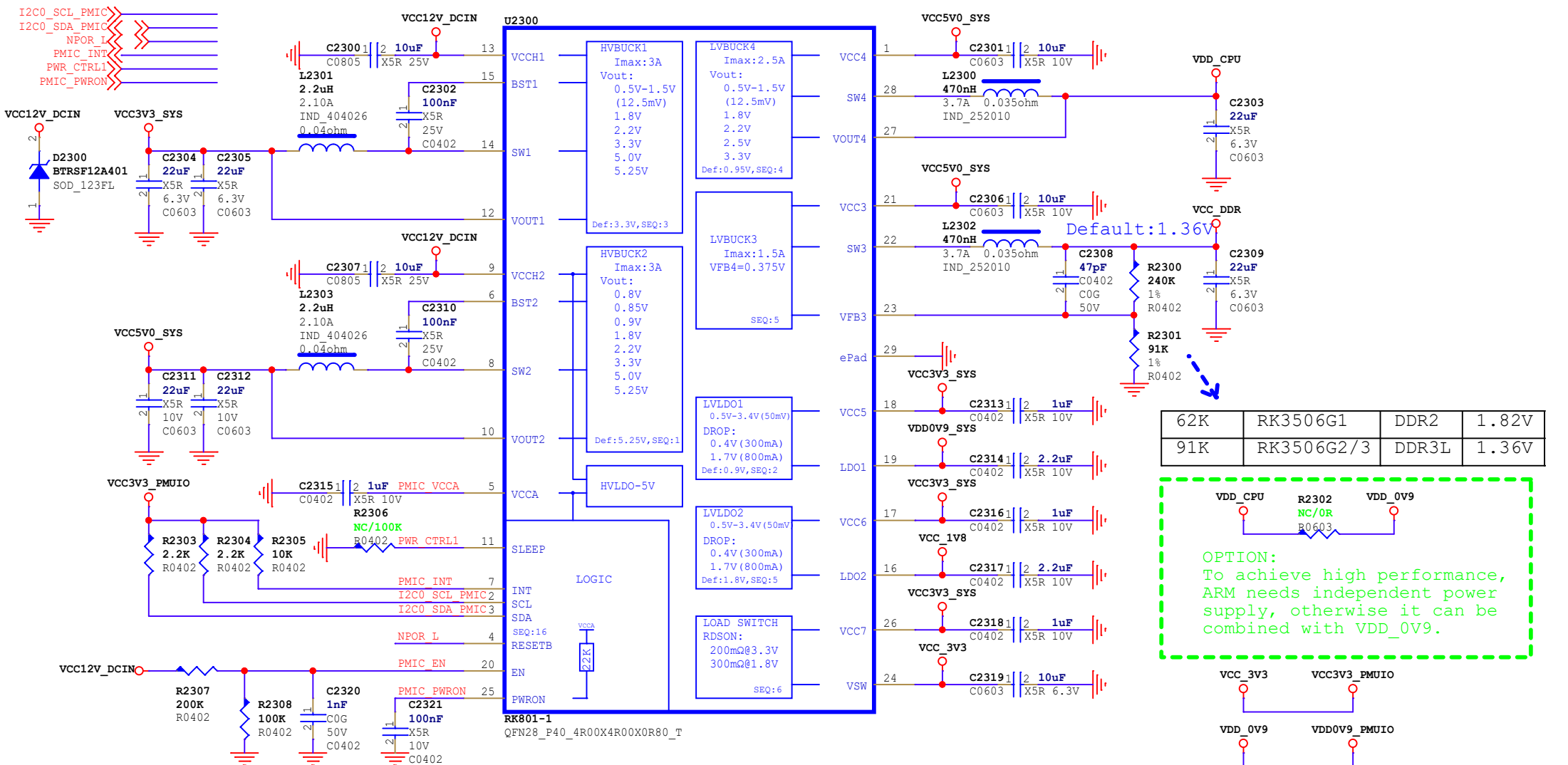
## VCC\_3V3 Step 3



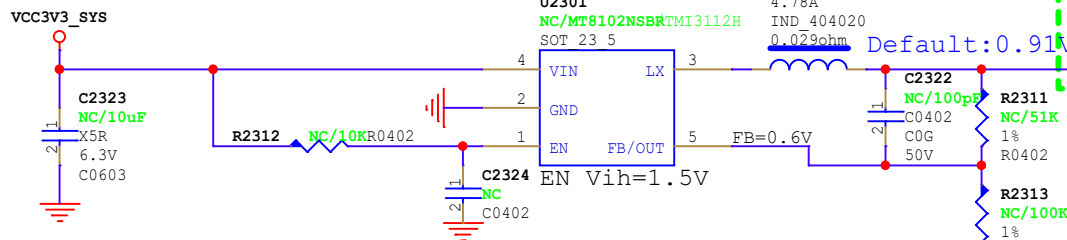
## VCC5V0\_SYS








VDD0V9\_EXT  
Step 3a

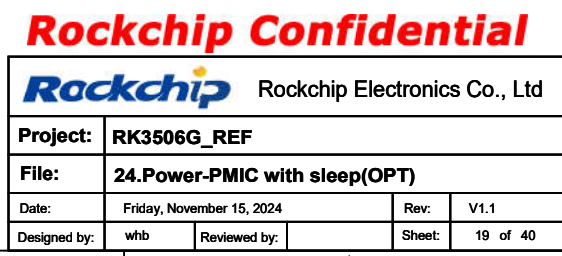


OPTION:either  
If power consumption is not concerned,  
you can consider using PMIC to supply  
power to VDD\_0V9, and the temperature  
rise of PMIC is increased by about 7°C.

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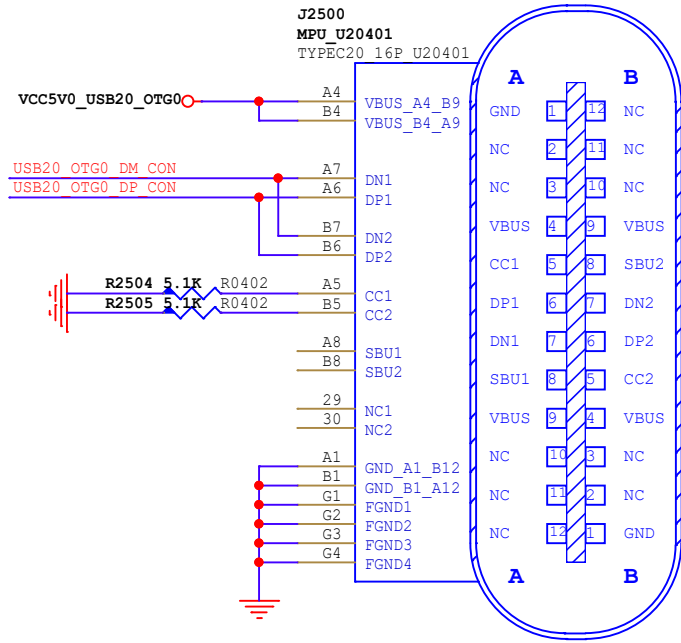
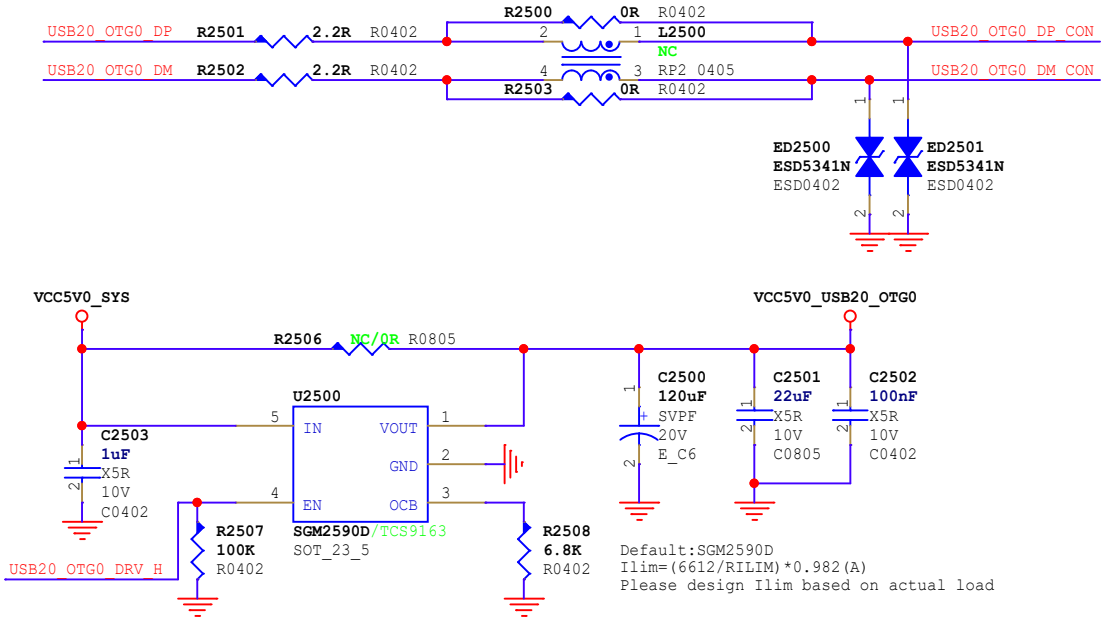
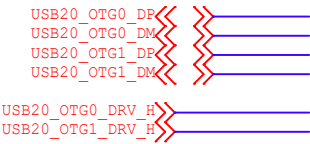
		Rockchip Electronics Co., Ltd	
Project:	RK3506G_REF		
File:	23.Power-PMIC(OPT)		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by:	Sheet: 18 of 40



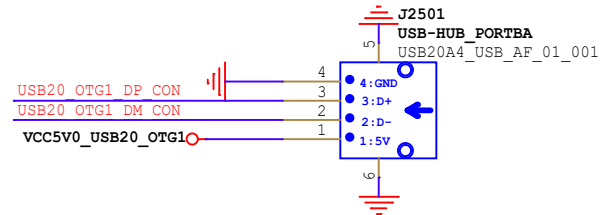
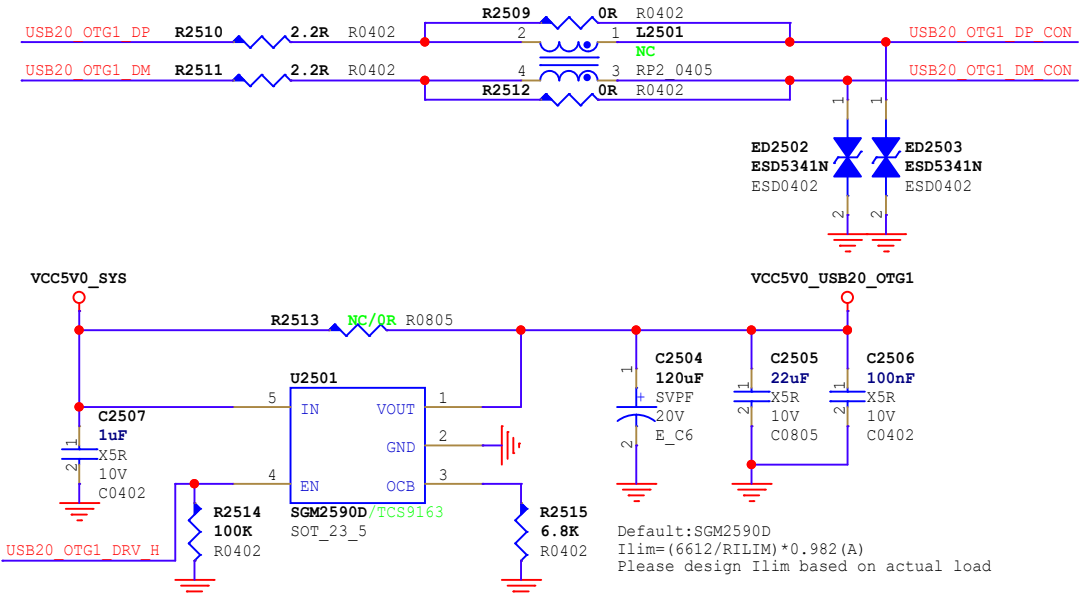





# USB2.0 OTG0(Download Port)



# USB2.0 OTG1



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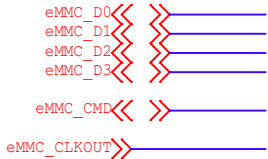


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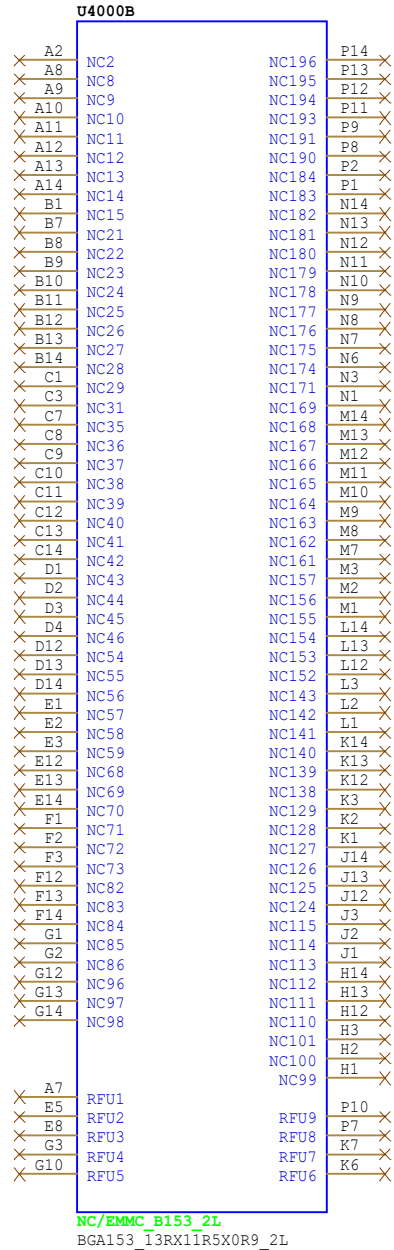
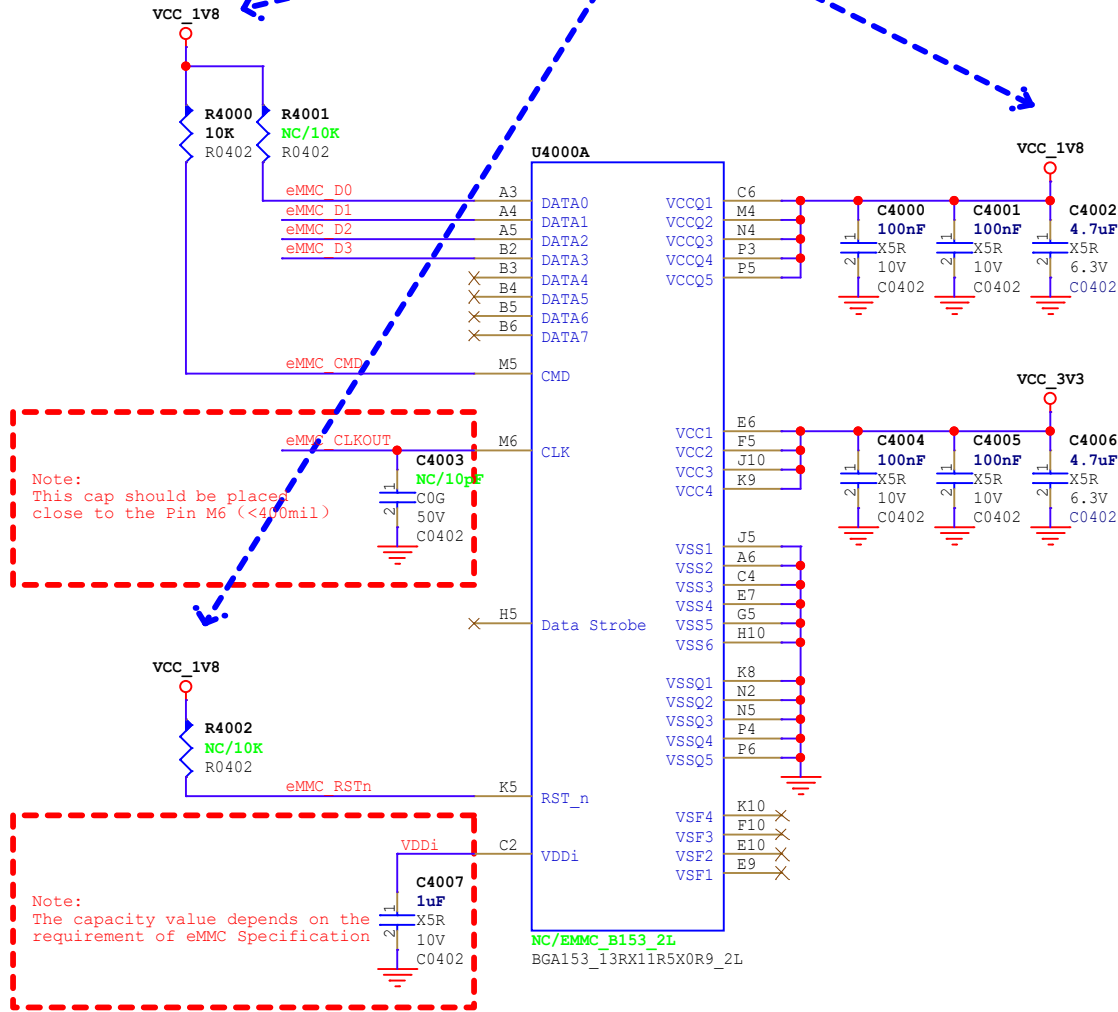
Project:	RK3506G_REF				
File:	25.USB-Port OTG				
Date:	Friday, November 15, 2024			Rev:	V1.1
Designed by:	whb	Reviewed by:		Sheet:	20 of 40




eMMC FLASH Option with SDMMC.



Note:  
The I/O voltage of the emmc must be consistent with that of the SOC VCCIO4 power domain.



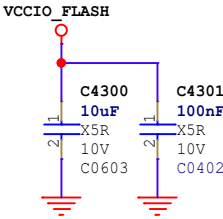
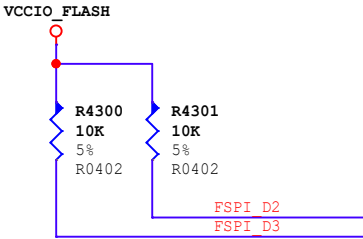
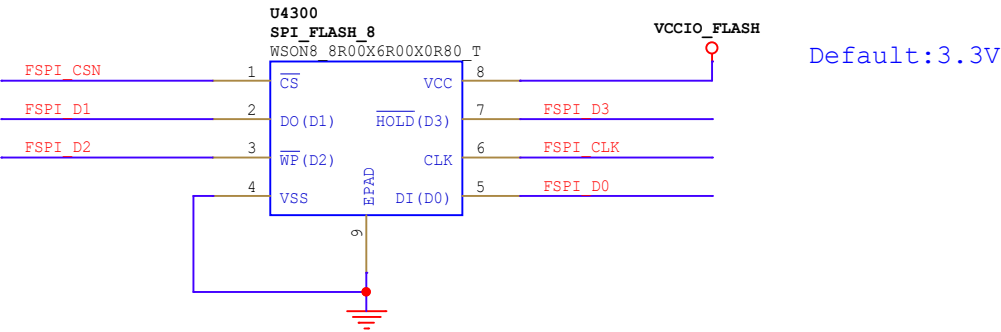
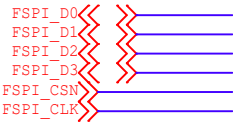
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		Rockchip Electronics Co., Ltd	
Project:	RK3506G_REF		
File:	40.Flash-eMMC(OPT)		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by:	Sheet: 21 of 40




# SPI Flash

NOTE:  
Refer to the latest AVL for parts selection.

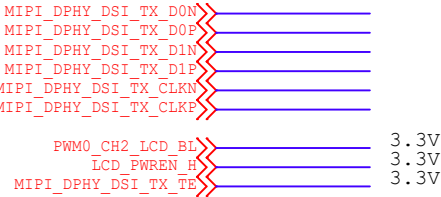


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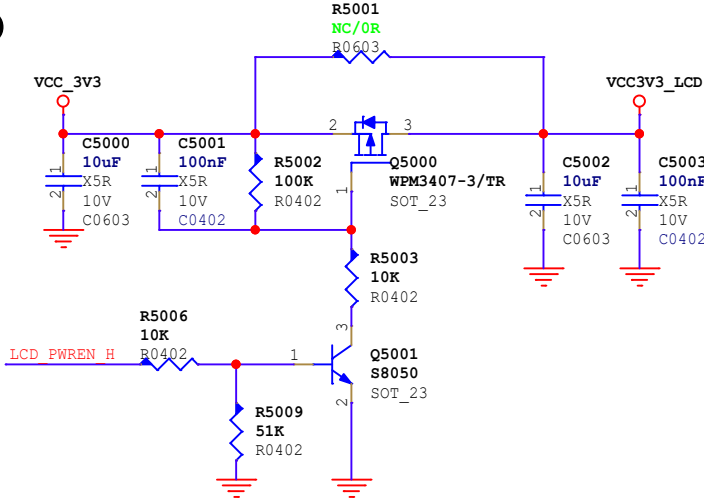
		Rockchip Electronics Co., Ltd	
Project:	RK3506G_REF		
File:	43.Flash-SPI Flash		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by: Default	Sheet: 22 of 40



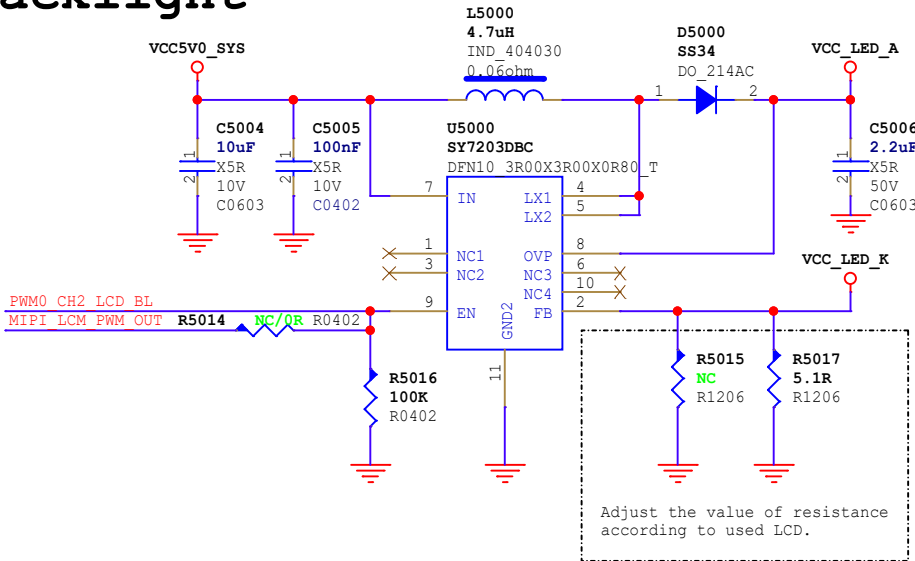
# MIPI DSI TX



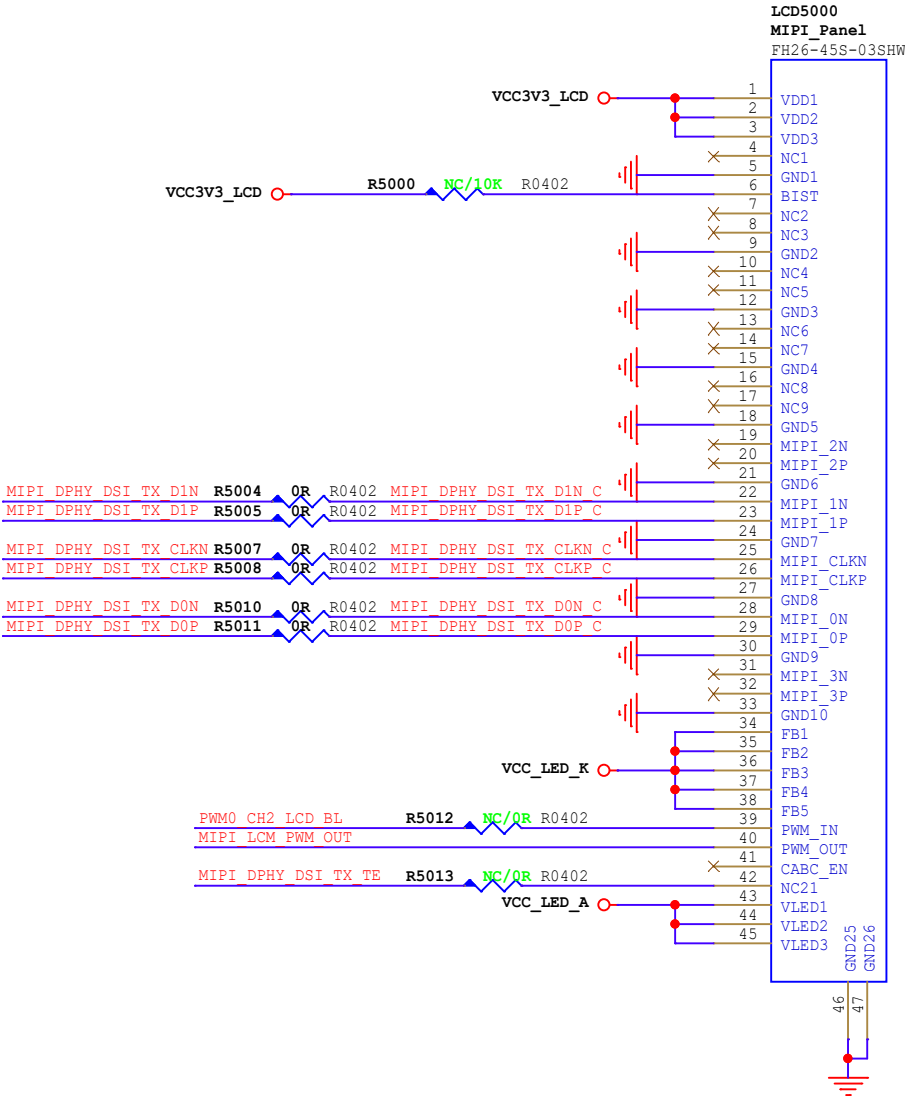
# Panel IO



# Backlight



# MIPI Panel Interface

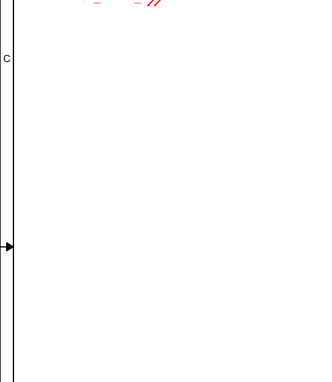


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Project:	RK3506G_REF		
File:	50.VO-MIPI_DSI		
Date:	Friday, November 15, 2024	Rev:	V1.1
Designed by:	whb	Reviewed by:	Default
Sheet:	23	of	40



[illegible]

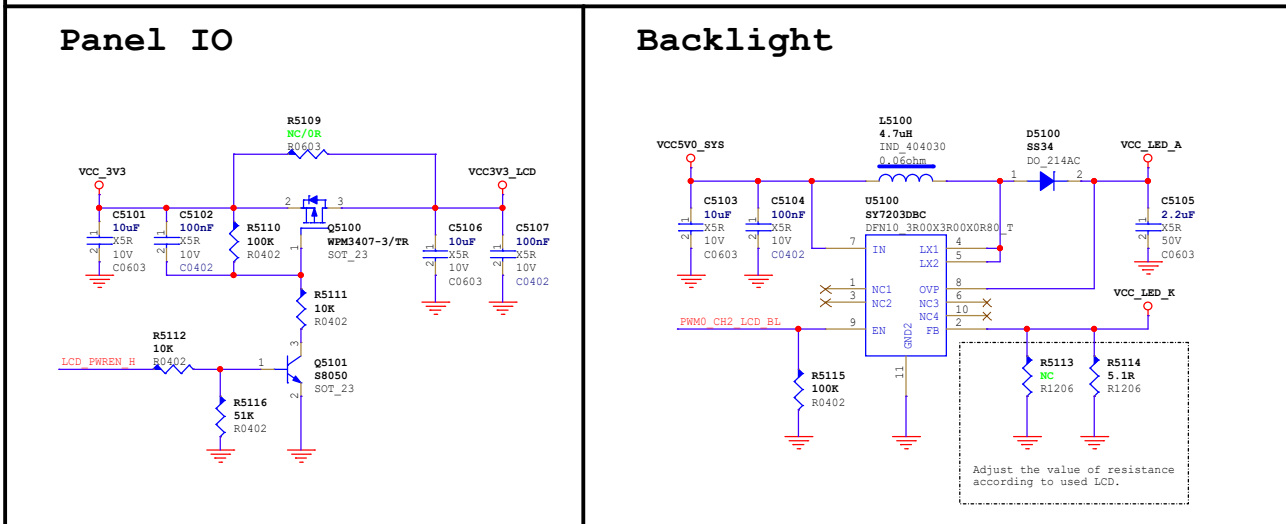
## Panel Configuration

The diagrams show five different configurations for the VCC3V3\_LCD pin. Each configuration consists of a pull-up resistor (R5100-R5104) and a pull-down resistor (R0402) connected to the VCC3V3\_LCD pin. The configurations are:

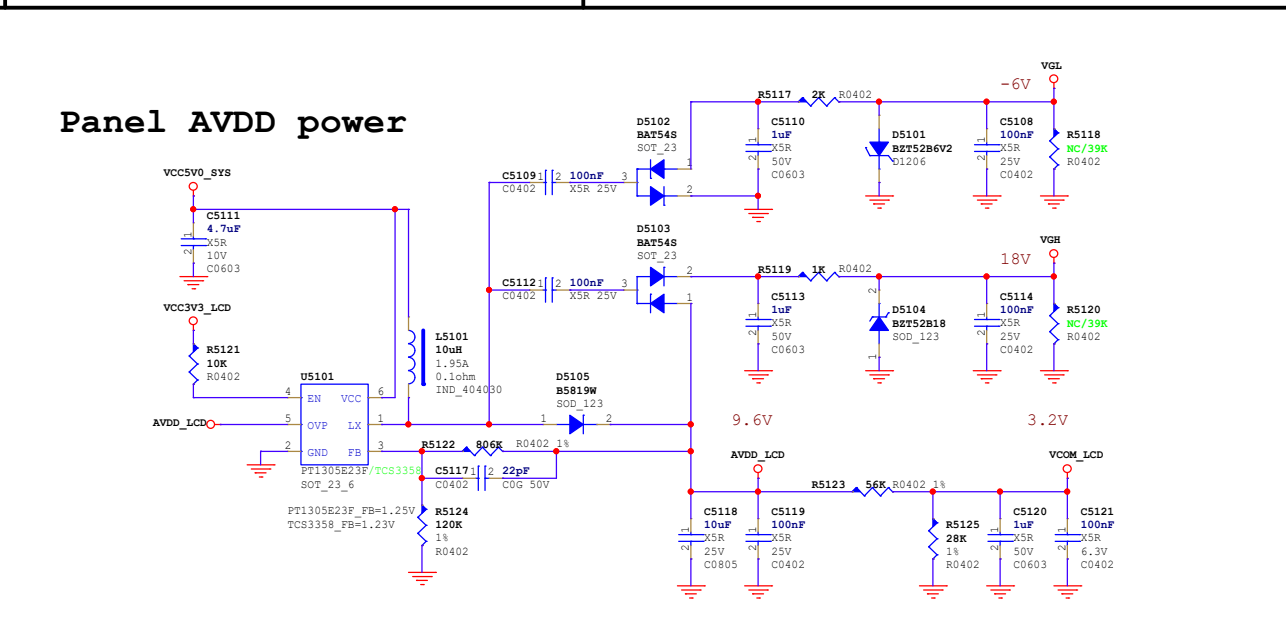
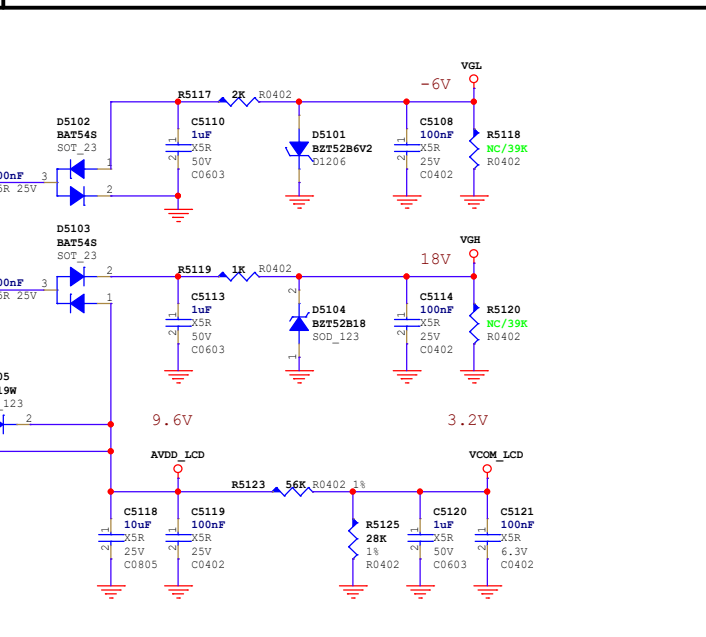
- Configuration 1:** R5100 (10K), R0402, LCD RST\_CON, CS100 (1uF), 6.3V, C0402.
- Configuration 2:** R5101 (10K), R0402, SHLR, R5105 (10K), R0402.
- Configuration 3:** R5102 (10K), R0402, UPDN, R5106 (10K), R0402.
- Configuration 4:** R5103 (10K), R0402, DITH, R5107 (10K), R0402.
- Configuration 5:** R5104 (10K), R0402, LCD MODE, R5108 (10K), R0402.

Legend:

- H: shift right
- L: shift left
- H: up shift
- L: down shift
- H: 6bit resolution
- L: 8bit resolution
- H: DE mode
- L: HS/VS mode



# Panel IO

[illegible]

**J5100**

**RGB\_Panel**

FPC50PIN\_DOWN1

GND\_6

VCOM\_LCD

AVDD\_LCD

DITH

LCD\_RST\_CON

VGL

VGH

UPDN

SHLR

VO\_LCDC\_CLK

VO\_LCDC\_DI6

VO\_LCDC\_DI7

VO\_LCDC\_DI8

VO\_LCDC\_DI9

VO\_LCDC\_D20

VO\_LCDC\_D21

VO\_LCDC\_D22

VO\_LCDC\_D23

VO\_LCDC\_D8

VO\_LCDC\_D9

VO\_LCDC\_DI0

VO\_LCDC\_DI1

VO\_LCDC\_DI2

VO\_LCDC\_DI3

VO\_LCDC\_DI4

VO\_LCDC\_DI5

VO\_LCDC\_DI0

VO\_LCDC\_DI1

VO\_LCDC\_D2

VO\_LCDC\_D3

VO\_LCDC\_D4

VO\_LCDC\_D5

VO\_LCDC\_D6

VO\_LCDC\_D7

VO\_LCDC\_HSYNC

VO\_LCDC\_VSYNC

VO\_LCDC\_DEN

LCD\_MODE

VCC3V3\_LCD

VCOM\_LCD

VCC\_LED\_K

VCC\_LED\_A

VCC3V3\_LCD

C5115

4.7uF

X5R

10V

C0603

C5116

100nF

X5R

6.3V

C0402

NC\_2

NC\_1

GND\_4

DITH

VCOM

NC

RSTB

AVDD

VGL

VGH

UPDN

SHLR

GND\_3

DCLK

GND\_2

R0

R1

R2

R3

R4

R5

R6

R7

G0

G1

G2

G3

G4

G5

G6

G7

B0

B1

B2

B3

B4

B5

B6

B7

HSD

VSD

DE

MODE

DVD

VCOM\_1

GND\_1

VLED+\_2

VLED-\_1

VLED+\_1

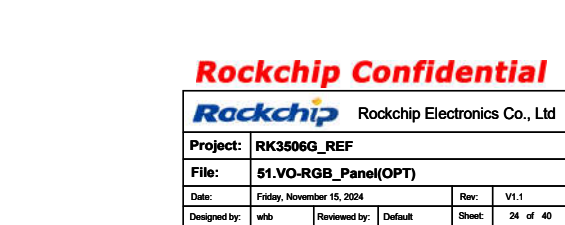
VLED-\_2



GND

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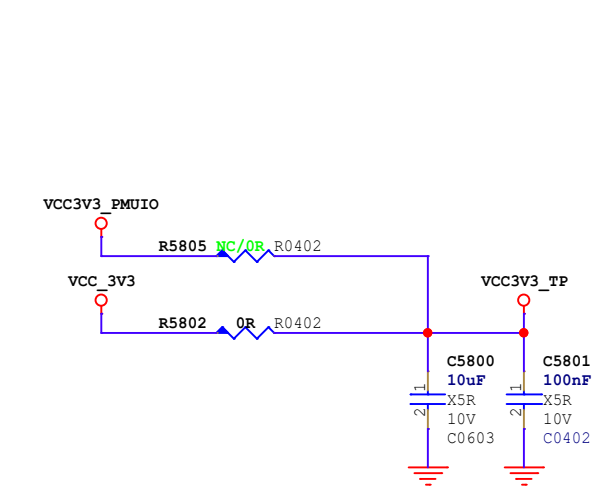
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Drawn by:	wbh	Reviewed by:	Default
Sheet:	24	Total:	40



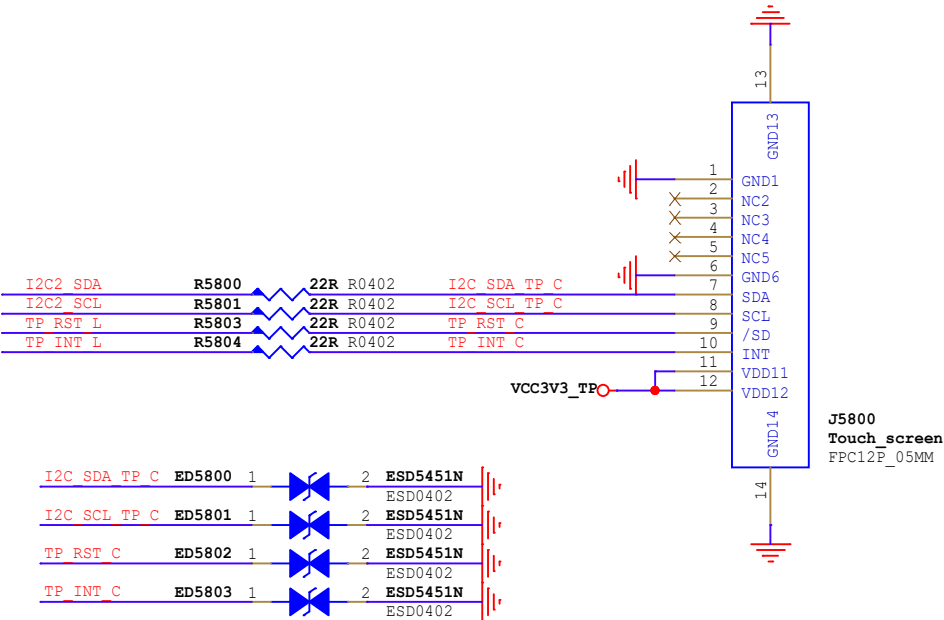
			
		Rockchip Electronics Co., Ltd	
Project:	RK3506G_REF		
File:	S1.VO-RGB_Panel(OPT)		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by: Default	Sheet: 24 of 40




TP



Default not support touch to wake-up under sleep mode. If touch wake-up is needed, you can move this circuits to the power domain of VCC3V3\_PMUIO. Please note that in this usage, the TP module will increase the standby current.

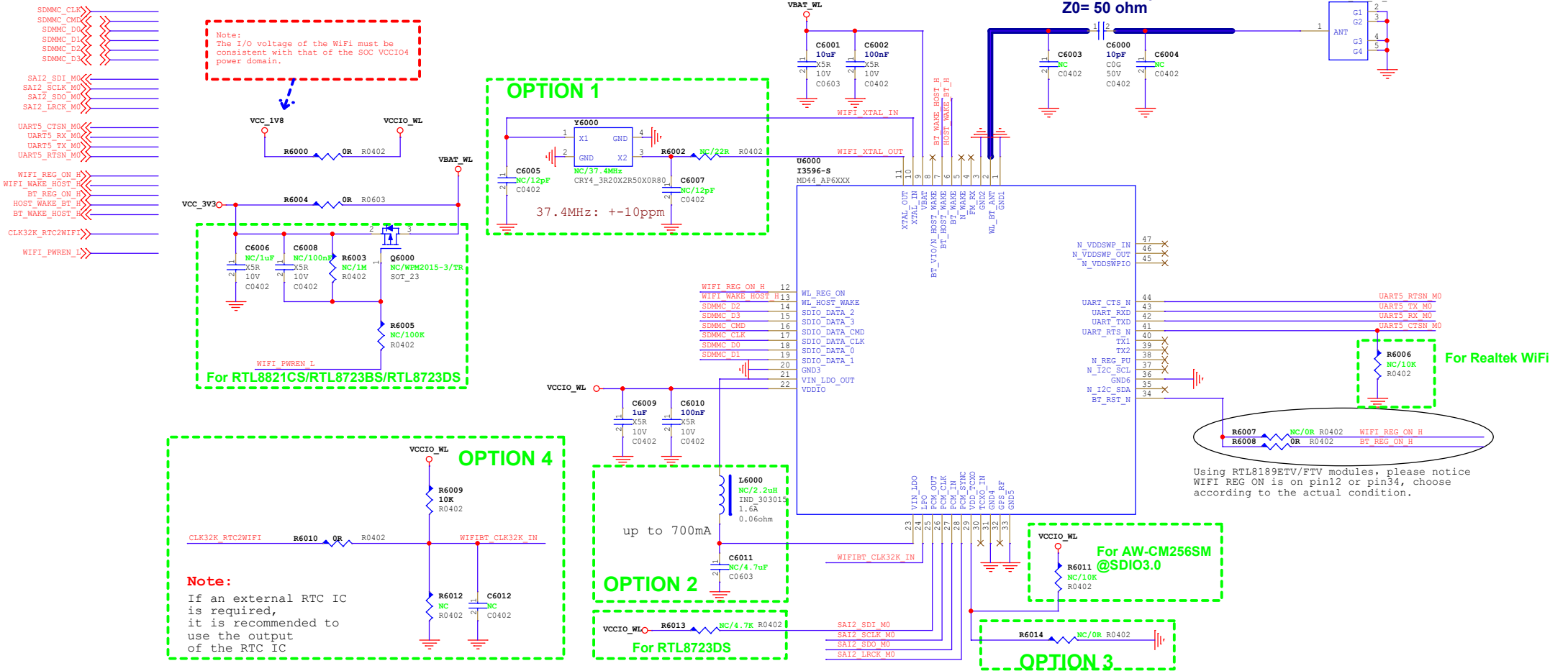


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Project:	RK3506G_REF		
File:	58.TP Connector_COF		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by: Default	Sheet: 25 of 40



# WIFI/BT Module *Option with eMMC/RMII1.*



OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
RK960 Module I3596-S	No	Yes	No	No	5.3	Module Integrated	1.8V/3.3V	No	No	No	Yes
CYM43455 Module AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Note:  
Yes: option circuit be mounted  
No: option circuit not be mounted



```

RMII0_TXD0<<
RMII0_TXD1<<
RMII0_TXEN<<

RMII0_RXD0<<
RMII0_RXD1<<
RMII0_RXDV_CRS<<

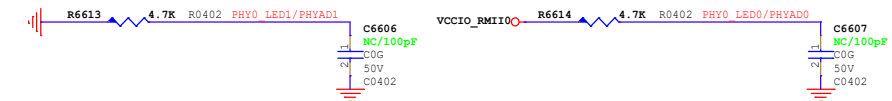
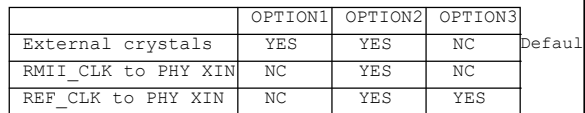
RMII0_CLK<<

RMII0_MDIQ<< >>
RMII0_MDC<<

RMII0_RSTn<<

ETH_CLK0_25M_OUT<<

```

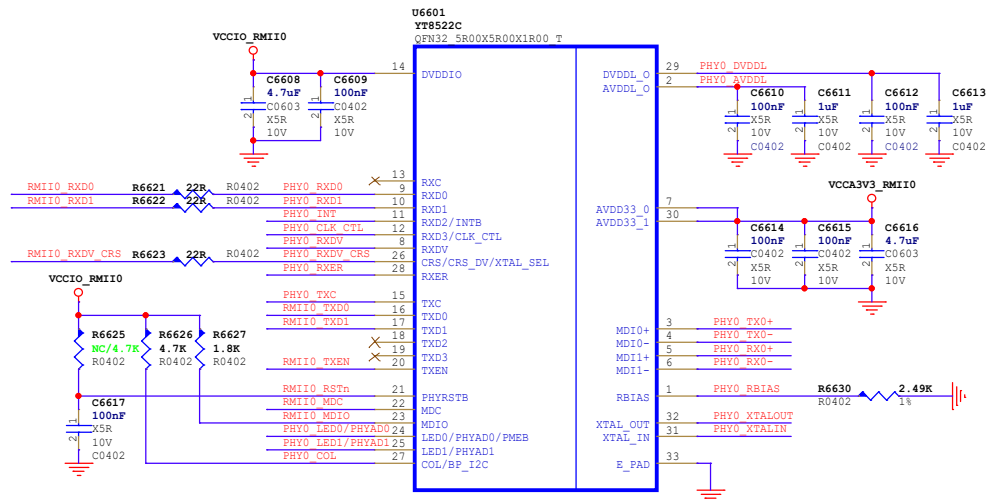


PHY Address	PHYAD[1:0]
1 (default)	2'b01



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Designed by:	whb	Reviewed by:		Sheet:	27 of 40
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Option with  
SAI2/UART5.

**OPTION1**

**PHY1 XTALOUT**

**PHY1 XTALIN**

**R6700**  
25MHz  
CRY4 3R20X2R50X0R80

**C6700**  
12pF  
COG  
50V  
C0402

**C6701**  
12pF  
COG  
50V  
C0402

**OPTION2**

**RMII1\_CLK**

**R6704** **OR** **R0402**

**PHY1\_TXC**

**MAC** -----> **PHY**

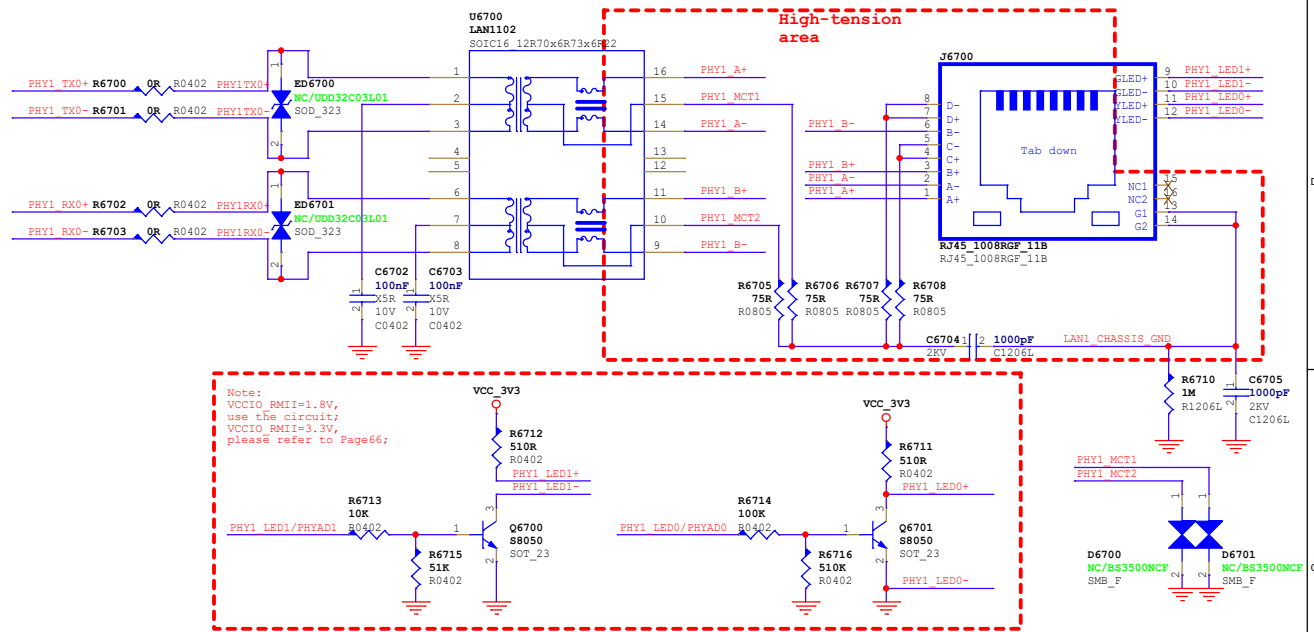
**OPTION3**

**ETH\_CLK1\_25M\_OUT**

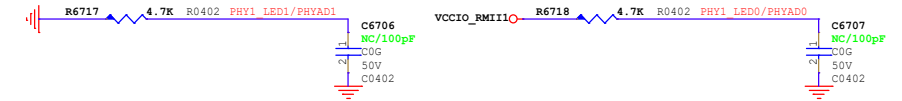
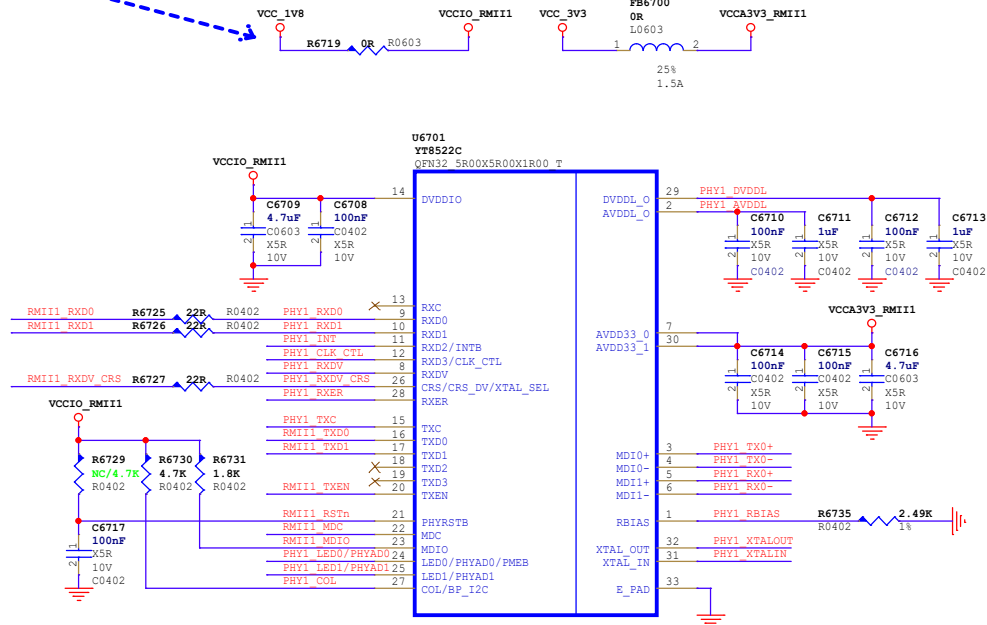
**R6709** **NC/OR** **R0402**

**PHY1\_XTALIN**

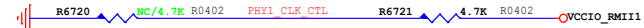
	OPTION1	OPTION2	OPTION3	
External crystals	YES	YES	NC	Default
RMII_CLK to PHY XIN	NC	YES	NC	
REF_CLK to PHY XIN	NC	YES	YES	



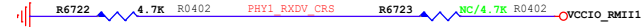
Note:  
The I/O voltage of the RMMI must be consistent with that of the SOC VCCIO4 power domain.



PHY Address	PHYAD[1:0]
1 (default)	2'b01



**Reference Clock input selection**  
(0 = Reference Clock from XTAC; 1 = Reference Clock from TXC)



PHY1 RXDV R6728 4.7K R0402 VCCIO\_RMII1

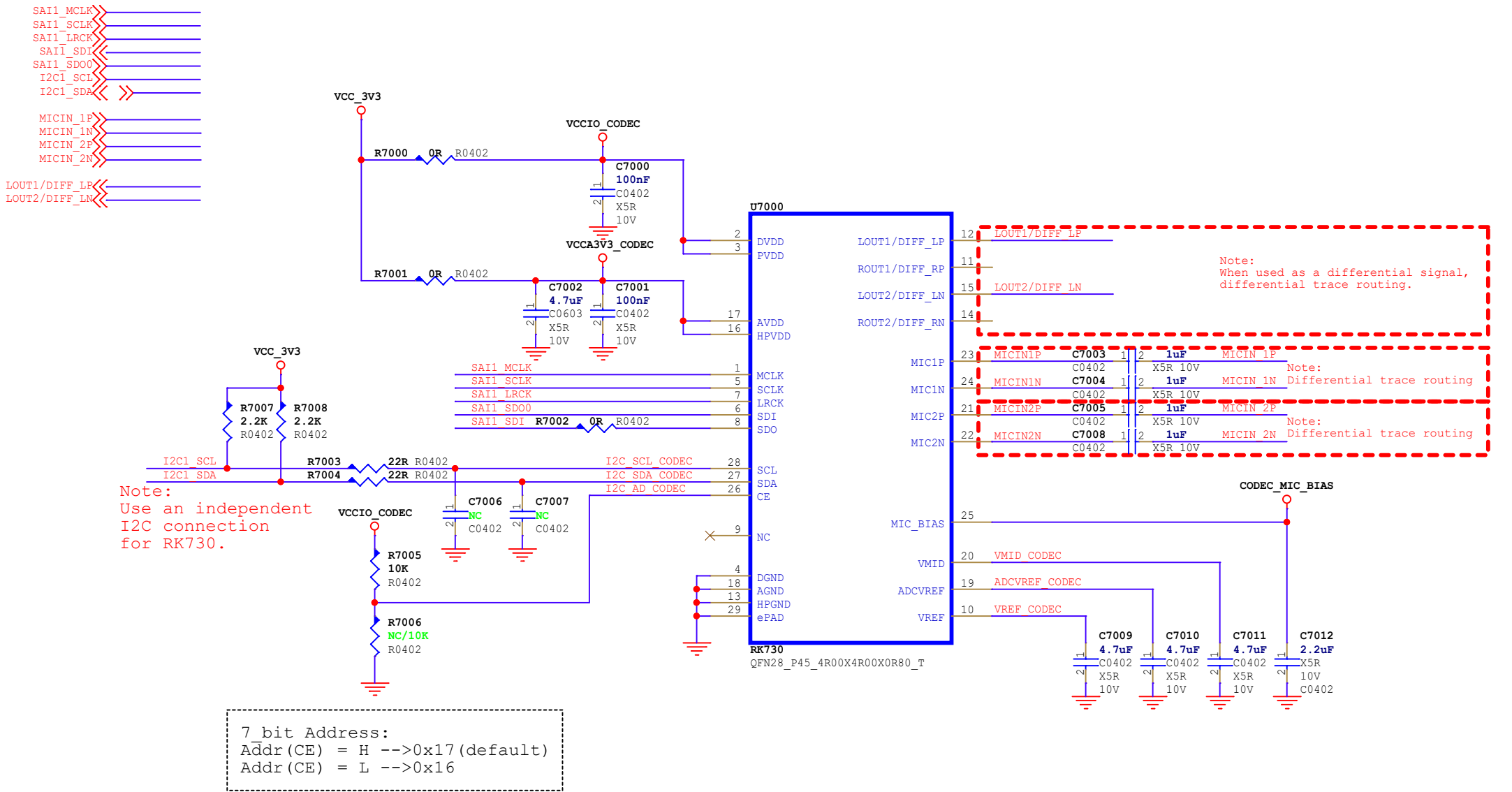


R6737 4.7K R0402 PHY1 RXER R6738 NC/4.7K R0402 VCCIO\_RMI1


**UTP / Fiber Selection (0 = UTP Mode(default); 1 = Fiber Mode)**



ACODEC Option with SPI0.

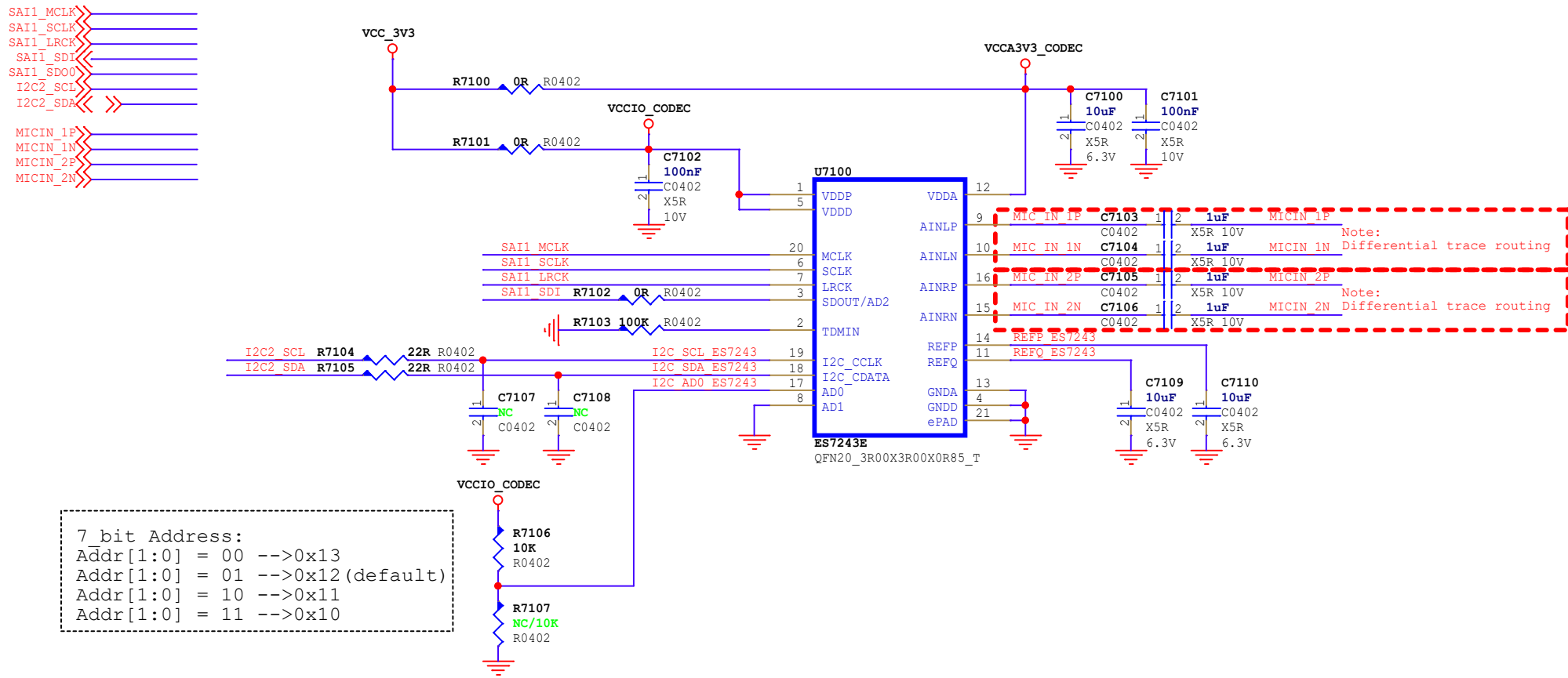


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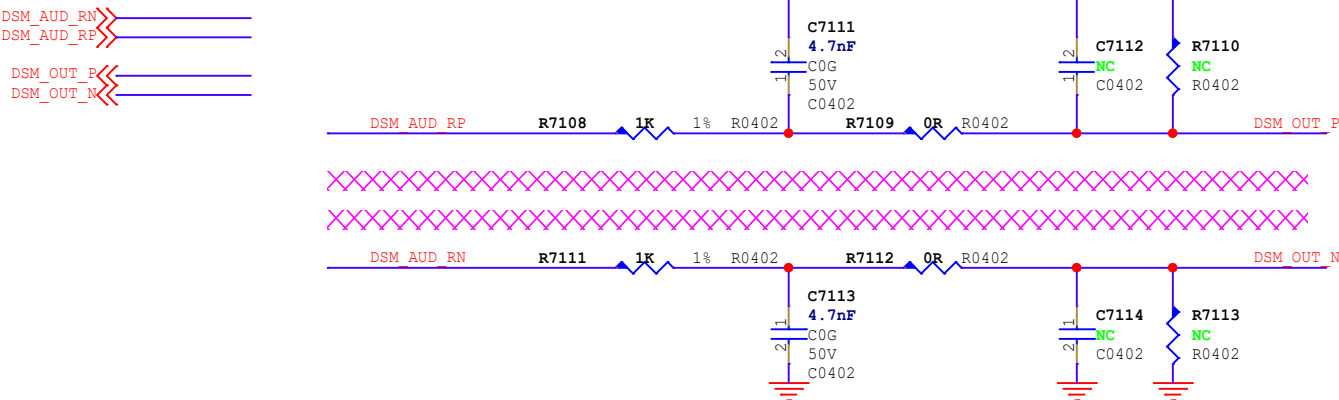
		Rockchip Electronics Co., Ltd	
Project:	RK3506G_REF		
File:	70.Audio-Codec		
Date:	Friday, November 15, 2024	Rev:	V1.1
Designed by:	whb	Reviewed by:	
		Sheet:	29 of 40



# ACODEC Option with SPI0.




## DSM



Note:  
Differential/Balanced Audio Signals!  
Layout must be routing by differential

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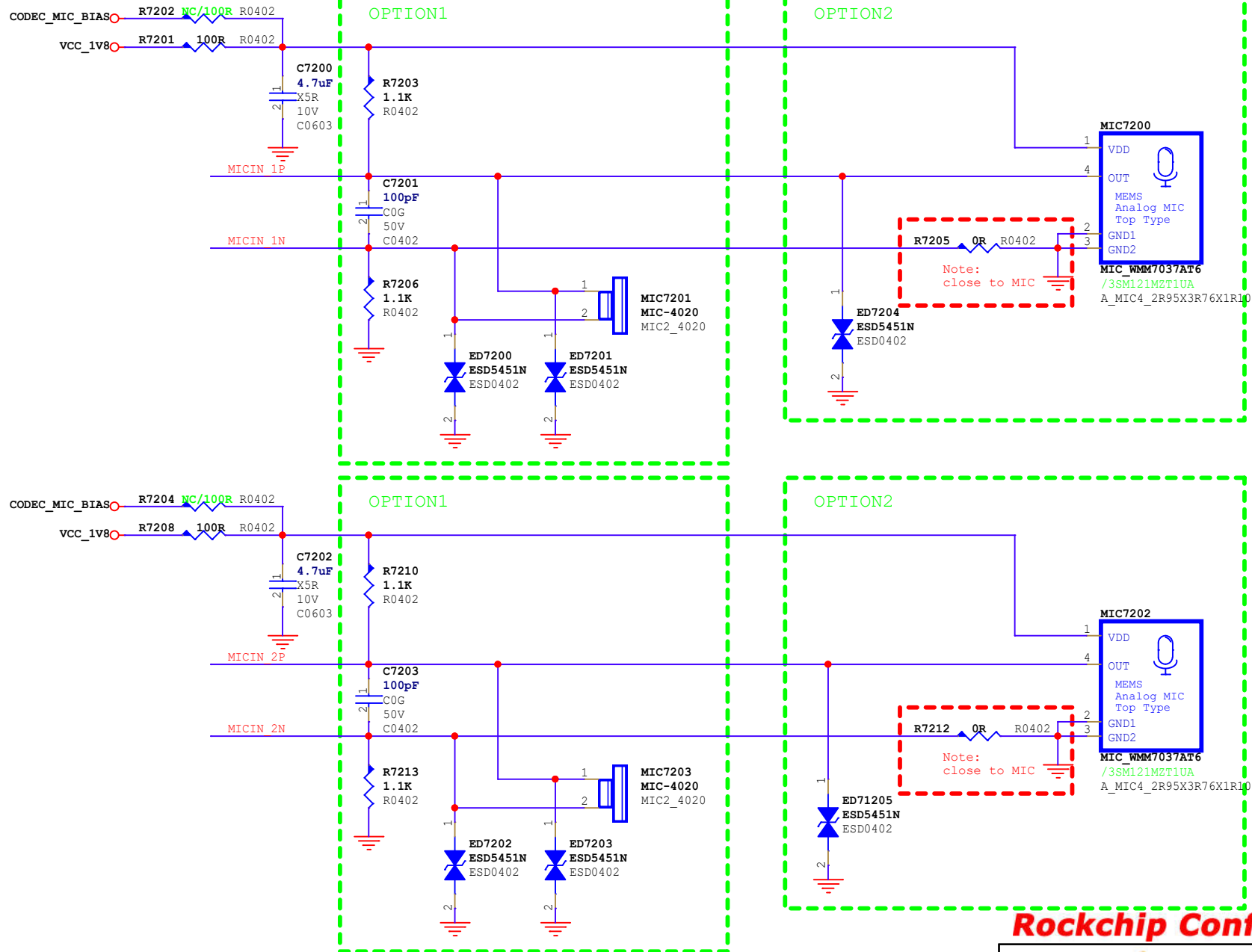
Rockchip Electronics Co., Ltd

Project:	RK3506G_REF		
File:	71.Audio-ES7243+DSM(OPT)		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by:	
		Sheet:	30 of 40




# MIC

MICIN\_1P  
MICIN\_1N  
MICIN\_2P  
MICIN\_2N



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Project:	RK3506G_REF		
File:	72.Audio-MIC		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by:	Sheet: 31 of 40



# SPEAKER PA

LOUT1/DIFF\_LP  
LOUT2/DIFF\_LN  
SPK\_CTRL

ACODEC\_ADC\_INP  
ACODEC\_ADC\_INN

DSM\_OUT\_P  
DSM\_OUT\_N

VCC5V0\_SYS  
VCC\_PA

L7300  
120R-100MHz  
L0603  
2A  
25%

SPK\_CTRL

R7300  
100K  
R0402

VHmin:1V

U7300  
OUTN  
VREF  
INN  
VDD  
INP  
OUTP  
TCS7191A MH  
msop8\_3r10x3r10x1r10

Note:  
Place close to Amp

FB7300  
120R-100M L0603  
1.3A 0.25  
AUDIO BEAD  
FB7301  
120R-100M L0603  
1.3A 0.25  
AUDIO BEAD

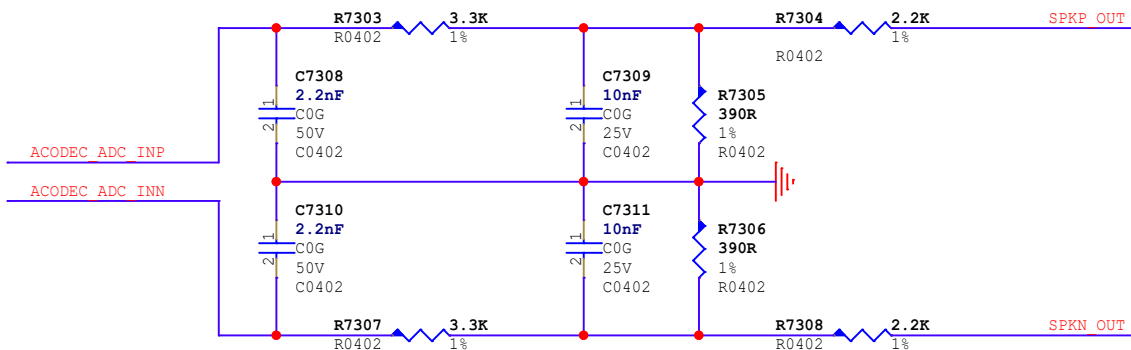
Note:  
Place close to Jack

J7300

Audio\_SPK\_Jack\_2P\_V  
CN2ML\_2R00\_V\_P\_DIP

Note:  
Place close to Amp

Gain=Rf/ (Ri +6k) , 即Gain=576k/ (75k +6k) =7.1  
Fc=196Hz



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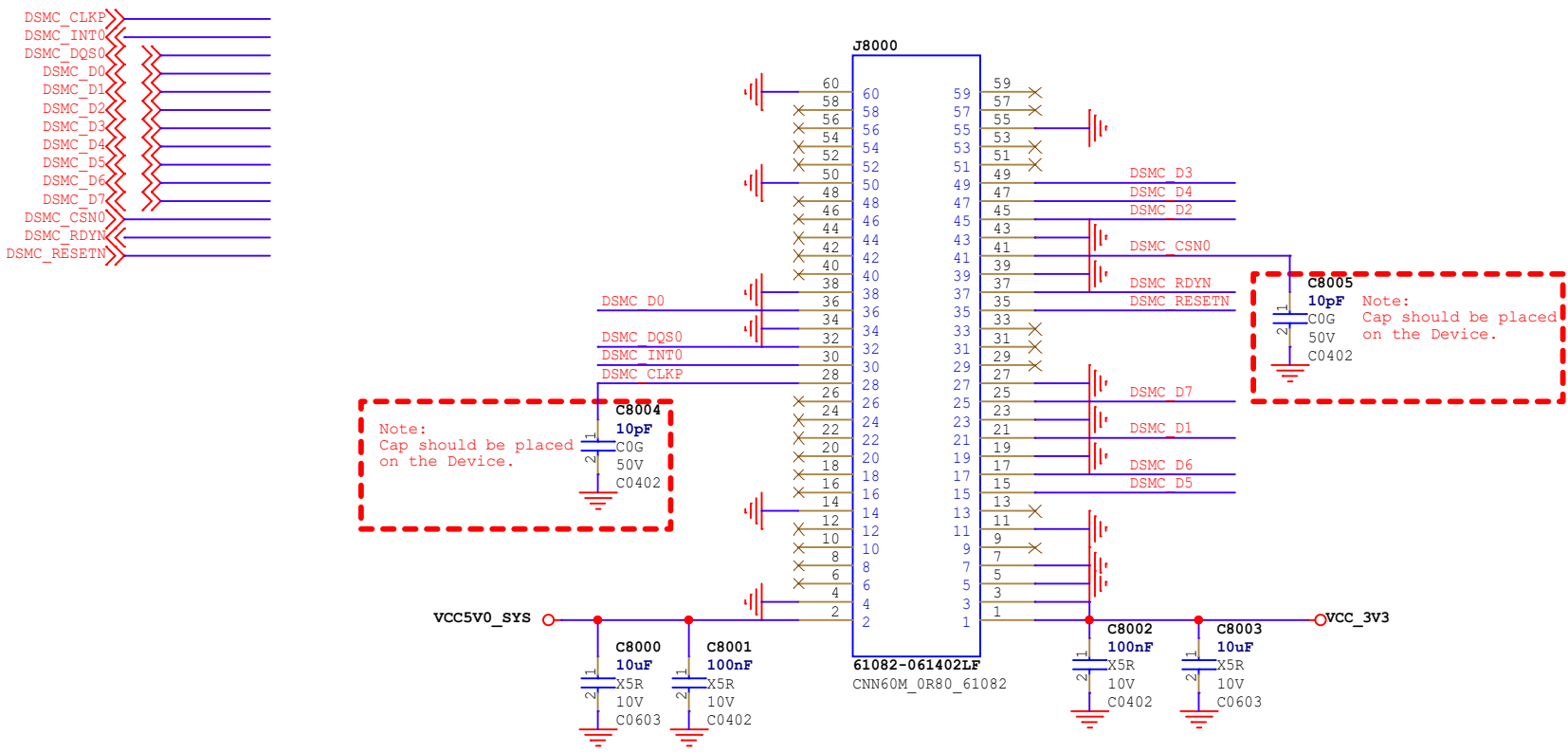
Rockchip Electronics Co., Ltd

Project:	RK3506G_REF		
File:	73.Audio-AMP		
Date:	Friday, November 15, 2024	Rev:	V1.1
Designed by:	whb	Reviewed by:	
Sheet:	32 of 40		




# DSMC

Option with RGB panel.



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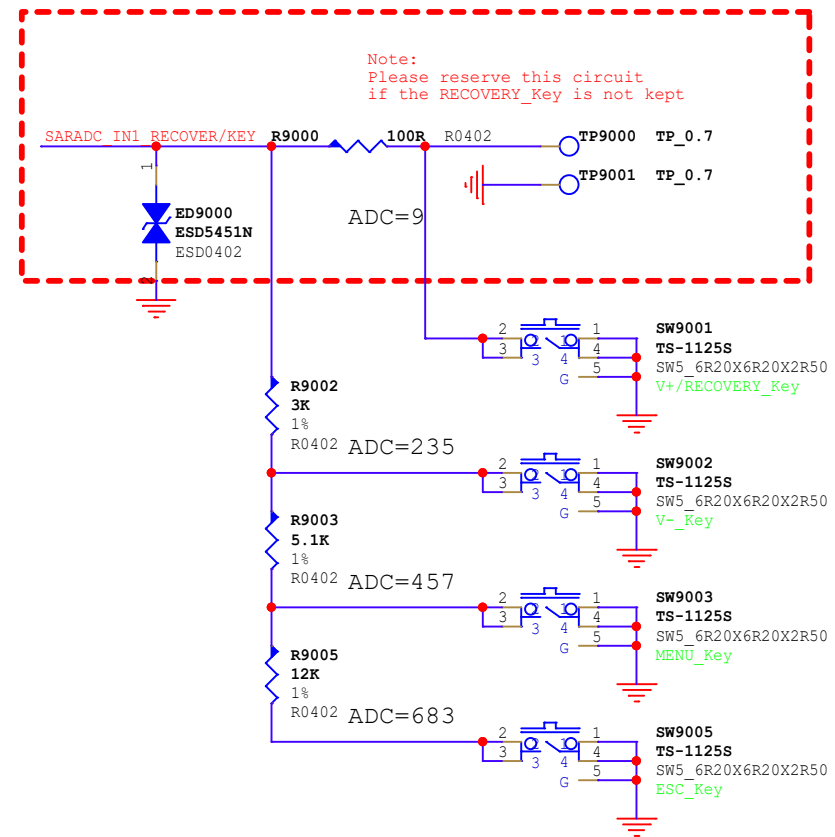
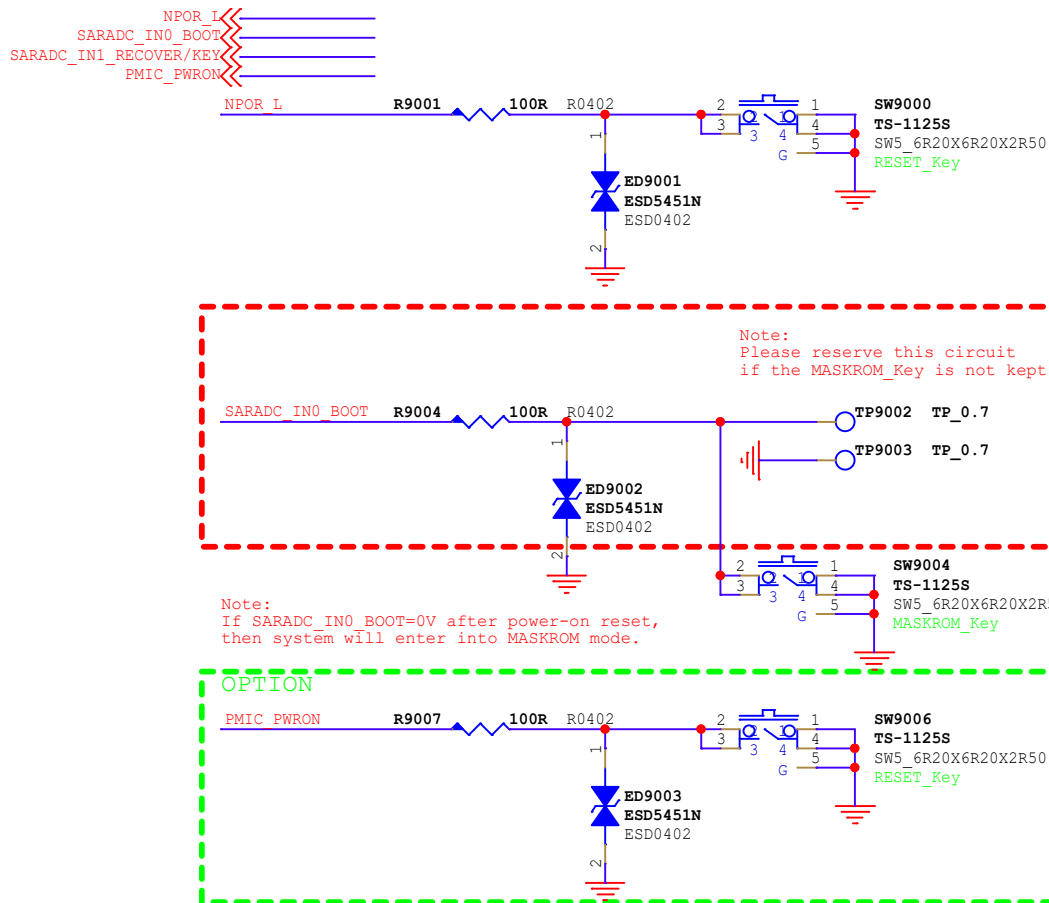


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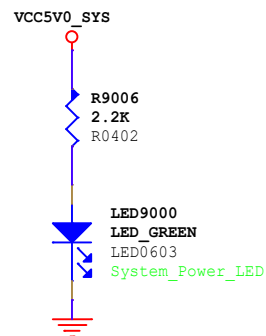
Project:	RK3506G_REF				
File:	80.DSMC				
Date:	Friday, November 15, 2024			Rev:	V1.1
Designed by:	whb	Reviewed by:	Default	Sheet:	33 of 40




# KEY



# Work\_LED



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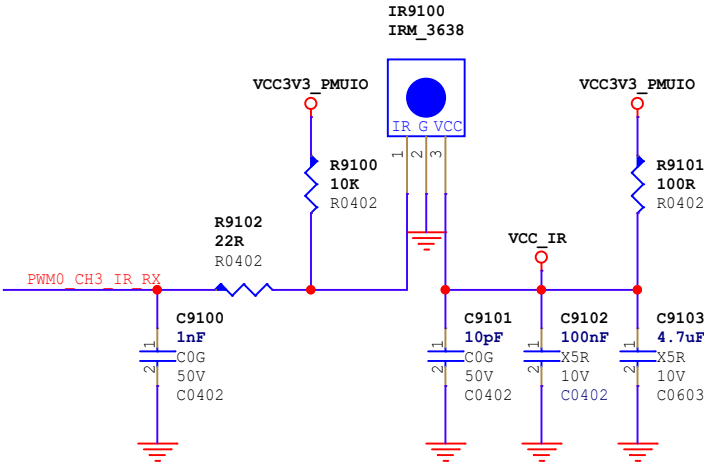
		Rockchip Electronics Co., Ltd	
Project:	RK3506G_REF		
File:	90.KEY_Array/LED		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by:	Sheet: 34 of 40



# IR Receiver

Option with UART2.

PWM0\_CH3\_IR\_RX<<<

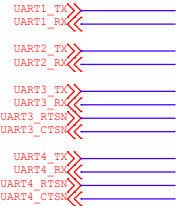


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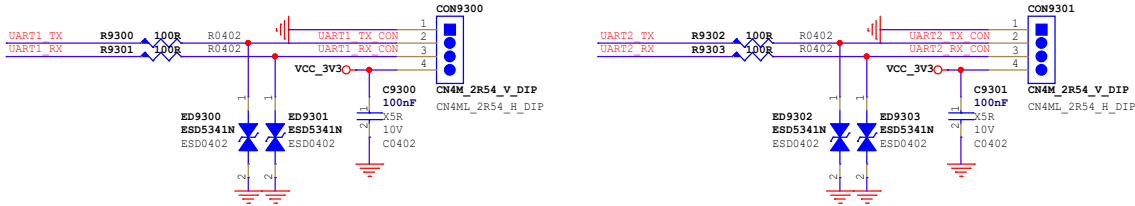
<b>Rockchip</b> Rockchip Electronics Co., Ltd			
Project:	RK3506G_REF		
File:	91.IR_RX		
Date:	Friday, November 15, 2024	Rev:	V1.1
Designed by:	whb	Reviewed by:	Sheet: 35 of 40



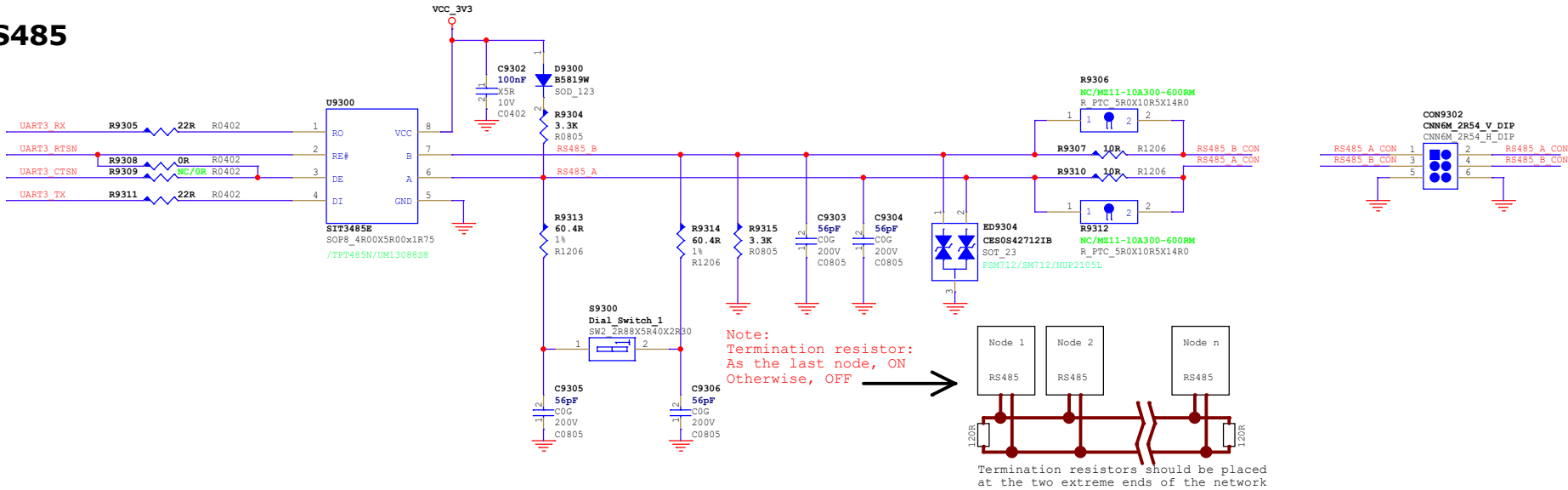
UART



Option with PMIC.

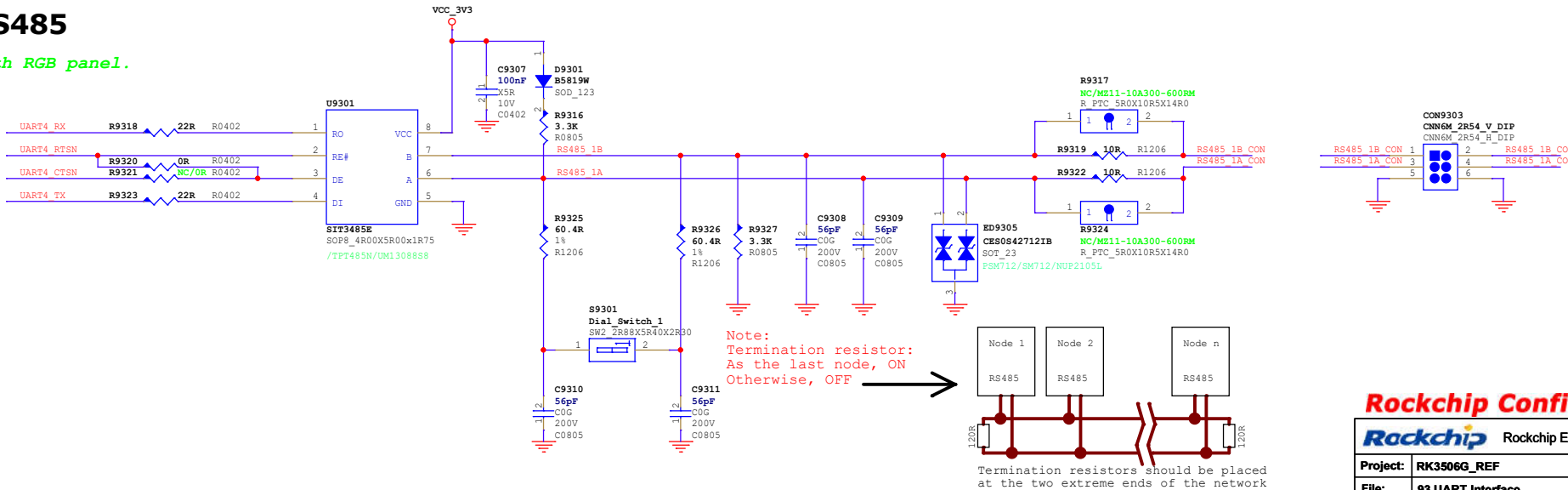


UART3 RS485



UART4 RS485

Option with RGB panel.



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Project: RK3506G\_REF

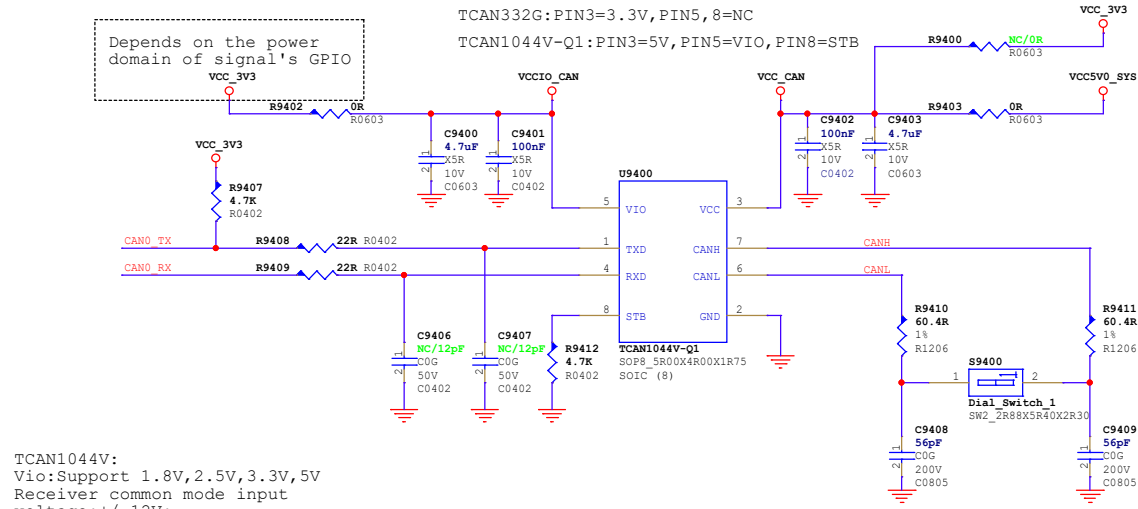
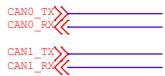
File: 93.UART Interface

Date: Friday, November 15, 2024 Rev: V1.1

Designed by: whb Reviewed by: Sheet: 36 of 40

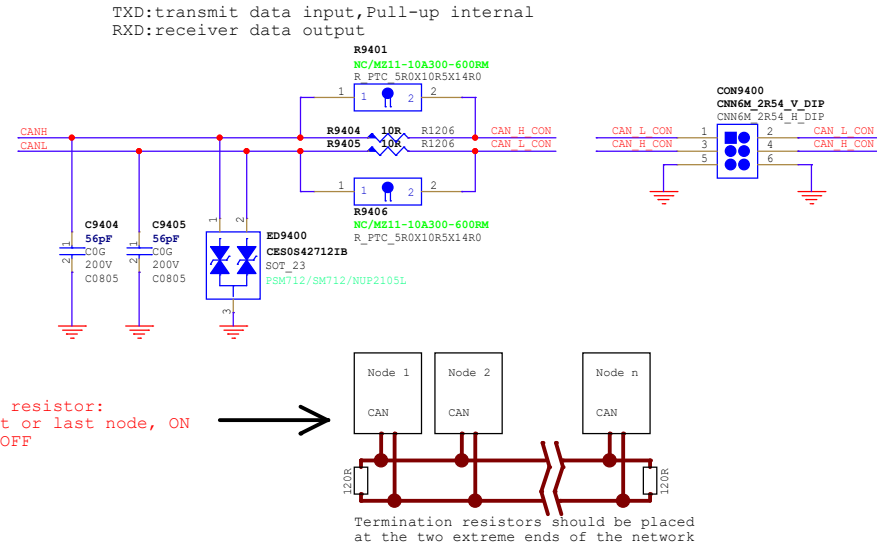


CAN0



TCAN1044V:  
Vio:Support 1.8V,2.5V,3.3V,5V  
Receiver common mode input  
voltage:+/-12V;  
Support of classical CAN and optimized  
CAN FD performance at 2,5,and 8 Mbps.  
Temperature grade:-40 to 125

STB(Standby)  
The STB pin is an input pin used for mode control of the  
transcervier.The STB pin can be supplied from either the  
system processor or from a static system voltage source,If  
normal mode is the only intended mode of operation then  
the STB pin can be tired directly to GND.



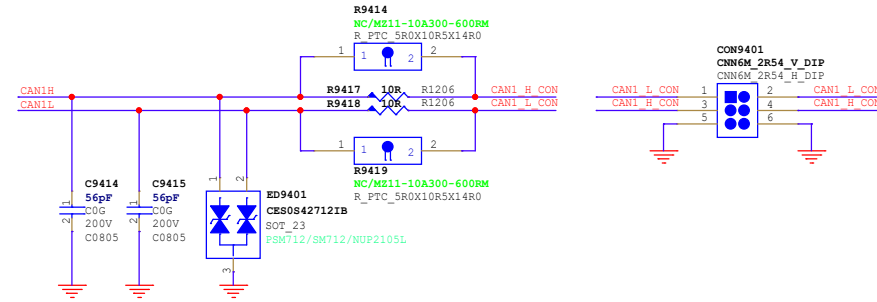
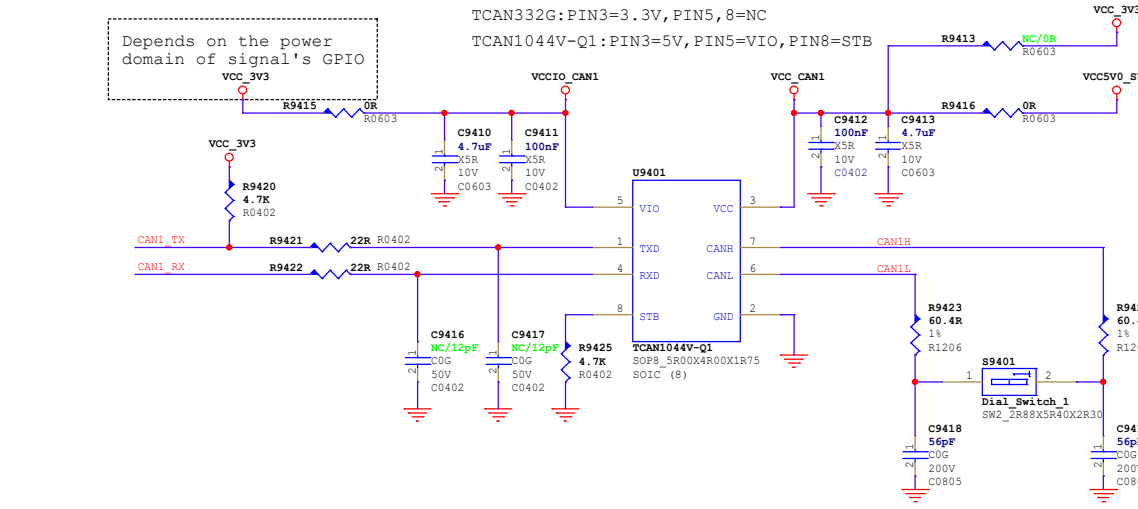
Note:  
Termination resistor:  
As the first or last node, ON  
Otherwise, OFF

Table 5. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See section 8.3.3.1
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

CAN1

Option with RGB panel.



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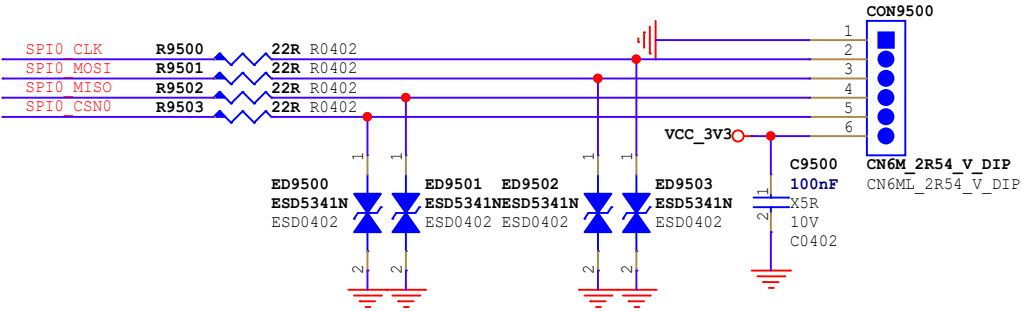
Project:	RK3506G_REF		
File:	94.CAN Interface		
Date:	Friday, November 15, 2024	Rev:	V1.1
Designed by:	whb	Reviewed by:	
Sheet:	37 of 40		



# SPI

Option with SAIL.

SPI0\_CLK  
SPI0\_MOSI  
SPI0\_MISO  
SPI0\_CSNO



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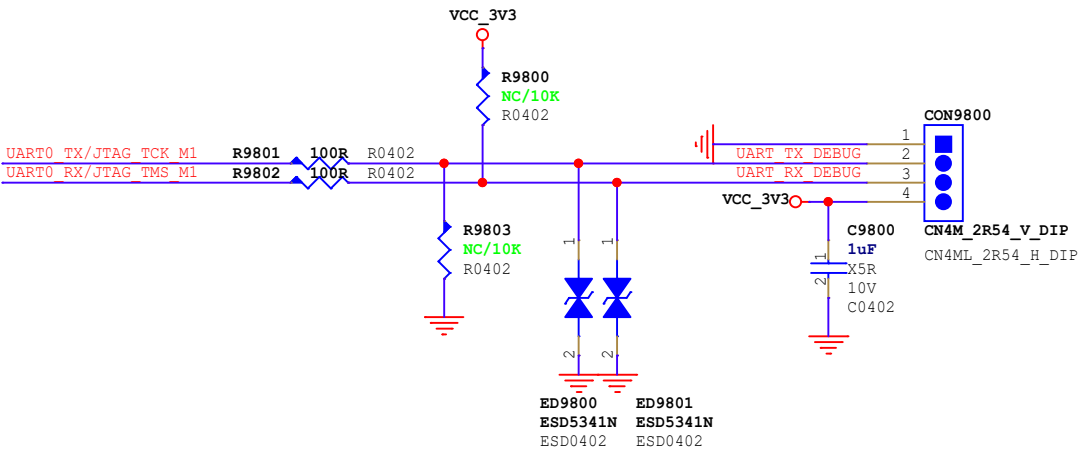
Rockchip Electronics Co., Ltd

Project:	RK3506G_REF		
File:	95.SPI Interface		
Date:	Friday, November 15, 2024	Rev:	V1.1
Designed by:	whb	Reviewed by:	Sheet: 38 of 40




# UART0 Debug

UART0\_TX/JTAG\_TCK\_M1  
UART0\_RX/JTAG\_TMS\_M1

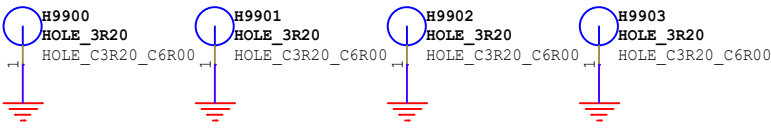


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		Rockchip Electronics Co., Ltd	
Project:	RK3506G_REF		
File:	98.UART/JTAG Debug Port		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by:	39 of 40



# Hole



# PCB Mark Point


TOP Mark



BOTTOM Mark



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		Rockchip Electronics Co., Ltd	
Project:	RK3506G_REF		
File:	99.Mark/Hole		
Date:	Friday, November 15, 2024		Rev: V1.1
Designed by:	whb	Reviewed by:	Sheet: 40 of 40