# Reference Schematic For PX30

## PX30_REF_V1.2

PMIC: RK809-1 (5BUCK + 9LDO + Codec)
RAM: DDR3 /LPDDR3/DDR4
ROM: eMMC/Nand + TF card
Interface: MIPI CSI/MIPI DSI/UART/I2S/RMII



| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 00.Cover Page | | |
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# Note

**NOTE 1:**
**Component parameter description**

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted
3. If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted

**NOTE 2:**
**Please use our recommended components to avoid too many changes.For more informations about the second source,please refer to our AVL.**

Note

Option

Description

Remind

**Bill of Materials**

**Header:**

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

**Combined property string:**

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

| | | | |
|---|---|---|---|
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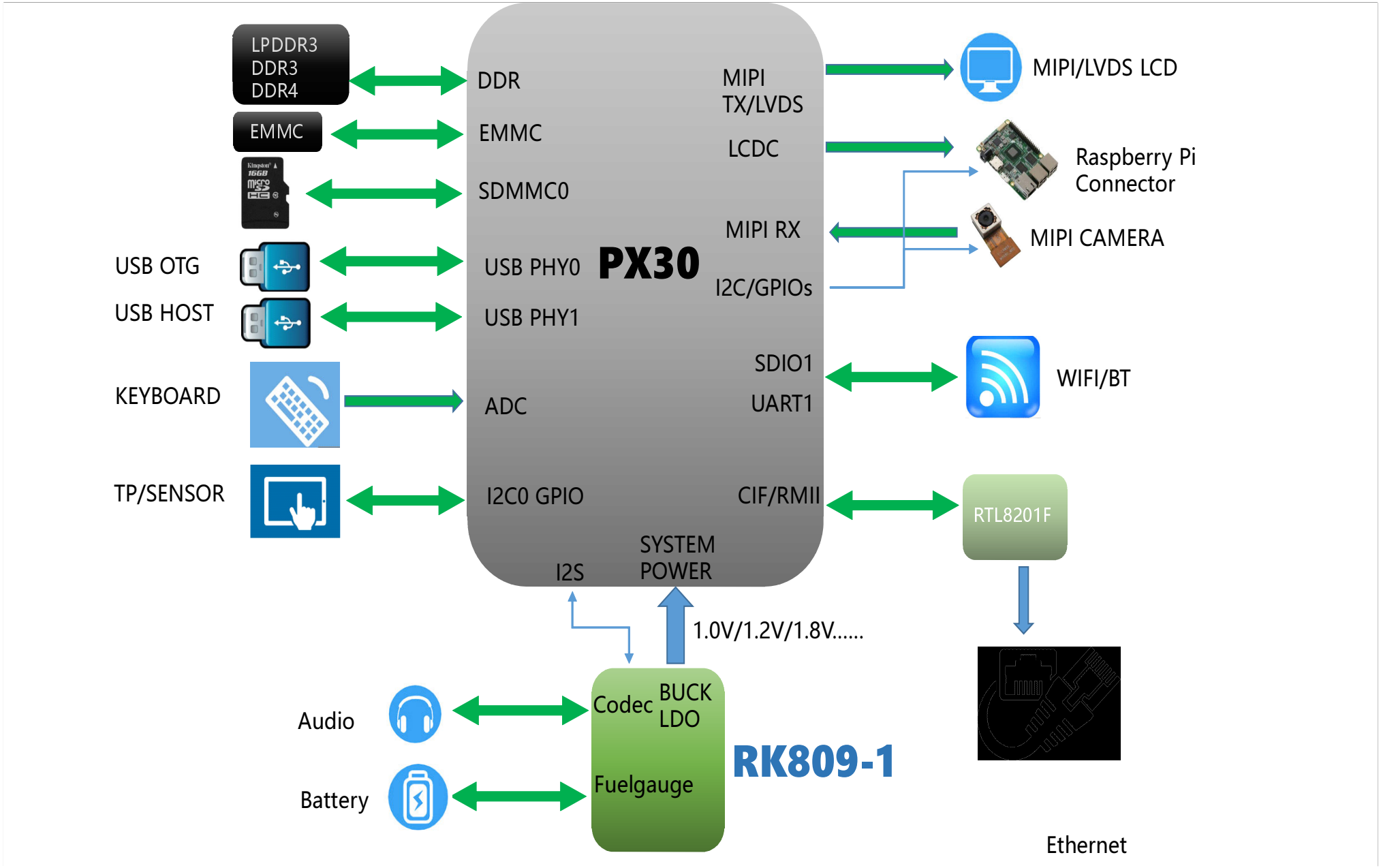
| Version | Date | Author | Change List | Approved |
|---|---|---|---|---|
| V1.0 | 20180504 | XHF | First edition for PX30 | |
| V1.1 | 20180928 | XHF | 1.Update the schematic of RK809<br>2.VREF0_DDR and VREF1_DDR are unified as VREF0_DDR<br>3.DDR_CKE changed to DDR_CKE0 | |
| V1.2 | 20190507 | XHF | 1.VREF0_DDR and VREF_DDR are linked together.<br>2.RK618 IS0_LRCK_RX and IS0_LRCK_TX are linked together.<br>3.Add a diode to RK809 RTC power supply foot | |




| | | | |
|---|---|---|---|
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| Project: | PX30 REF | | |
| File: | 03.Block Diagram | | |
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# I2C MAP

| Port | Pin name | Domain | Bus name | Pull-up voltage | Slave Device | Slave Addr (MS 7Bits) | Note | Slave Bus Capability |
|---|---|---|---|---|---|---|---|---|
| I2C0 | I2C0_SCL/GPIO0_B0_u<br>I2C0_SDA/GPIO0_B1_u | PMUIO2 | I2C0_SCL_PMIC<br>I2C0_SDA_PMIC | VCC3V0_PMU | Rockchip RK809 | 0x20 | PMIC | |
| | | | | | Rockchip RK618 | 0x50 | Video | |
| I2C1 | I2C1_SCL/PMU_DEBUG5/GPIO0_C2_u<br>I2C1_SDA/GPIO0_C3_u | PMUIO2 | I2C1_SCL<br>I2C1_SDA | VCC3V0_PMU | MMA7660FCT | 0x4C | 3-Axis Orientation/Motion Detection Sensor | 100kHz,400kHz |
| | | | | | AK8963C | 0x0E | 3-axis Electronic Compass | 100kHz,400kHz |
| | | | | | GSL1680 | 0x40 | Touch IC | 100kHz,400kHz |
| | | | | | GSL3676 | 0x40 | Touch IC | 100kHz,400kHz |
| | | | | | | | | |
| I2C2 | I2C2_SCL/GPIO2_B7_u<br>I2C2_SDA/GPIO2_C0_u | VCCIO3 | I2C2_SCL_CAM<br>I2C2_SDA_CAM | VCCIO_DVP | OV5695 | 0X36 | MIPI Camera | |
| | | | | | IMX323 | 0X1a | CIF Camera | |

| | | | |
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| Project: | PX30 REF | | |
| File: | 04.I2C MAP | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
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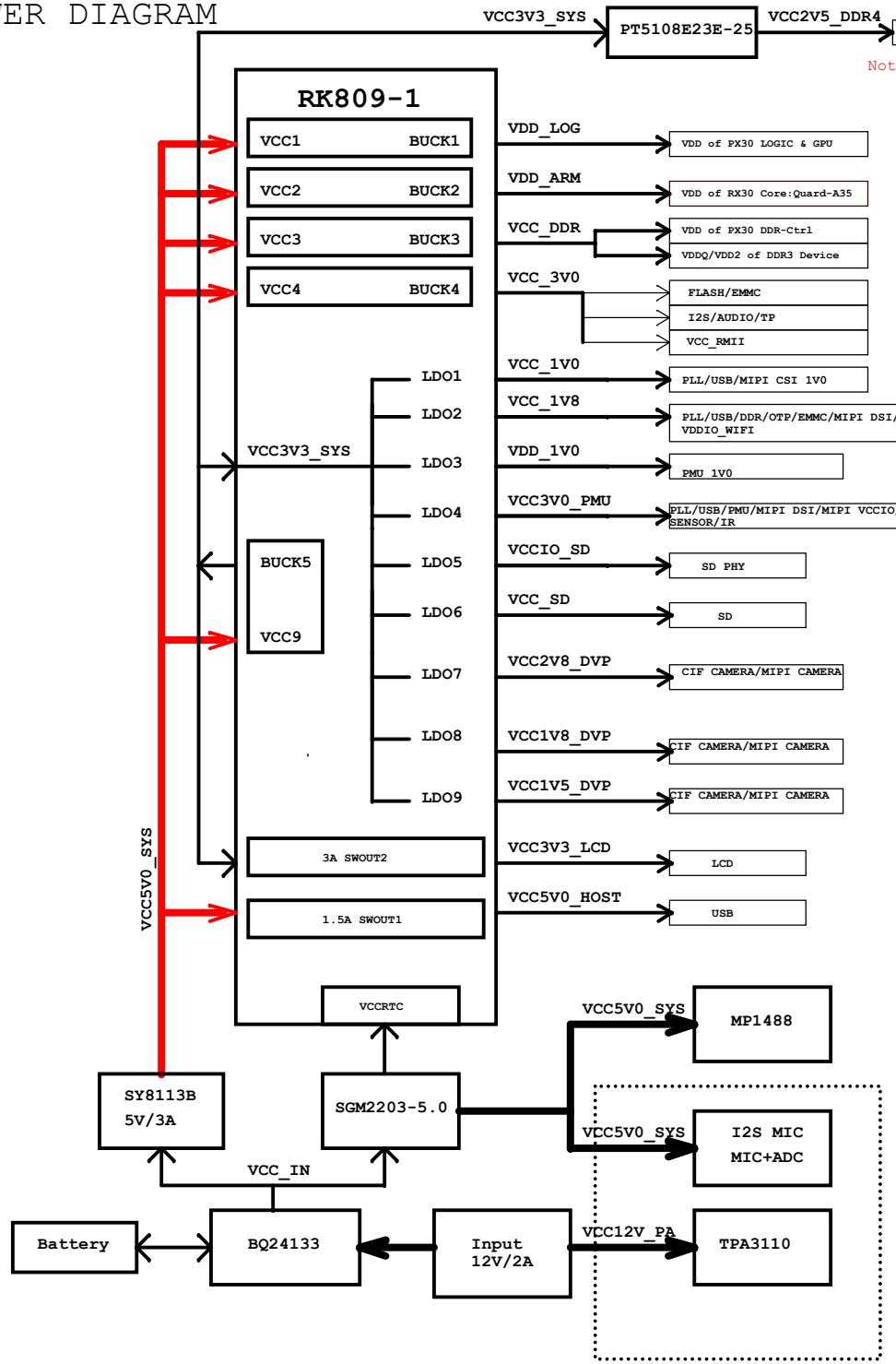
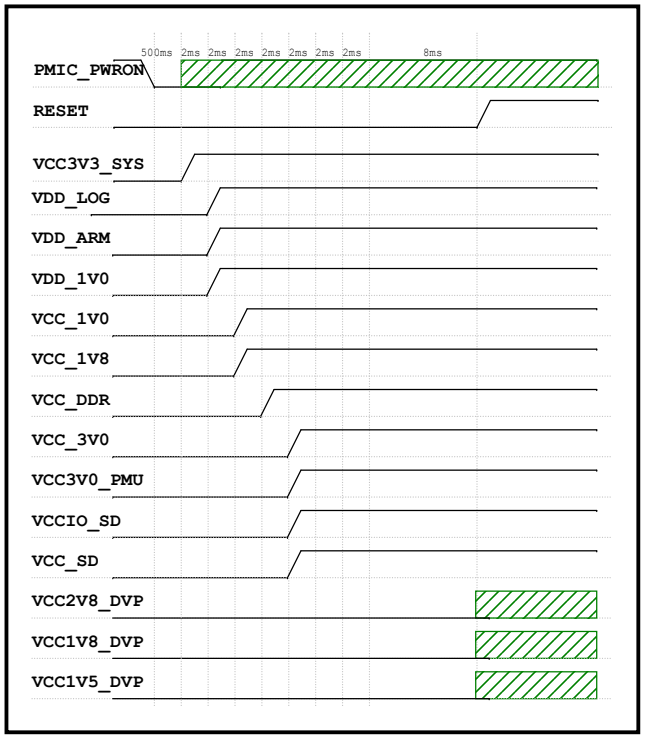
# POWER DIAGRAM




Note:Power parameter shows the Peak value of system consumption.
功耗参数体现的是系统峰值功率

RK809-1 Power-on Sequence

| PowerName | PMIC Channel | Time Slot (step 2mS) | Default voltage | Supply Limit | Default ON/OFF | Sleep ON/OFF | Peak Current |
|---|---|---|---|---|---|---|---|
| VDD_ARM | BUCK1 | Slot:2 | 1.0V | 2.5A | ON | OFF | 1160mA |
| VDD_LOG | BUCK2 | Slot:2 | 1.0V | 2.5A | ON | | 1020mA |
| VCC_DDR | BUCK3 | Slot:4 | FB=0.6V | 1.5A | ON | ON | 790mA |
| VCC_3V0 | BUCK4 | Slot:5 | 3.0V | 1.5A | ON | ON | 360mA |
| VCC3V3_SYS | BUCK5 | Slot:1 | 3.3V | 1.5A | ON | ON | |
| VCC_1V0 | LDO1 | Slot:3 | 2.5V | 500mA | ON | ON | |
| VCC_1V8 | LDO2 | Slot:3 | 1.8V | 500mA | ON | ON | 236mA |
| VDD_1V0 | LDO3 | Slot:2 | 1.0V | 500mA | ON | ON | 13.6mA |
| VCC3V0_PMU | LDO4 | Slot:5 | 3.0V | 100mA | ON | ON | 9mA |
| VCCIO_SD | LDO5 | Slot:5 | 3.0V | 500mA | ON | | |
| VCC_SD | LDO6 | Slot:5 | 3.0V | 500mA | ON | | |
| VCC2V8_DVP | LDO7 | | 2.8V | 500mA | OFF | OFF | |
| VCC1V8_DVP | LDO8 | | 1.8V | 500mA | OFF | OFF | |
| VCC1V5_DVP | LDO9 | | 1.5V | 500mA | OFF | OFF | |
| RESET | RESETB | Slot:11 | OD | | | | |




| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 05.Power diagram and Sequence | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
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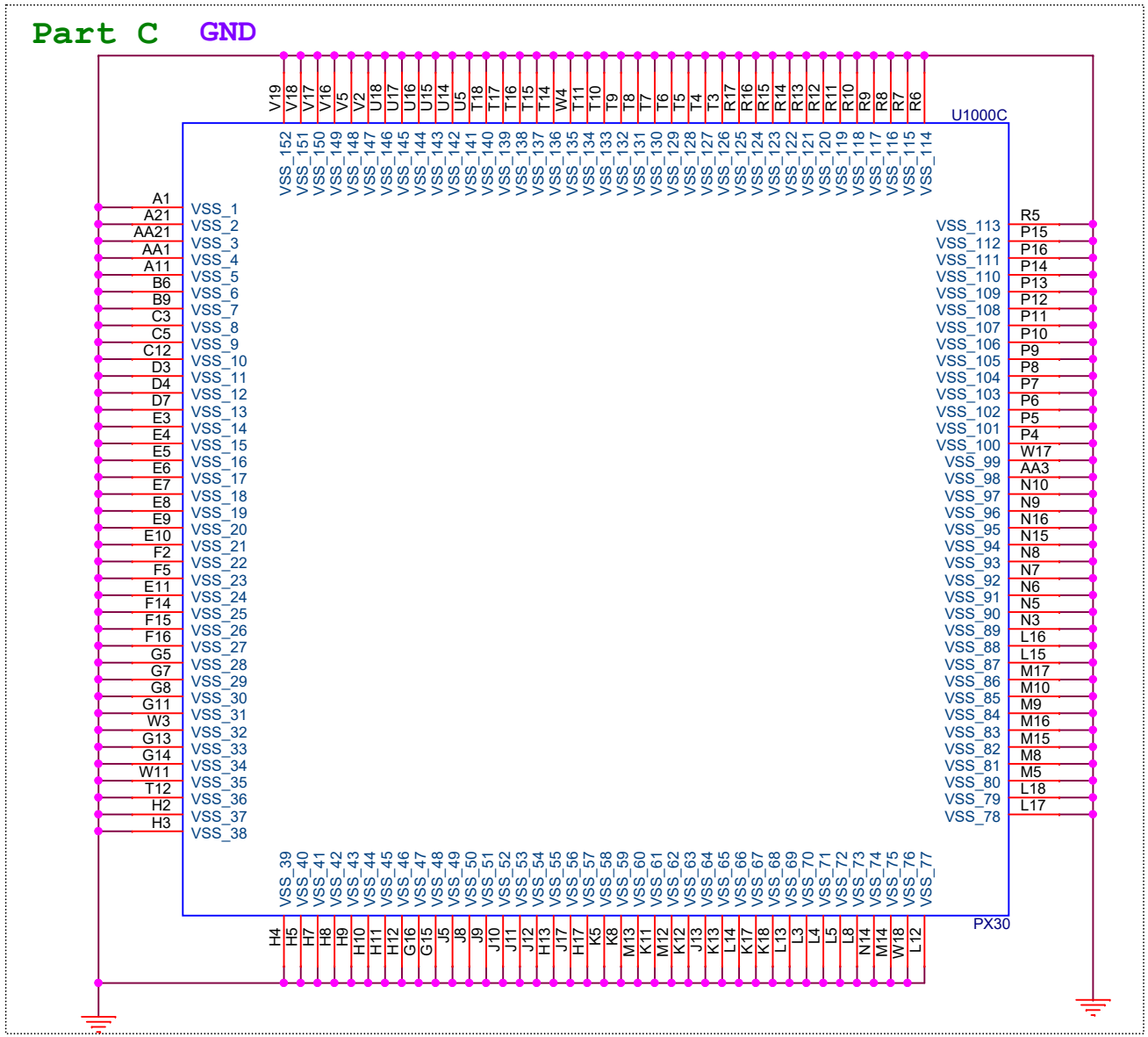


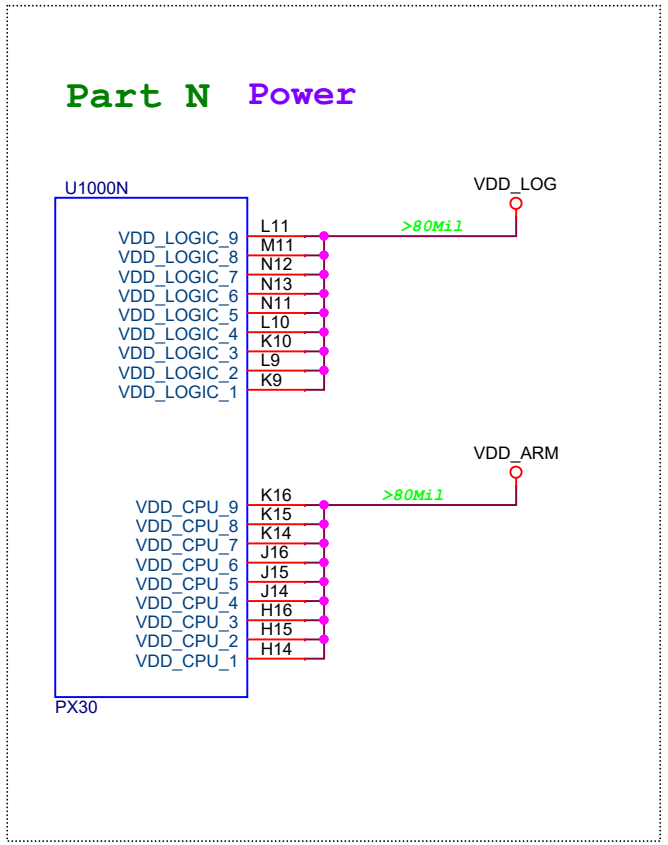


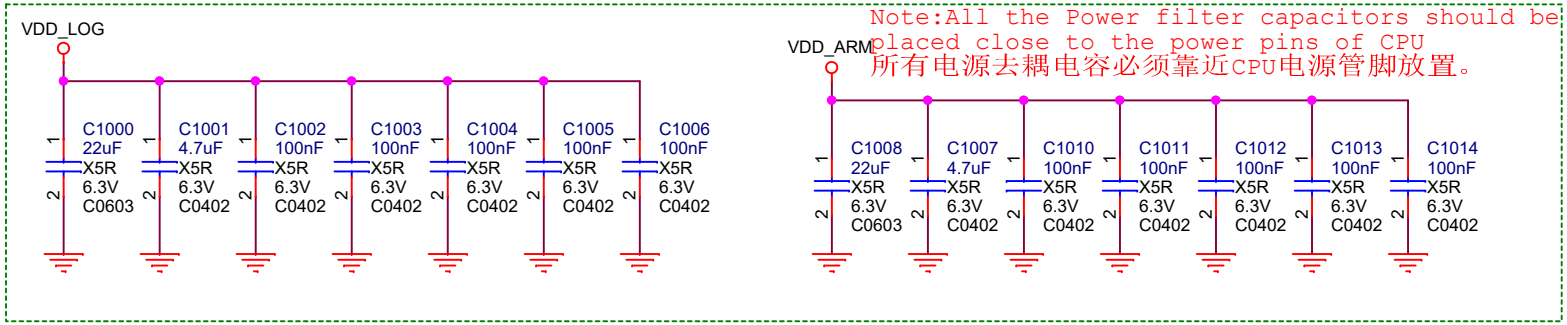


| | |
|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics |
| Project: | PX30 REF |
| File: | 10.PX30 Power |
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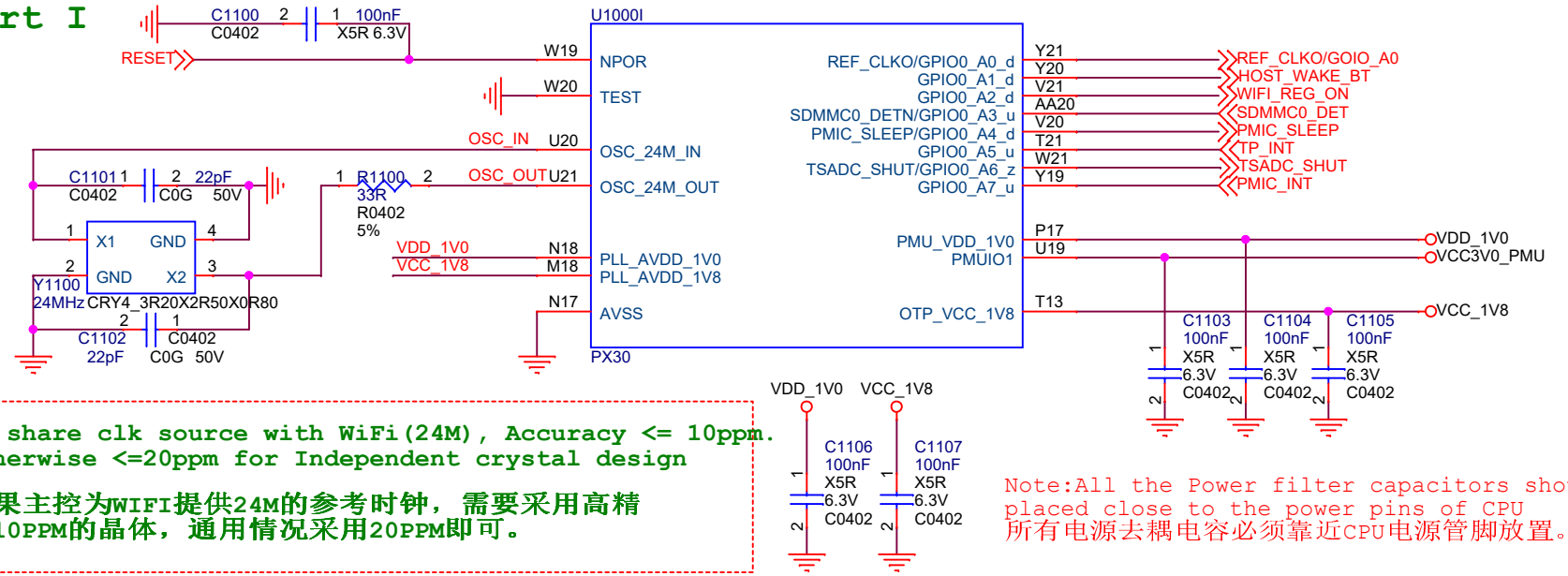
## Part I



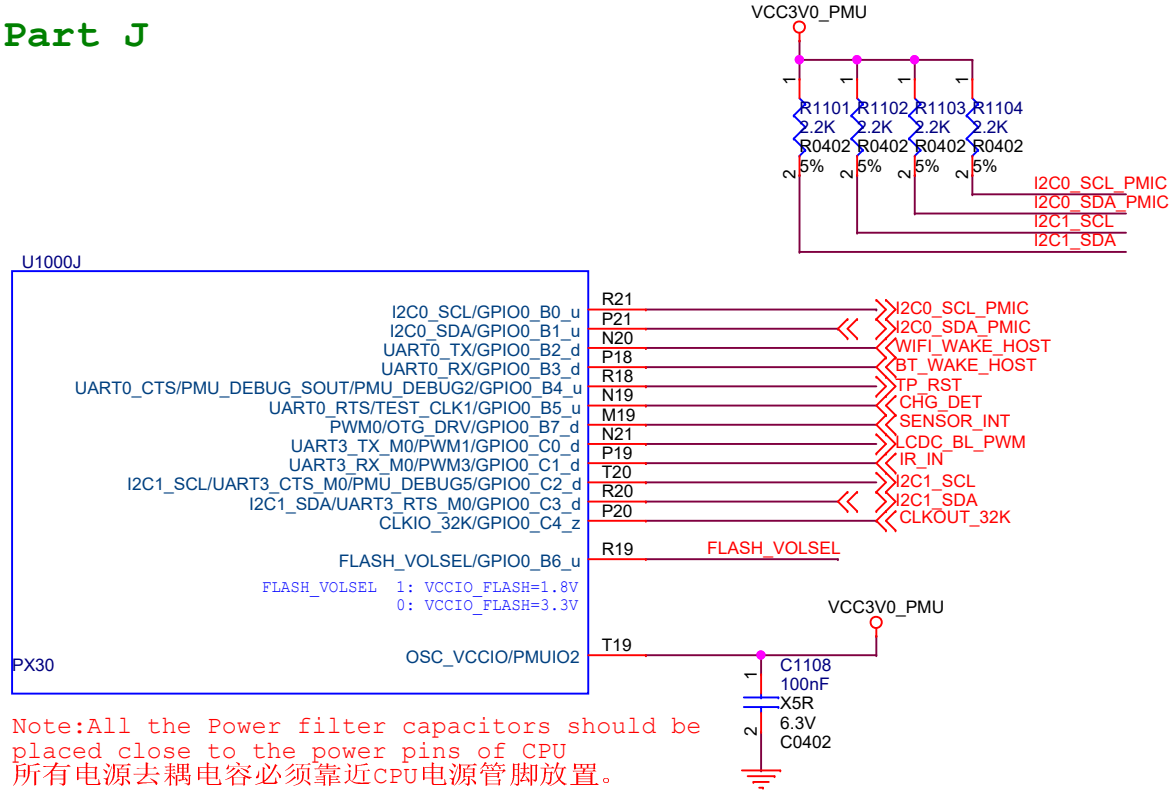

If share clk source with WiFi(24M), Accuracy <= 10ppm.
Otherwise <=20ppm for Independent crystal design

如果主控为WIFI提供24M的参考时钟，需要采用高精度10PPM的晶体，通用情况采用20PPM即可。

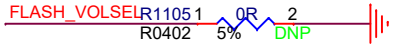



Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

## Part J




Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。




| | |
|---|---|
| Floating or Pull-up<br>FLASH_VOLSEL=1 | Pull-down<br>FLASH_VOLSEL=0 |
| VCCIO_FLASH=1.8V | VCCIO_FLASH=3.3V |

| | | | |
|---|---|---|---|
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| Project: | PX30 REF | | |
| File: | 11.PX30 OSC/PMUIO | | |
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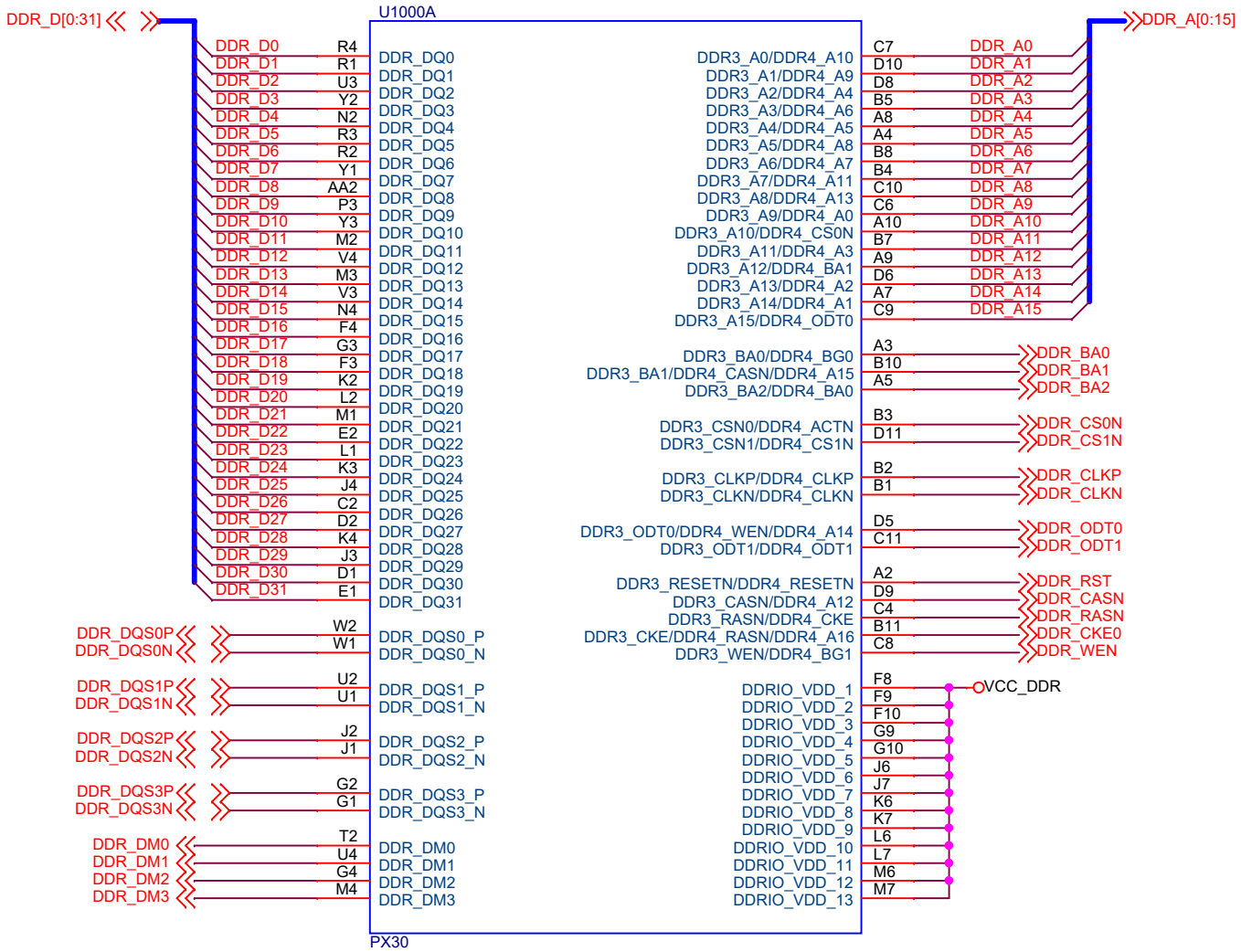
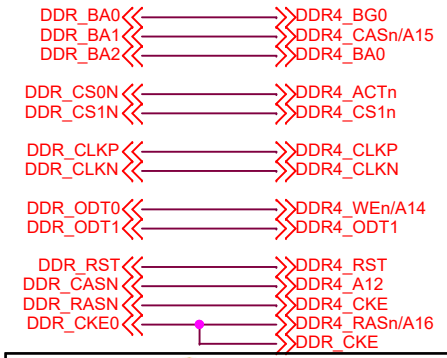
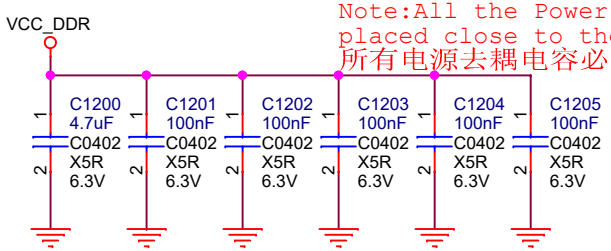
# Part A DDR Controler




## DDR3/DDR4 PIN MUX

| | |
|---|---|
| DDR3_A0 | DDR4_A10 |
| DDR3_A1 | DDR4_A9 |
| DDR3_A2 | DDR4_A4 |
| DDR3_A3 | DDR4_A6 |
| DDR3_A4 | DDR4_A5 |
| DDR3_A5 | DDR4_A8 |
| DDR3_A6 | DDR4_A7 |
| DDR3_A7 | DDR4_A11 |
| DDR3_A8 | DDR4_A13 |
| DDR3_A9 | DDR4_A0 |
| DDR3_A10 | DDR4_CS0n |
| DDR3_A11 | DDR4_A3 |
| DDR3_A12 | DDR4_BA1 |
| DDR3_A13 | DDR4_A2 |
| DDR3_A14 | DDR4_A1 |
| DDR3_A15 | DDR4_ODT0 |
| DDR3_BA0 | DDR4_BG0 |
| DDR3_BA1 | DDR4_CASn/DDR4_A15 |
| DDR3_BA2 | DDR4_BA0 |
| DDR3_CS0N | DDR4_ACTn |
| DDR3_CS1N | DDR4_CS1N |
| DDR3_ODT0 | DDR4_WEn/DDR4_A14 |
| DDR3_ODT1 | DDR4_ODT1 |
| DDR3_CLKP | DDR4_CLKP |
| DDR3_CLKn | DDR4_CLKn |
| DDR3_CKE | DDR4_RASn/DDR4_A16 |
| DDR3_RASn | DDR4_CKE |
| DDR3_CASN | DDR4_A12 |
| DDR3_WEn | DDR4_BG1 |
| DDR3_RST | DDR4_RST |




Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 12.PX30 DDR Controller | | |
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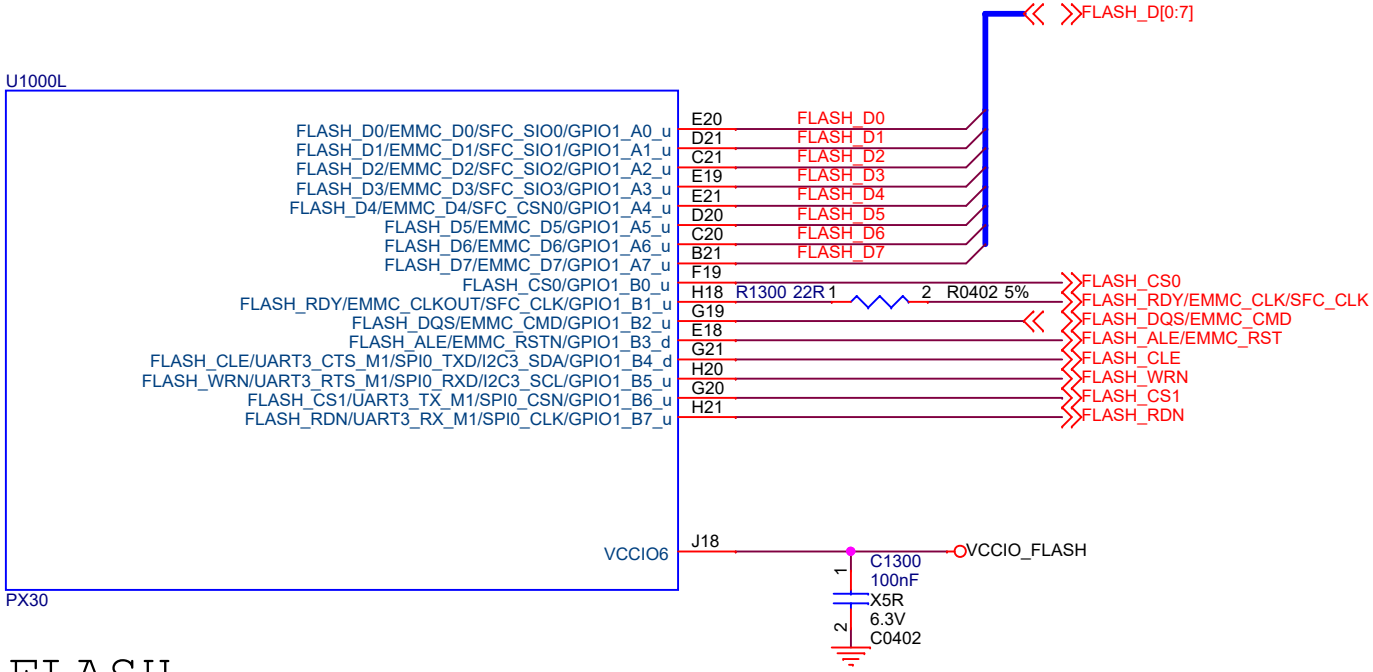
## Part L




# FLASH

Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 13.PX30 Flash Controller | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
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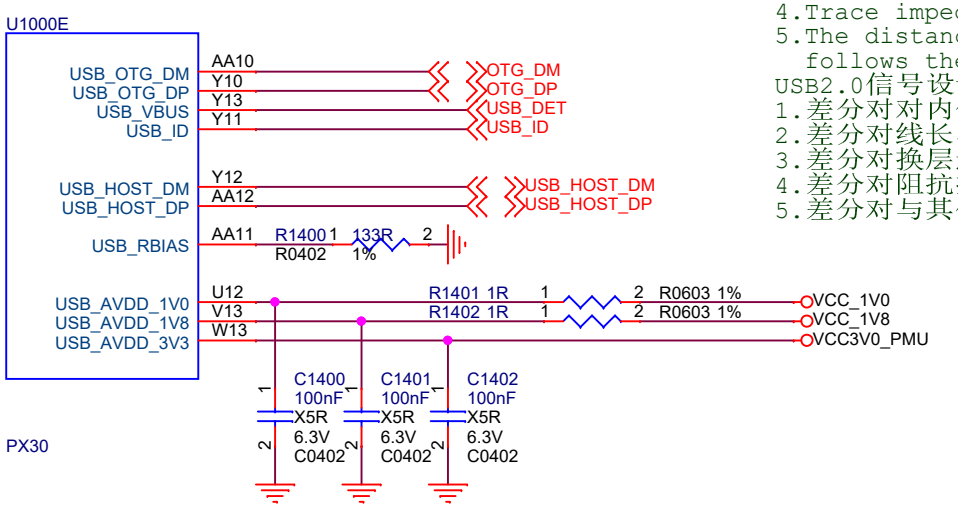
# Part E




Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

USB2.0 design rules:
1.Max intra-pair skew < 4ps;
2.Max trace length < 6inchs;
3.Max allowed via < 6;
4.Trace impedance 90ohm+/-10%;
5.The distance between other signals follows the 3W rule;
USB2.0信号设计规则:
1.差分对对内偏移小于4ps;
2.差分对线长小于6英寸;
3.差分对换层过孔数量少于6个;
4.差分对阻抗控制在90ohm+/-10%;
5.差分对与其他信号的间距遵循3W原则;

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| Project: | PX30 REF | | |
| File: | 14.PX30 USB Controller | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
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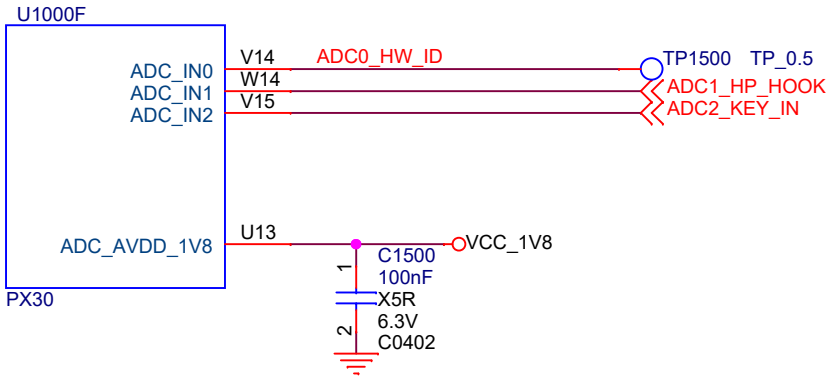
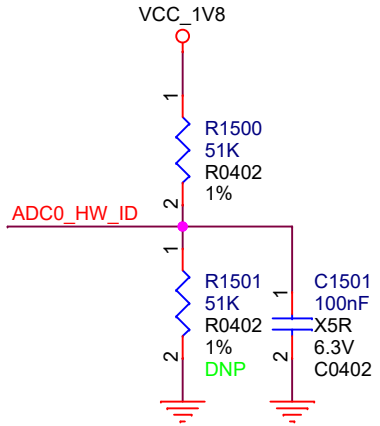
# Part F




Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

It is reserved for the hardware version of the product.
If it is not needed, it can be removed.




## HW ID

| ADC0_HW_ID | Pull-up Resistance | Pull-down Resistance | ADC Value |
|---|---|---|---|
| **Version0 (Default)** | 51K | DNP | 1024 |
| | | | |
| | | | |
| | | | |
| | | | |

| | | | |
|---|---|---|---|
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| **Project:** | **PX30 REF** | | |
| **File:** | **15.PX30 ADC** | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
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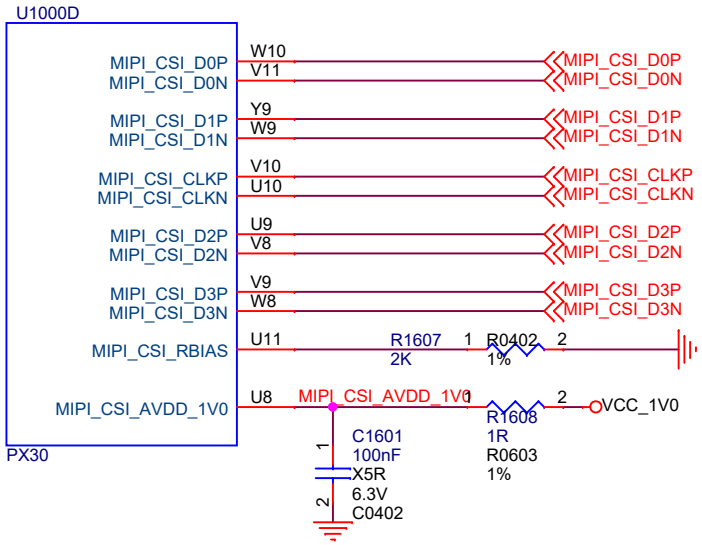
## Part D

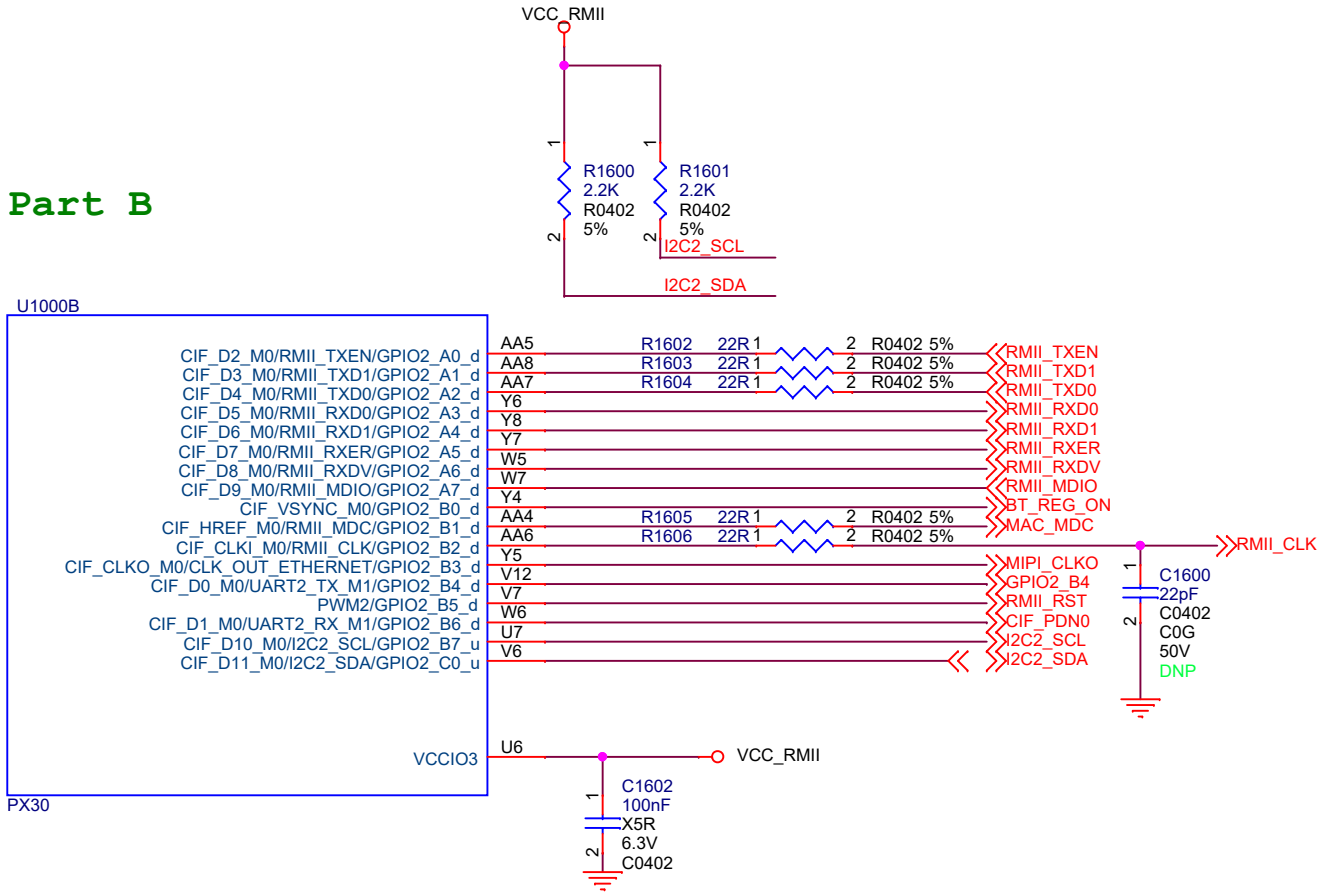



Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

# MIPI CSI

MIPI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;
MIPI信号设计规则:
1.差分对对内偏移小于4ps;
2.Clk与Data的差分对组间偏移小于7ps;
3.差分对线长小于7.2英寸;
4.差分对换层过孔数量少于4个;
5.差分对阻抗控制在100ohm+/-10%;
6.差分对与其他信号的间距遵循3W原则;

## Part B




# CIF/RMII

Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 16.PX30 DVP Interface | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
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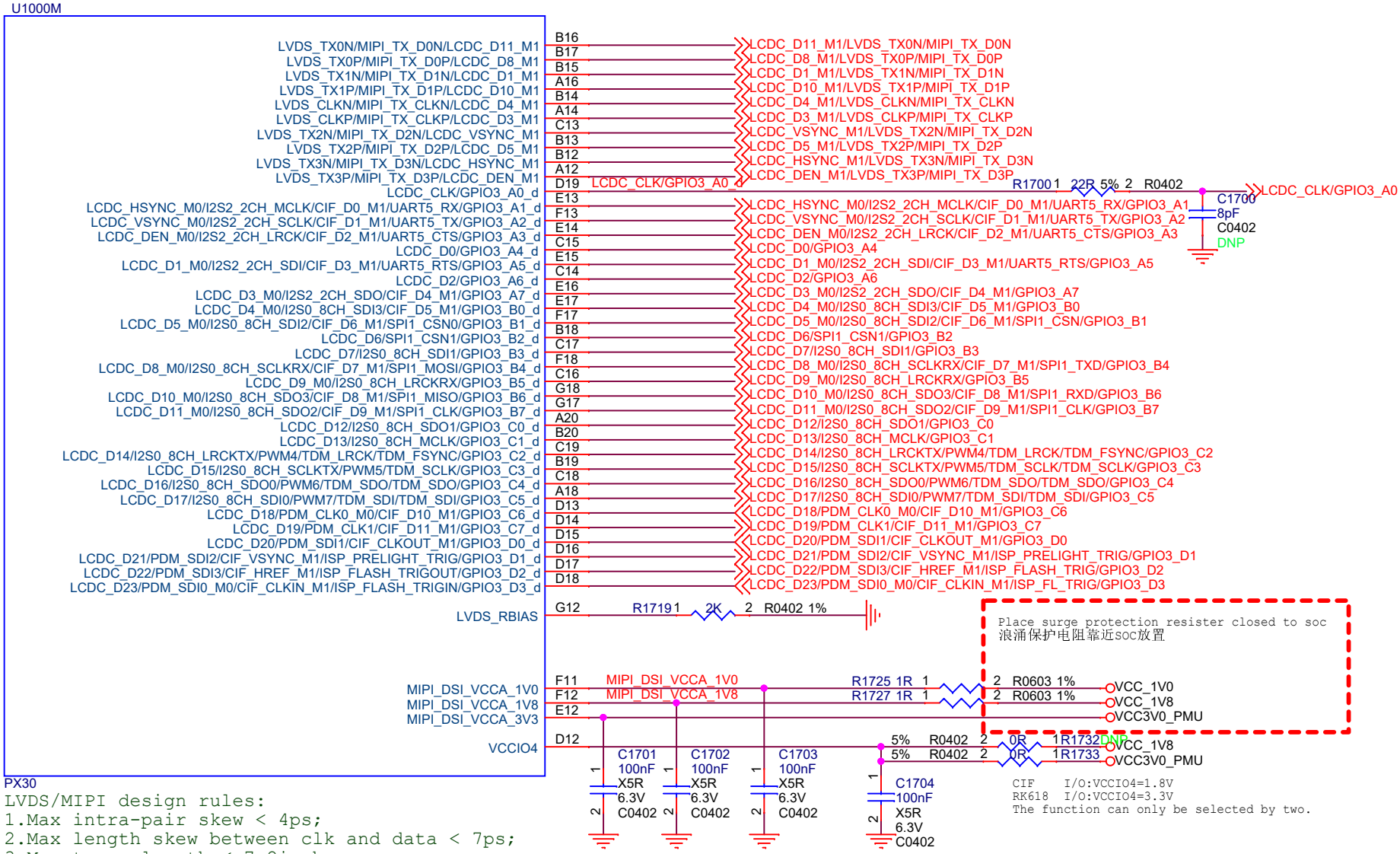
# Part M




Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

LVDS/MIPI design rules:
1.Max intra-pair skew < 4ps;
2.Max length skew between clk and data < 7ps;
3.Max trace length < 7.2inchs;
4.Max allowed via < 4;
5.Trace impedance 100ohm+/-10%;
6.The distance between other signals follows the 3W rule;

MIPI信号设计规则:
1.差分对对内偏移小于4ps;
2.Clk与Data的差分对组间偏移小于7ps;
3.差分对线长小于7.2英寸;
4.差分对换层过孔数量少于4个;
5.差分对阻抗控制在100ohm+/-10%;
6.差分对与其他信号的间距遵循3W原则;

| | | | |
|---|---|---|---|
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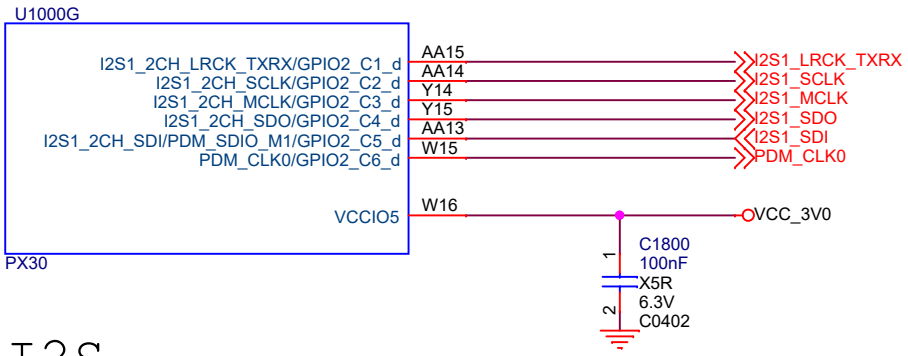
| Project: | PX30 REF | | |
| File: | 17.PX30 MIPI DSI/LCDC | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 14 of 44 |

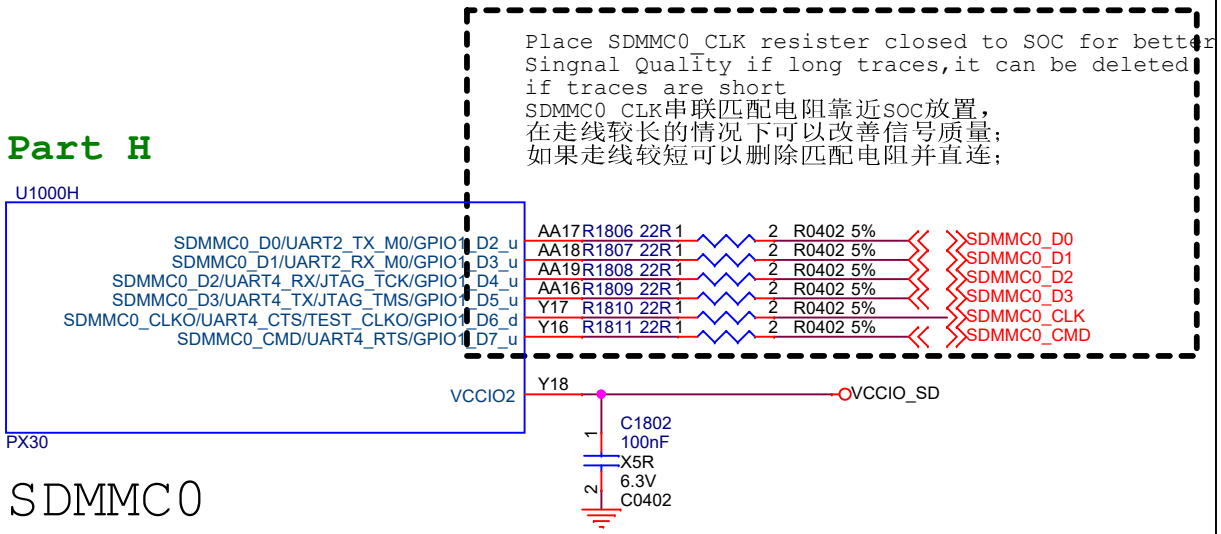
## Part G




I2S

Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

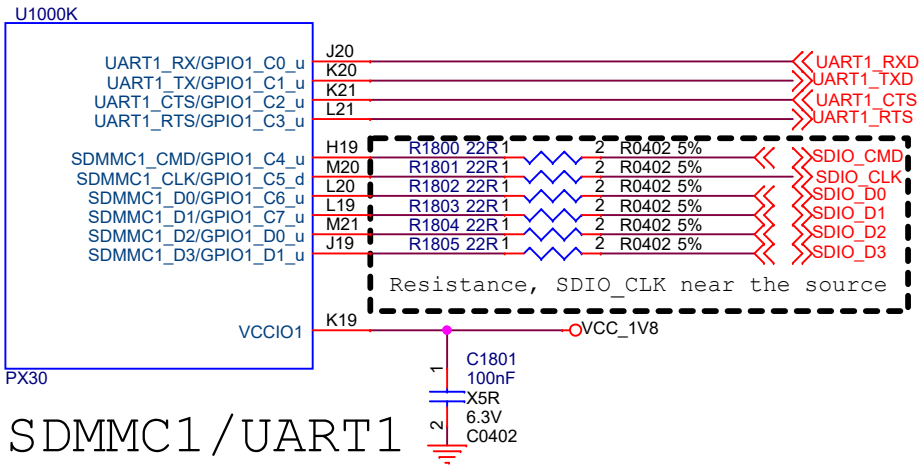
## Part H




SDMMC0

Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

## Part K

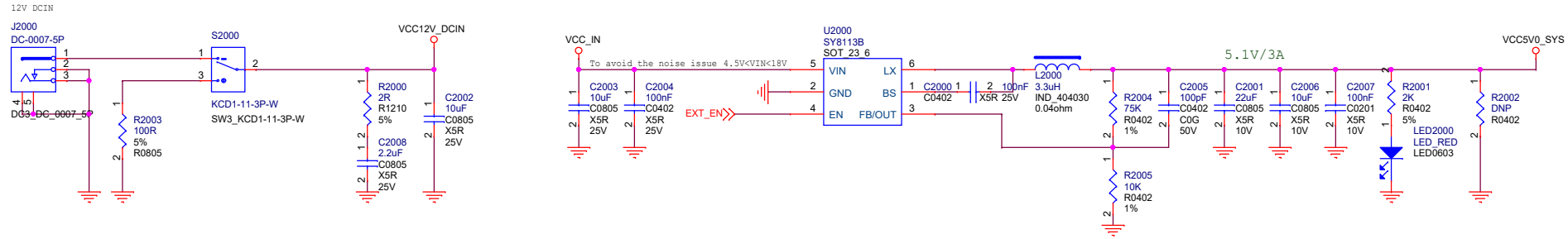


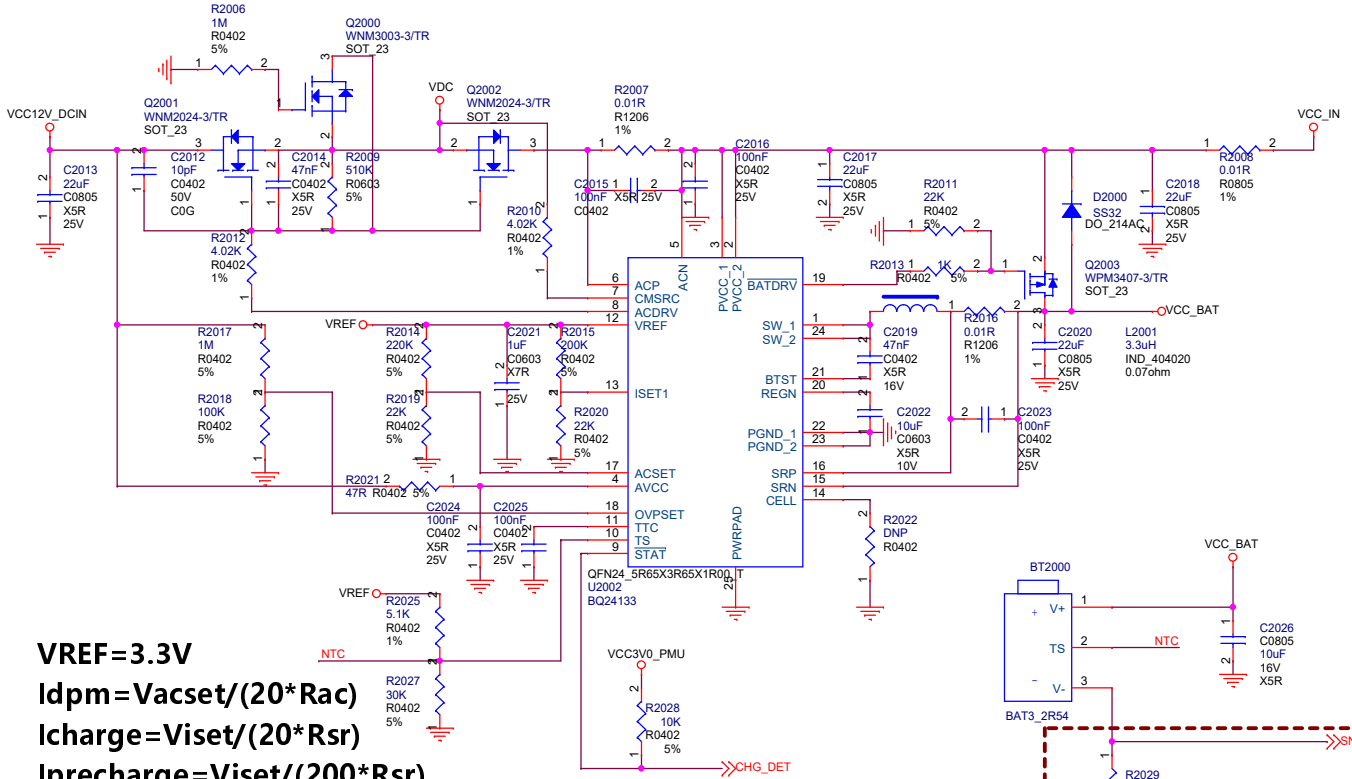

SDMMC1/UART1

Note:All the Power filter capacitors should be placed close to the power pins of CPU
所有电源去耦电容必须靠近CPU电源管脚放置。

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 18.PX30 I2S/SDMMC0/SDMMC1 | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 15 of 44 |

# DC IN&SYSTEM Power




**VREF=3.3V**

**Idpm=Vacset/(20*Rac)**

**Icharge=Viset/(20*Rsr)**

**Iprecharge=Viset/(200*Rsr)**

**Iterm=Viset/(200*Rsr)**

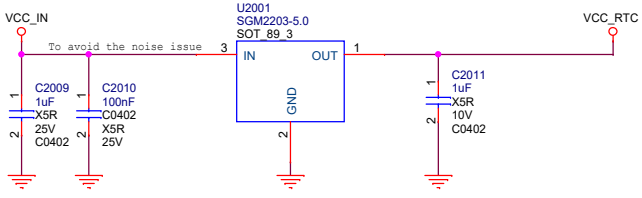
**Tttc=Cttc*Kttc(Kttc=5.6min/nF)**

**If Vovpset above 1.6V or below 0.5V,charge is disabled.**

Close to BAT

0ohm resister closed to pin2 of 0.01R resister , and both of them closed to Battery.

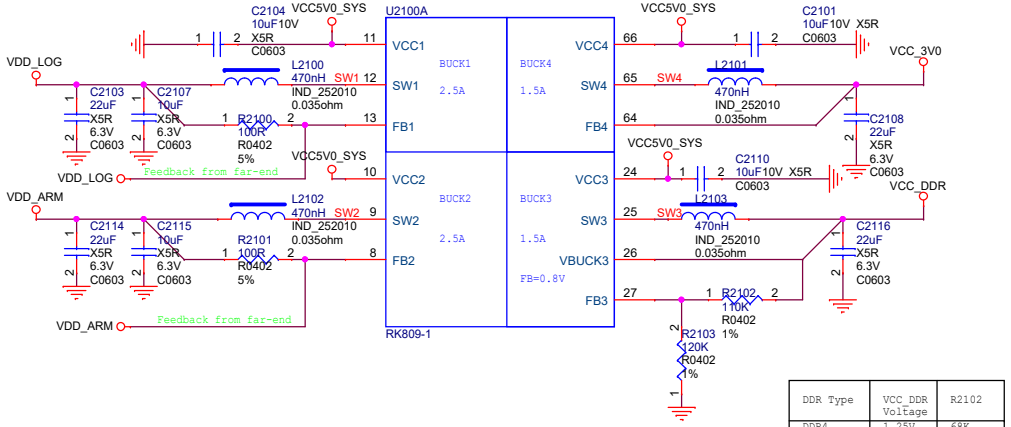
1.6-MHz Synchronous Switched-Mode Li-Ion and Li-Polymer Stand-Alone Battery Charger




LDO-VCCRTC

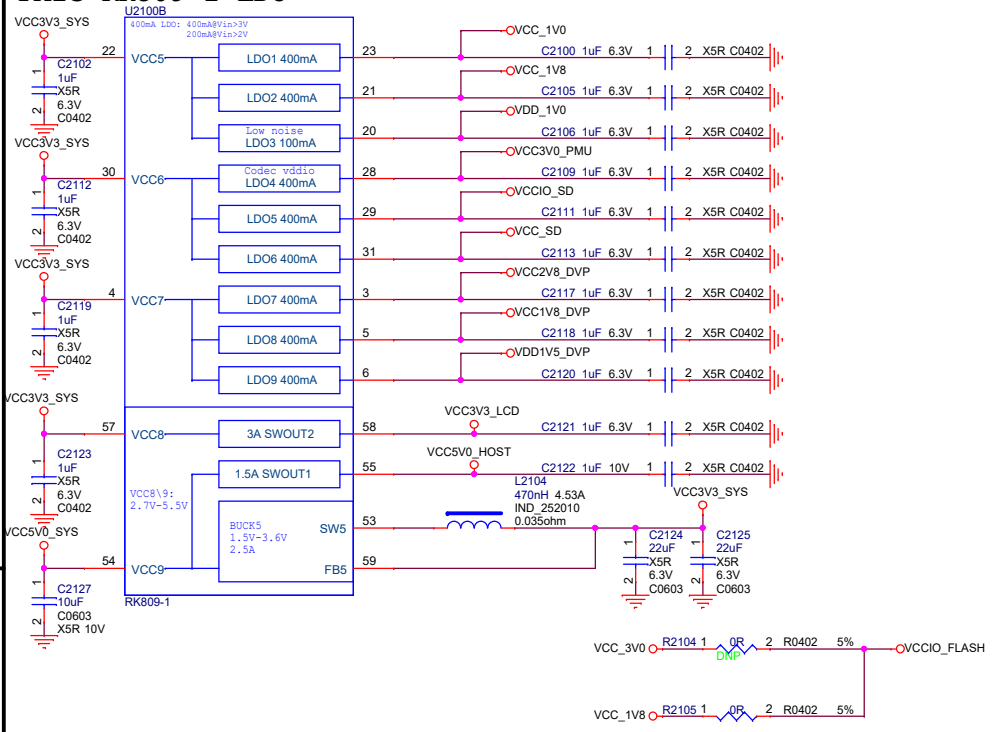
| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 20.Power-DC IN | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 16 of 44 |

# PMIC RK809-1 DCDC

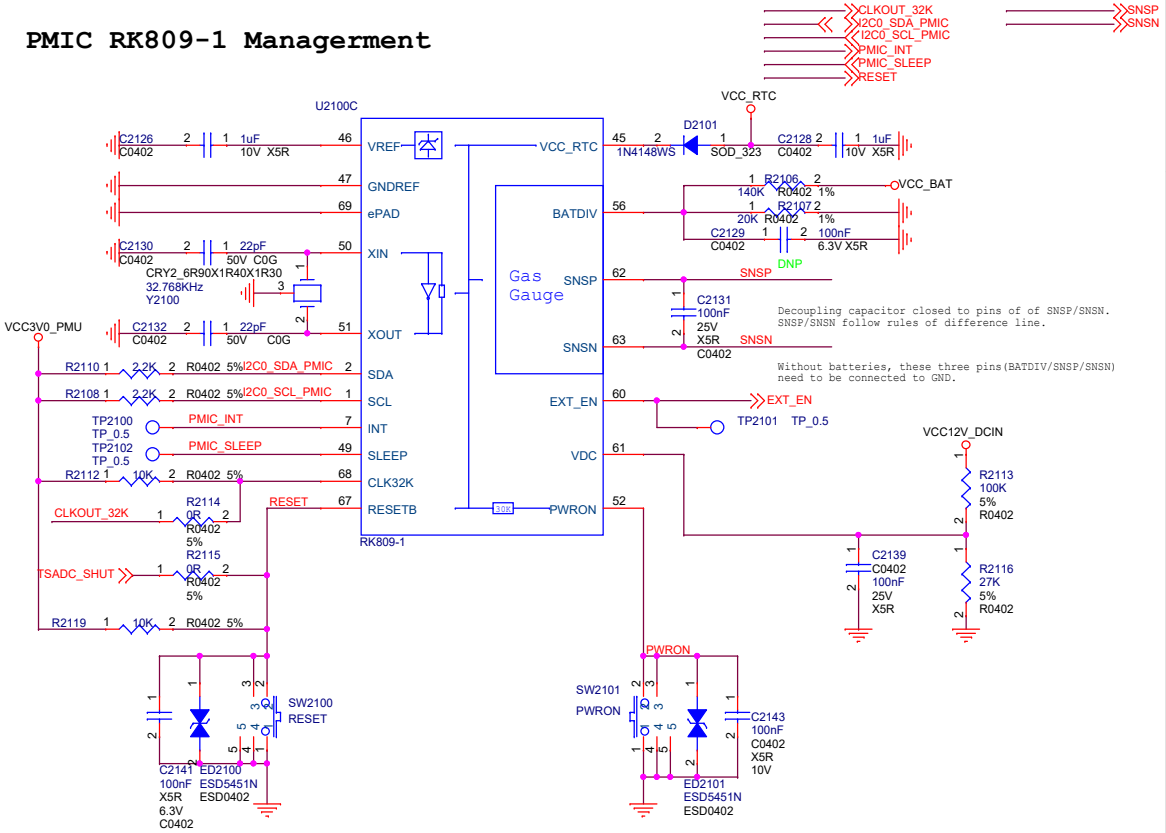



| DDR Type | VCC_DDR Voltage | R2102 |
|---|---|---|
| DDR4 | 1.25V | 68K |
| LPDDR3 | 1.25V | 68K |
| DDR3L | 1.35V | 82K |
| DDR3 | 1.53V | 110K |

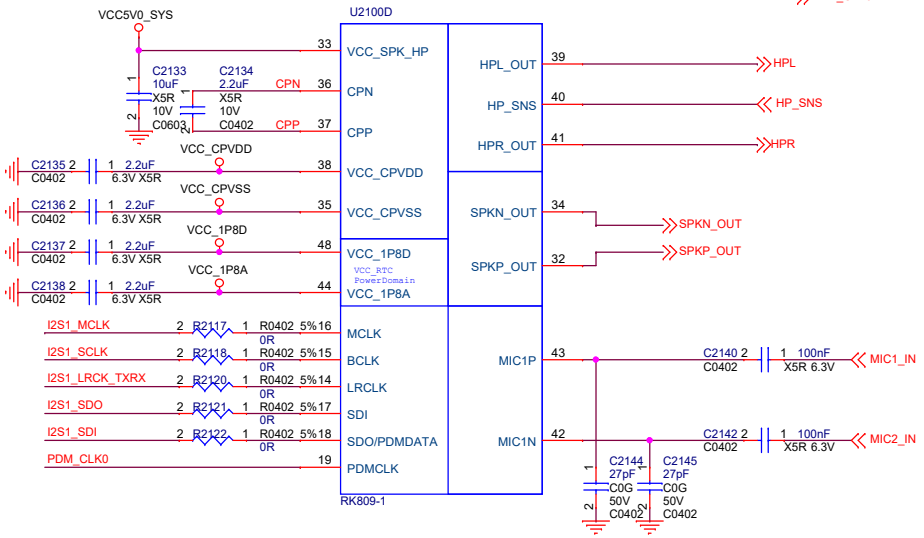
# PMIC RK809-1 LDO




# PMIC RK809-1 Managerment

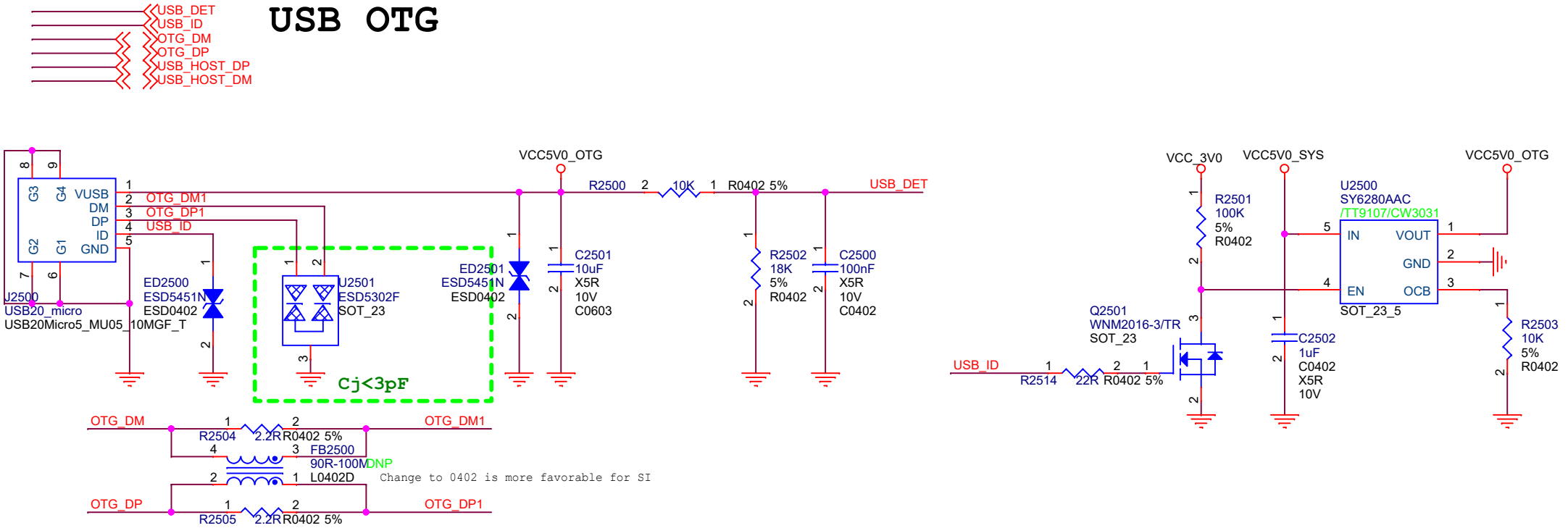



# PMIC RK809-1 CODEC

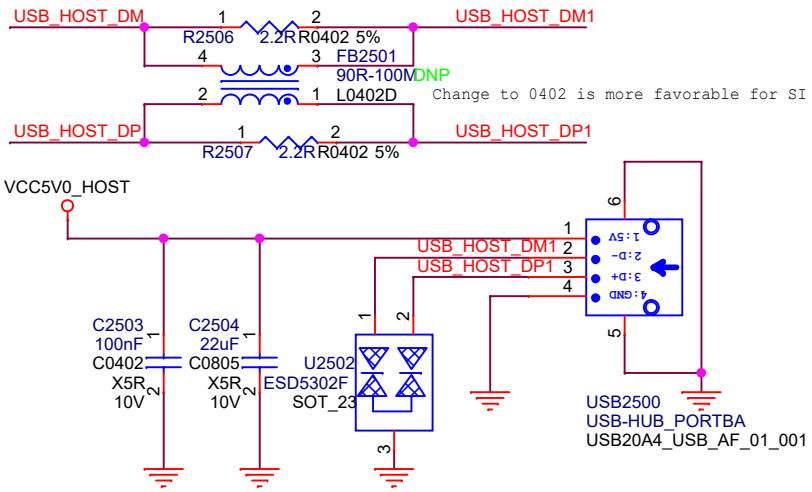



| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 21:Power-PMIC RK809-1 | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 17 of 44 |

# USB OTG



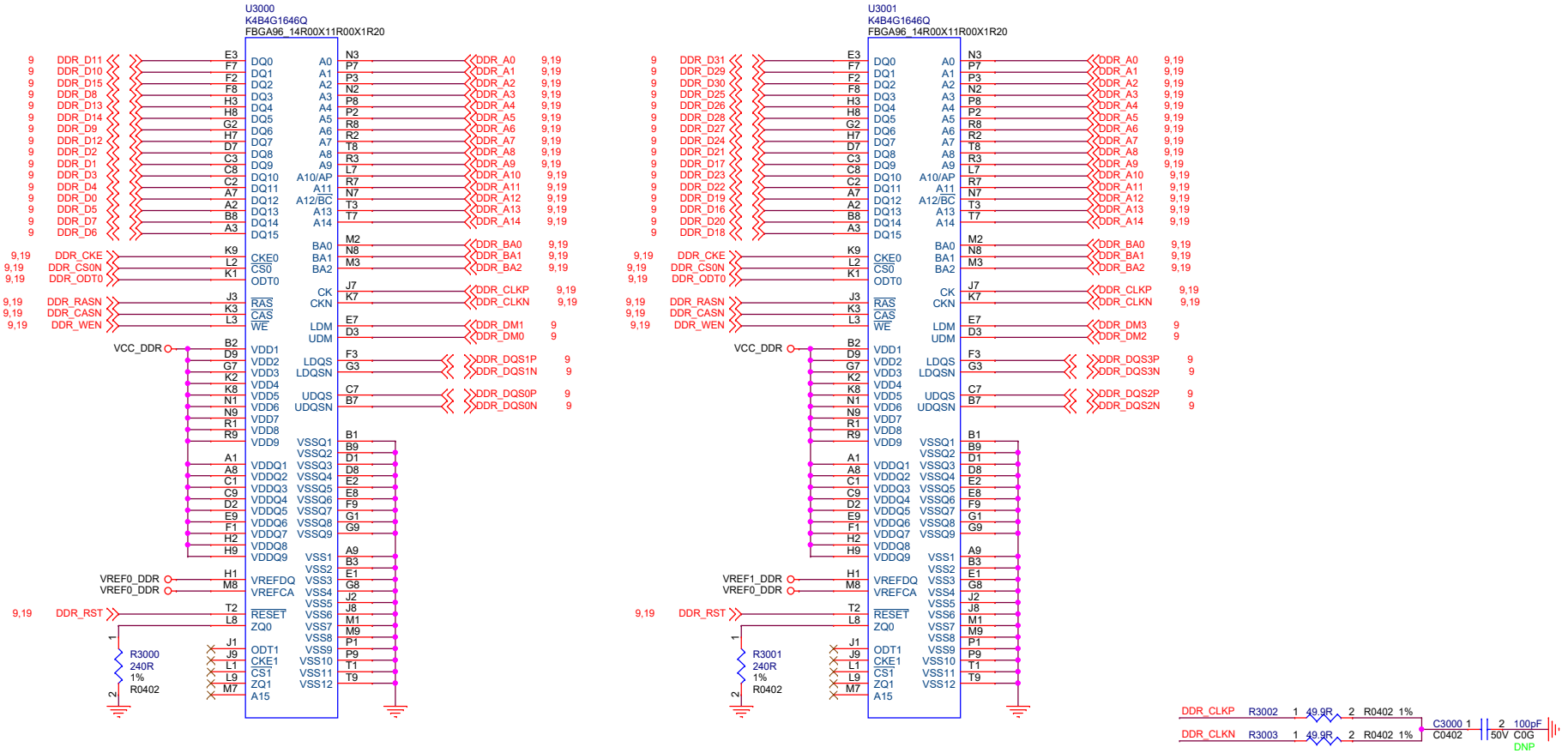

# USB HOST



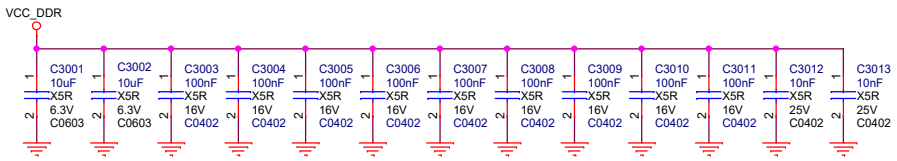

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 25.USB OTG/HOST | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 18 of 44 |

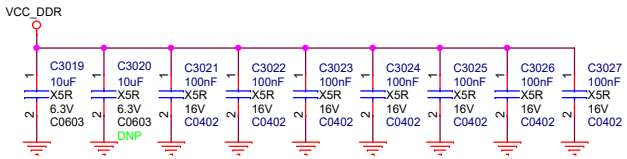
# DDR3/DDR3L 2x16bit

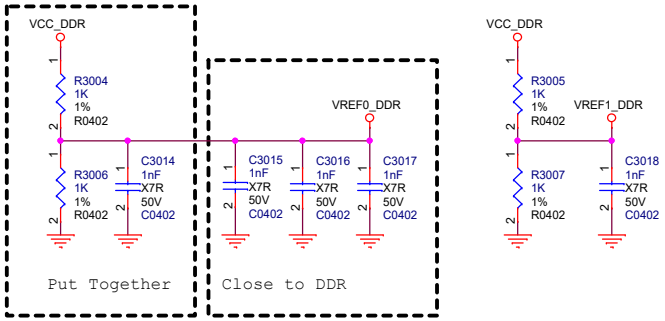
**Remind: Refer to the latest AVL for parts selection.**




Note:All the Power filter capacitors should be placed close to the power pins of DDR3



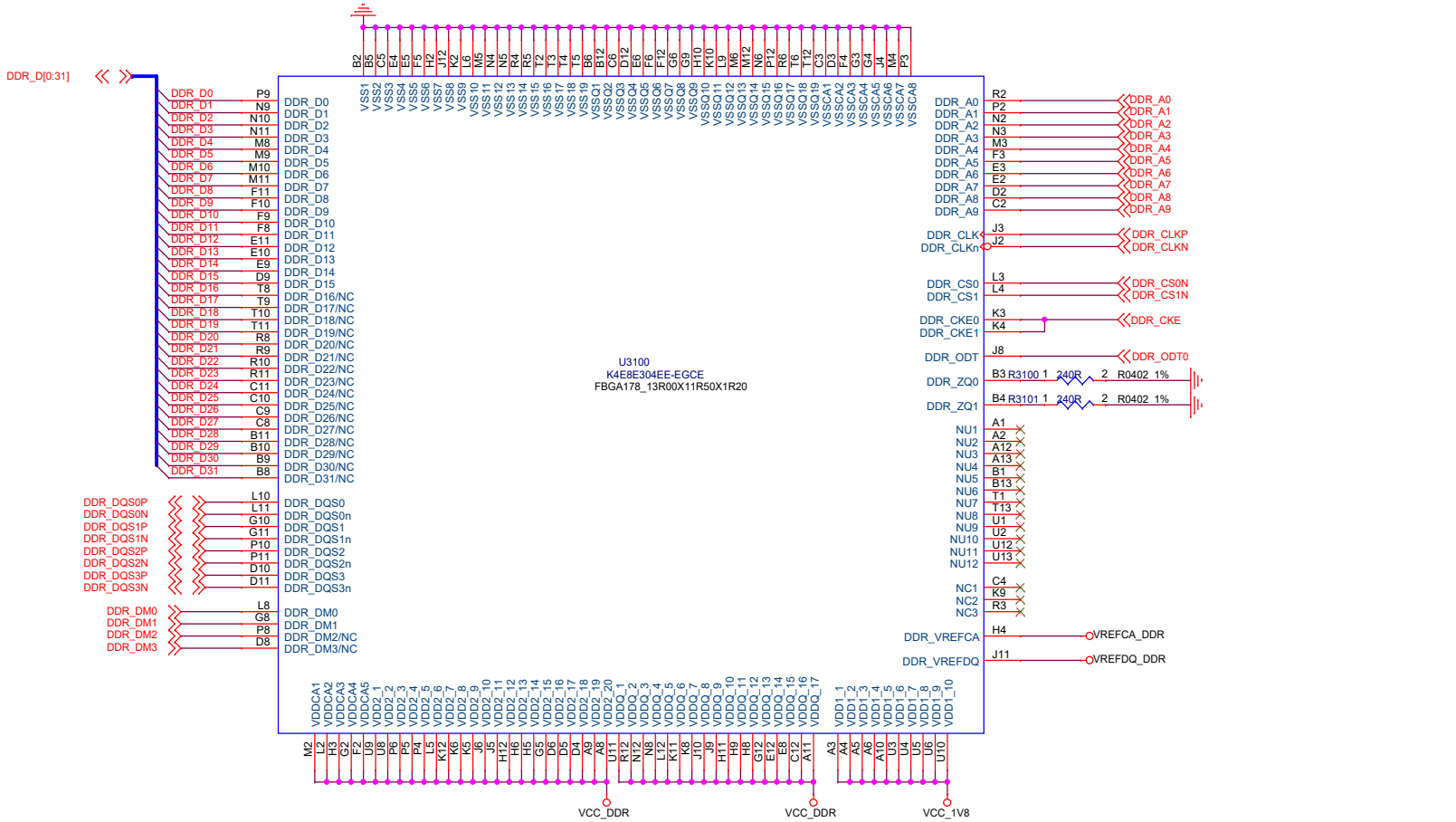



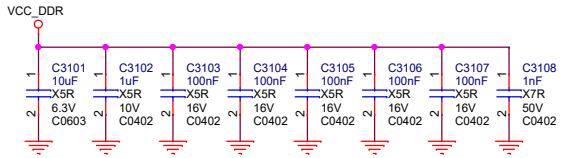



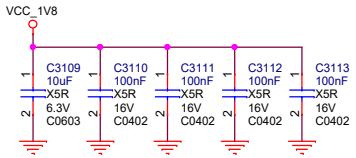

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 30.RAM DDR3 2x16bit(option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 19 of 44 |

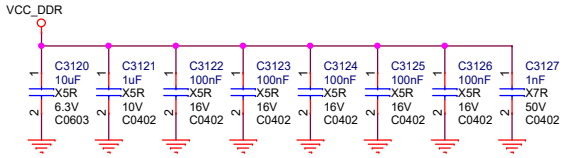
# LPDDR3 1x32bit

Remind: Refer to the latest AVL for parts selection.

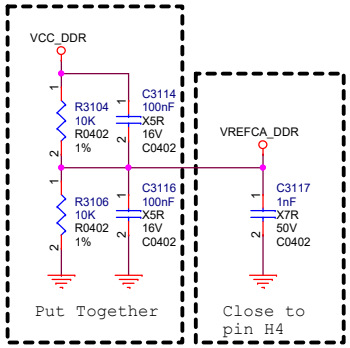


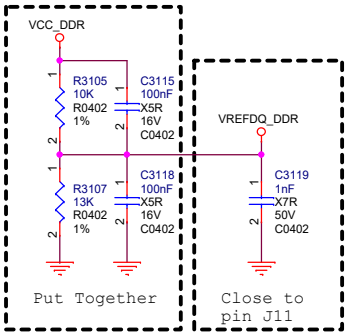




Note:All the power filter capacitors should be placed close to the power pins of LPDDR3



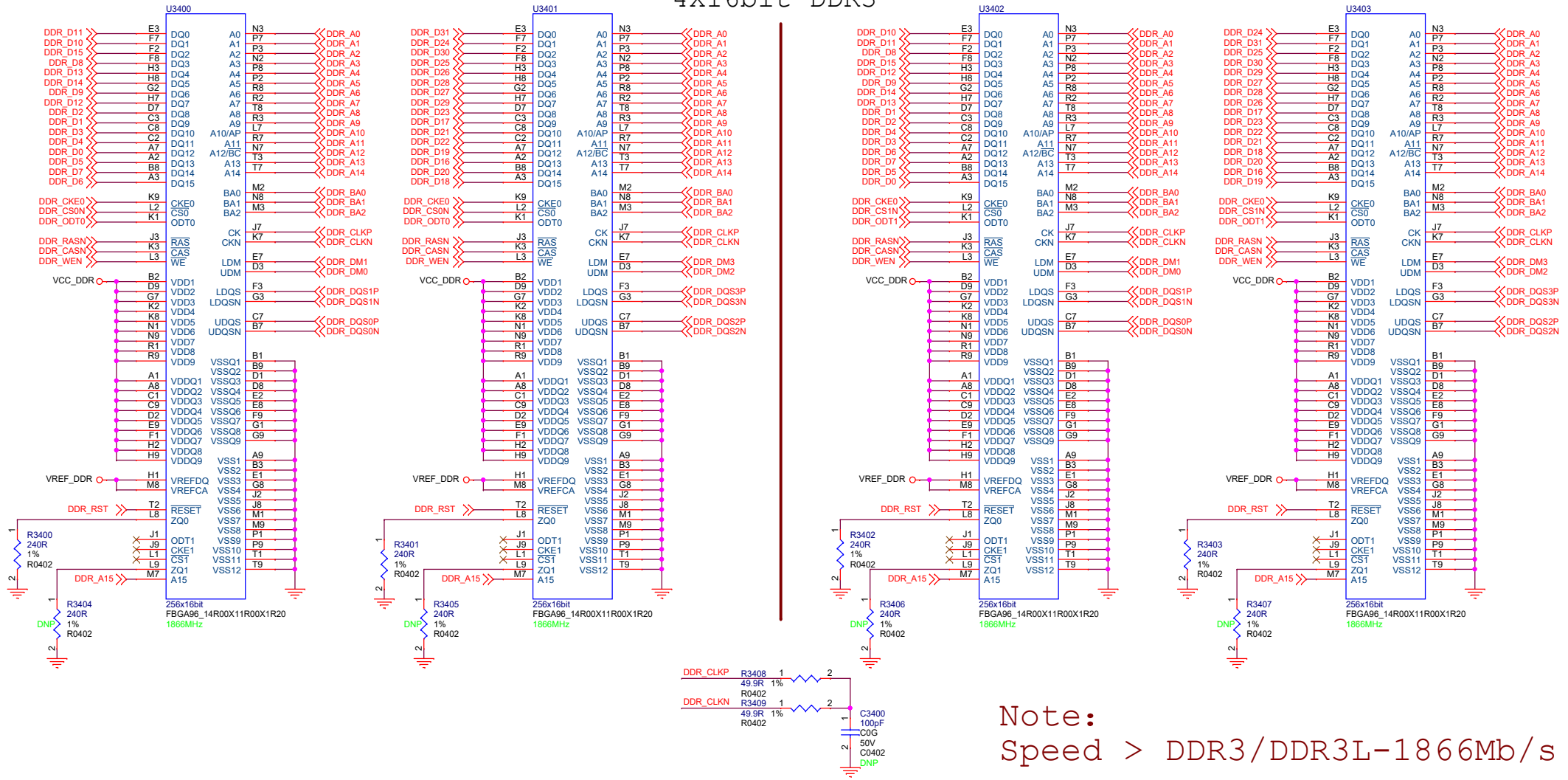




**Note:**
**Vih=VCC**
**Vil=VCC*Ron/(Ron+Rodt)**
**VREFDQ_DDR=(Vih+Vil)/2**

**eg:VCC=1.2V,Ron=34ohm,Rodt=240ohm**
**so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V**

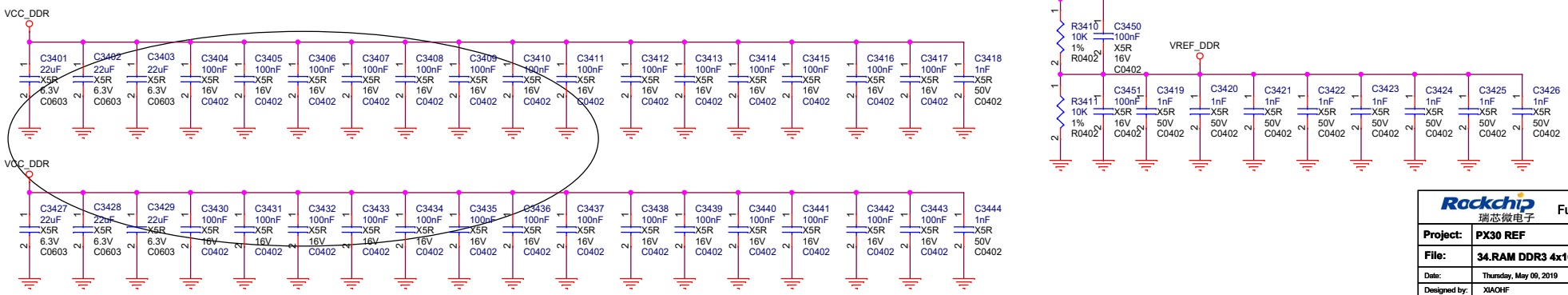
| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 31.RAM-LPDDR3 1x32bit(option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 20 of 44 |

# 4X16bit DDR3

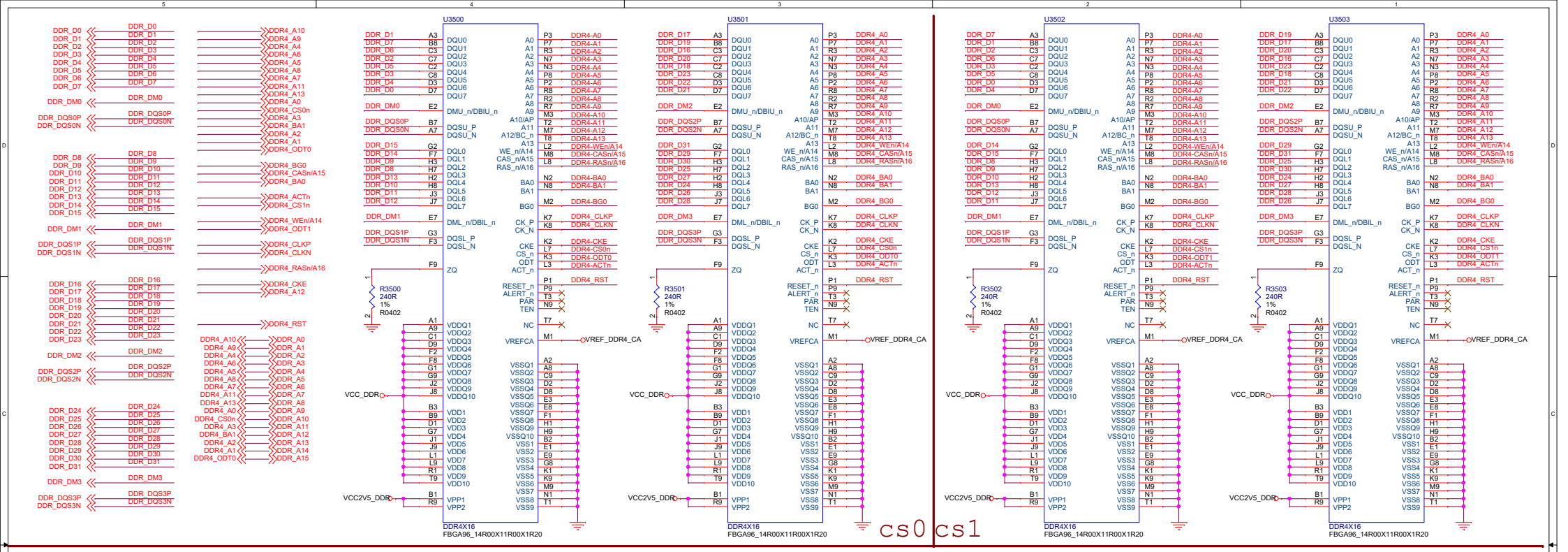



Note:
Speed > DDR3/DDR3L-1866Mb/s

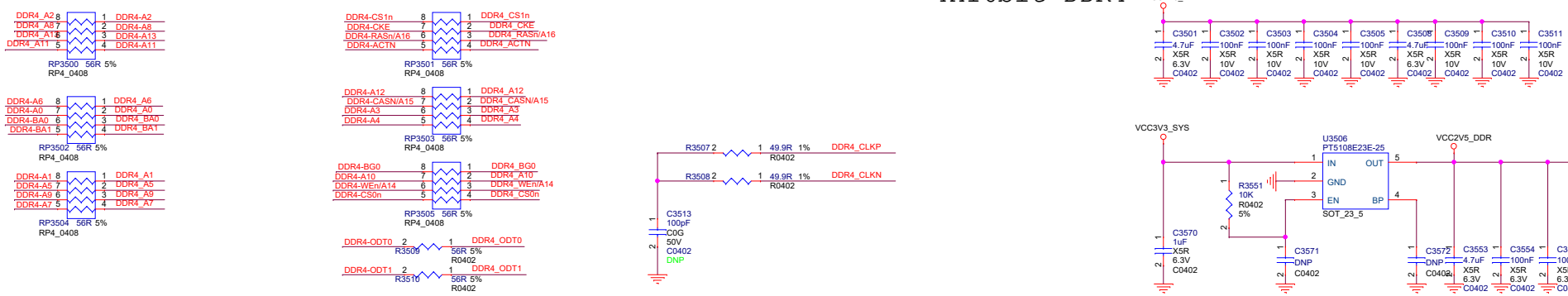
## DDR3 FILTER



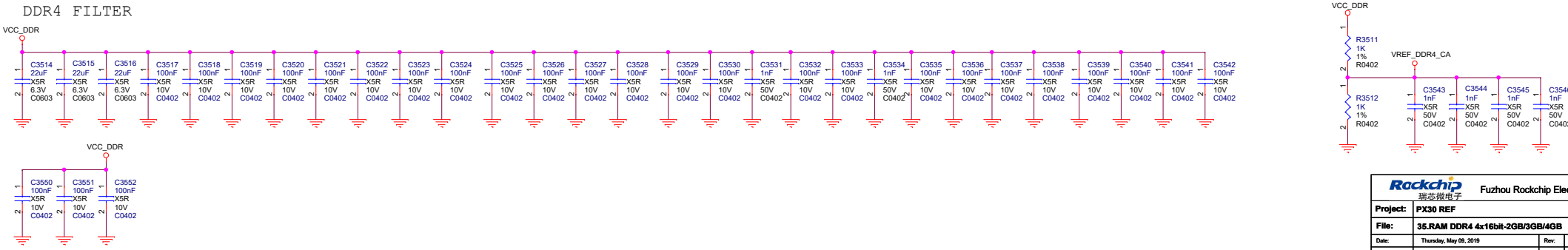

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 34.RAM DDR3 4x16bit(option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 21 of 44 |




## 4X16bit DDR4




## DDR4 FILTER



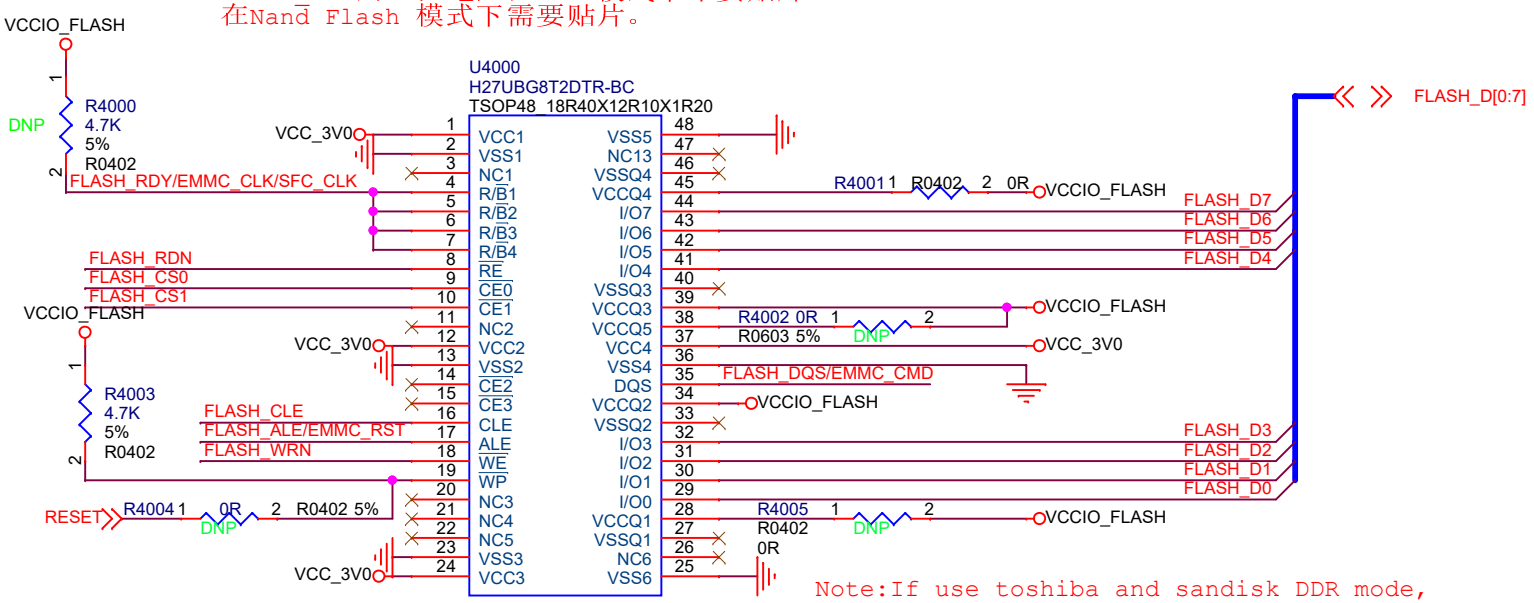

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 35.RAM DDR4 4x16bit-2GB/3GB/4GB | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIACHF | Sheet: | 22 of 44 |

# Nand Flash

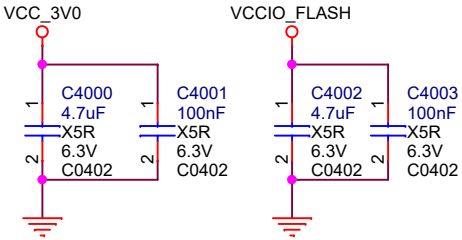
**Remind: Refer to the latest AVL for parts selection.**

FLASH_RDN
FLASH_RDY/EMMC_CLK/SFC_CLK
FLASH_WRN
FLASH_CLE
FLASH_ALE/EMMC_RST
FLASH_DQS/EMMC_CMD
FLASH_CS0
FLASH_CS1

Note:Flash_RDY pull-up resister must
be deleted in eMMC Flash mode and
be mounted in Nand Flash mode.
Flash_RDY的上拉电阻在eMMC模式下不要贴片，
在Nand Flash 模式下需要贴片。




Note:If use toshiba and sandisk DDR mode,
VCCQ1 and VCCQ4 must be connected to VCC_IO。
如果使用Toshiba或者Sandisk颗粒的DDR模式，
VCCQ1和VCCQ2需要连接到电源VCC_IO.

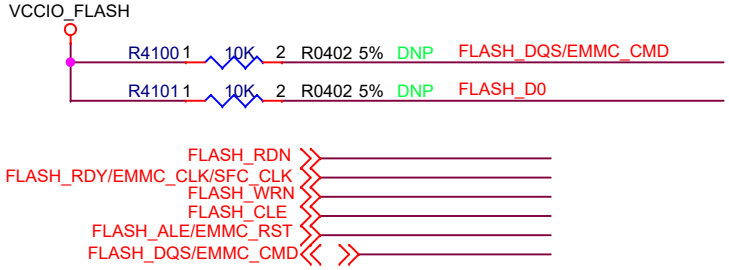


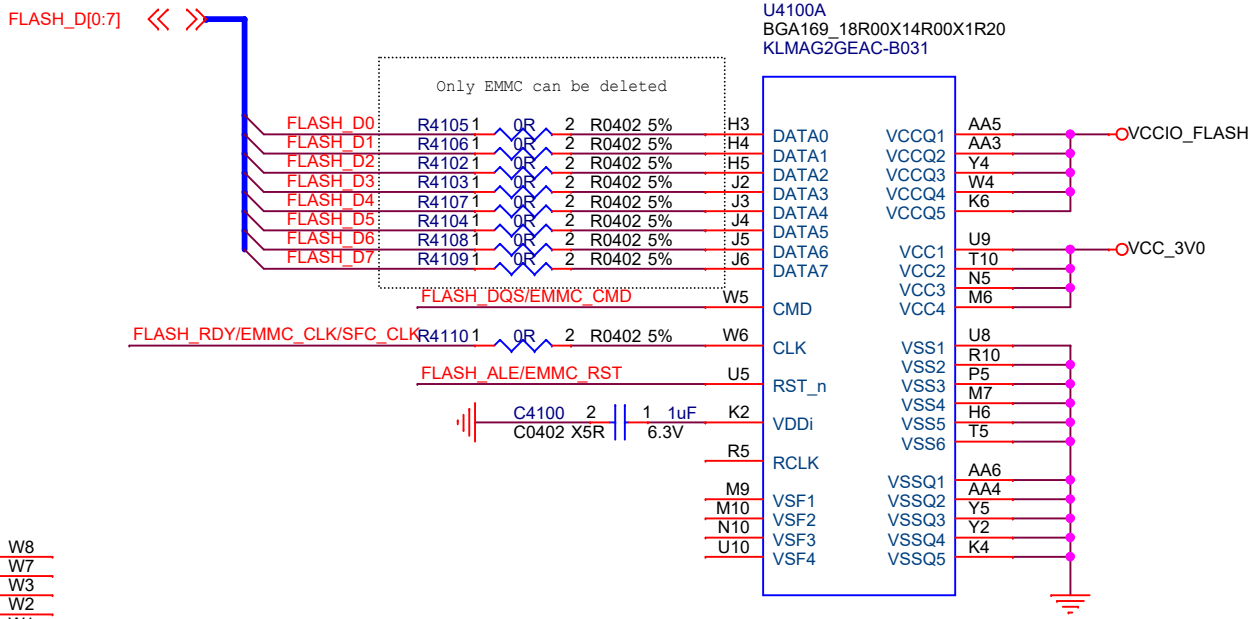

Note:All the Power filter capacitors should be
placed close to the power pins of Nand Flash
所有电源去耦电容必须靠近Nand Flash电源管脚放置。

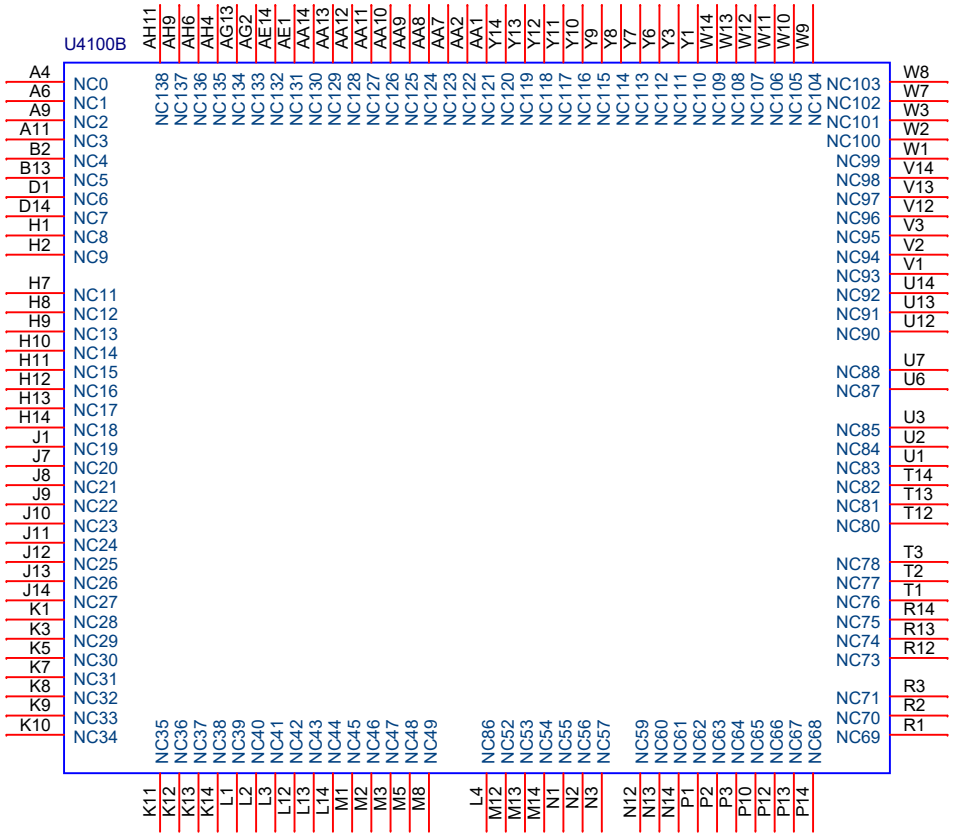

Note:
Reserve TestPoint for firmware update.
If FLASH_D0=0V at power-on reset,
then system will enter into Maskrom mode.
预留用于固件升级的测试点，上电复位情况下如果
FLASH_D0为低电平，系统会进入Maskrom模式。

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 40.Flash-Nand Flash(option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 23 of 44 |

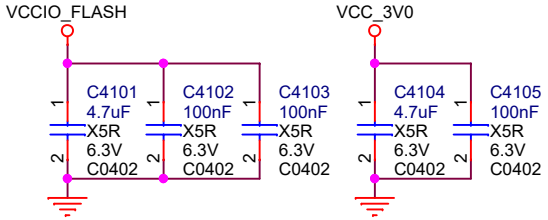
# eMMC

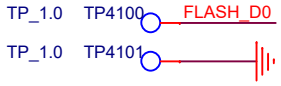



KLMAG2GEAC-B031
BGA169_18R00X14R00X1R20



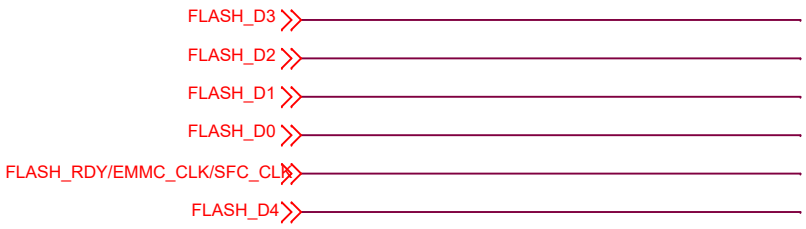

Note:
Short two TP points to Enter Maskrom Mode.

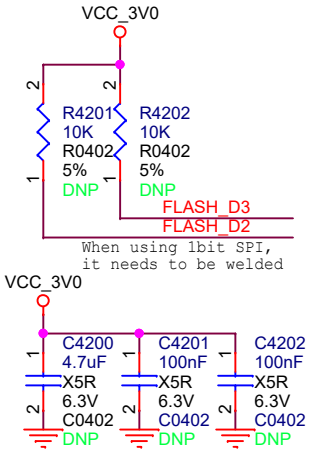
Remind: Refer to the latest AVL for parts selection.

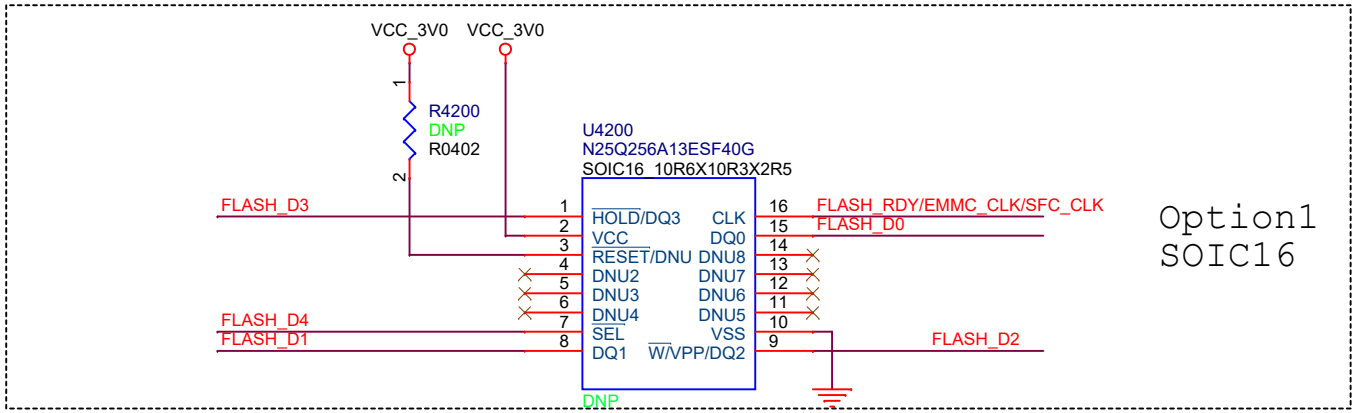
| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 41.Flash-EMMC | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 24 of 44 |

# SPI Flash

Reserved for minimal system.



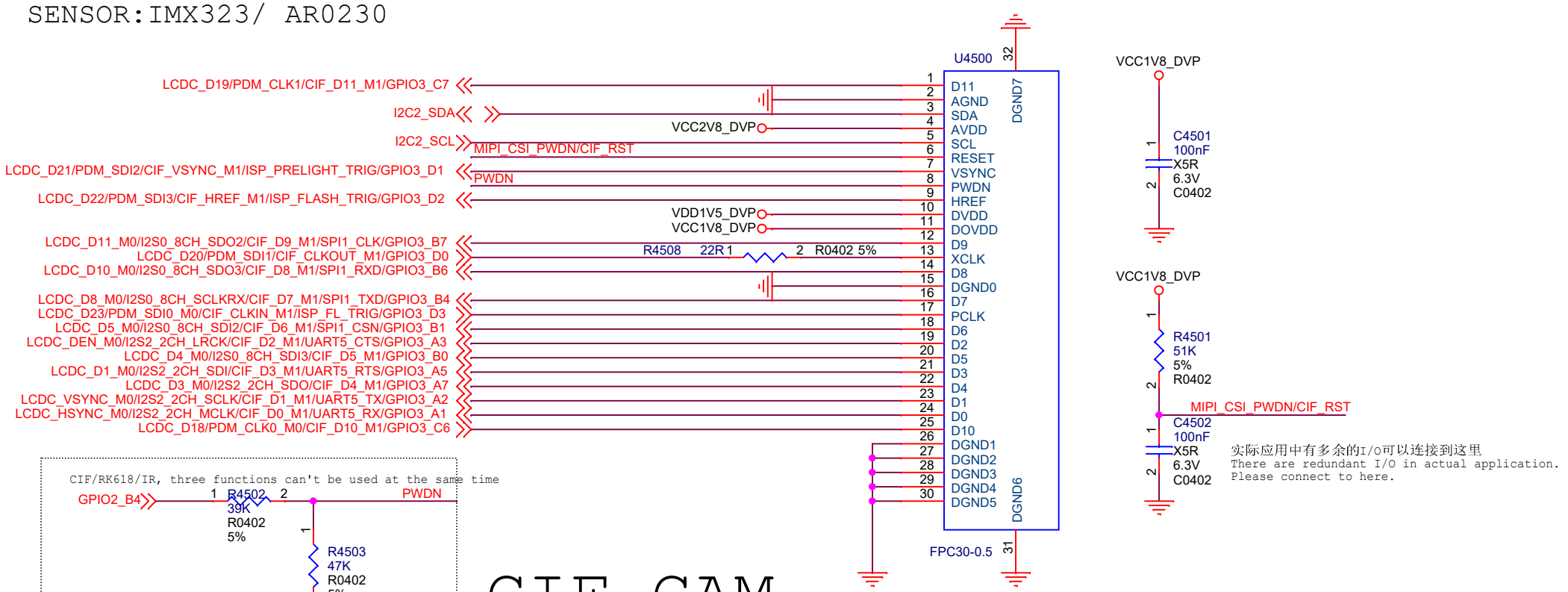


Note:
Short two TP points to Enter Maskrom Mode.

**Remind: Refer to the latest AVL for parts selection.**

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 42.Flash-SPI Flash(option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 25 of 44 |

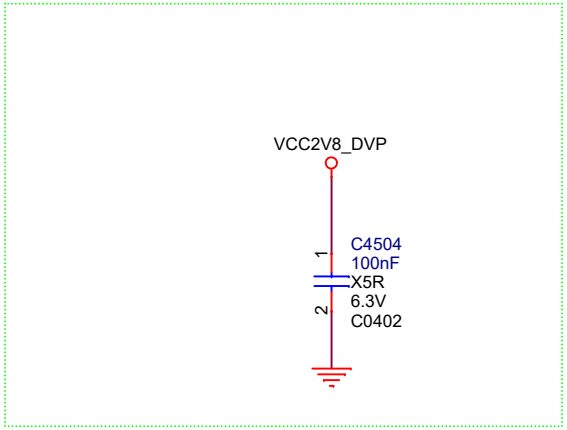
SENSOR:IMX323/ AR0230

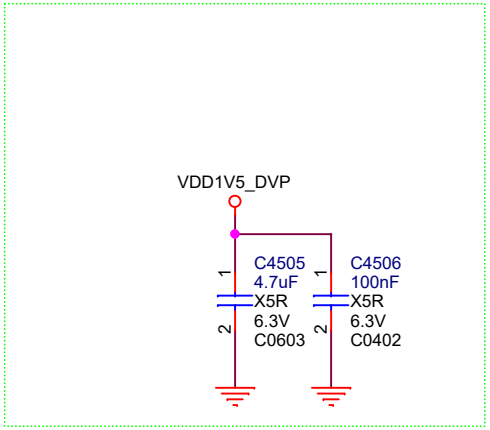






# CIF CAM





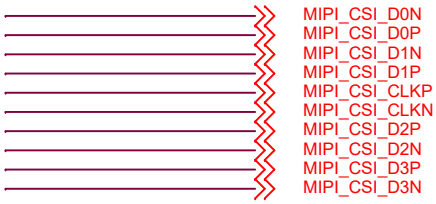


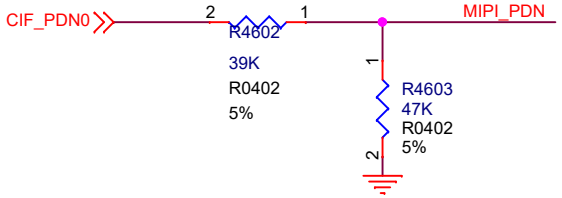


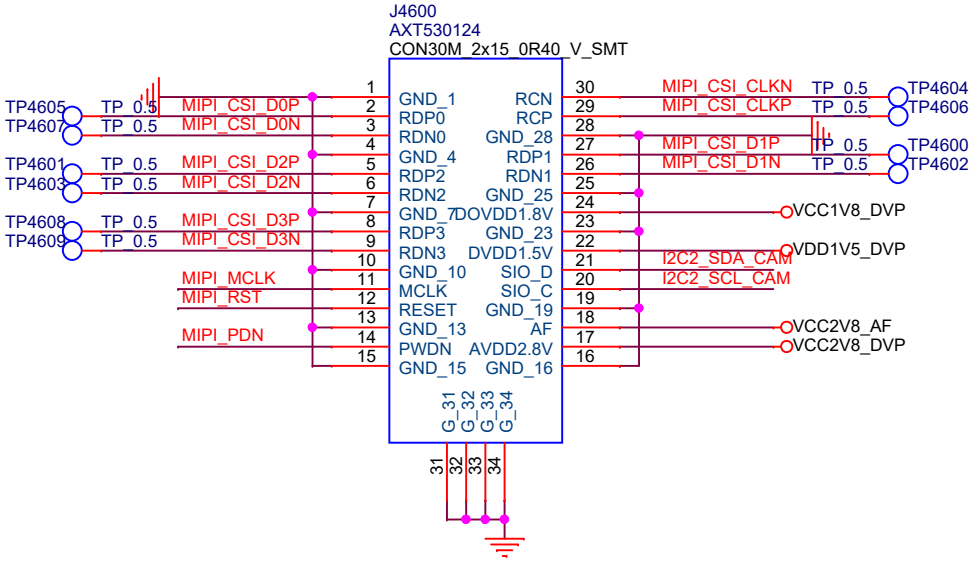

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 45.Camera-CIF (option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 26 of 44 |

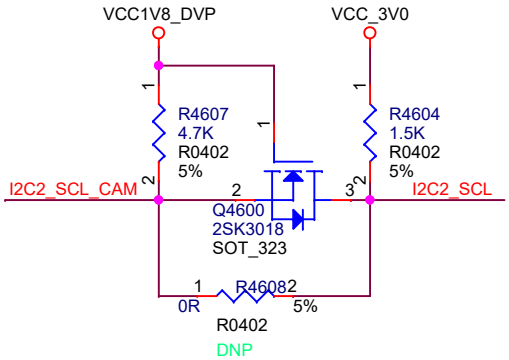
# MIPI Camera

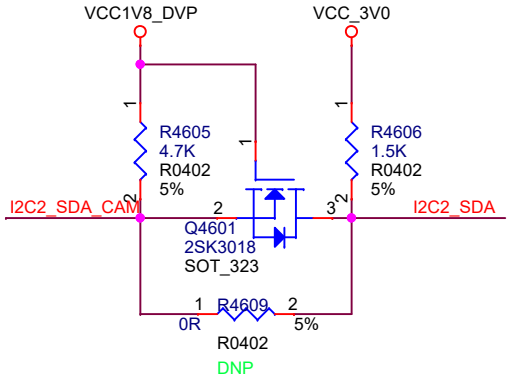


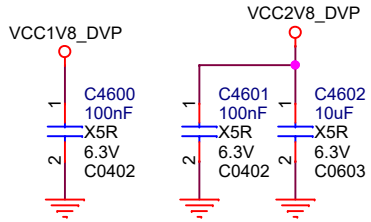


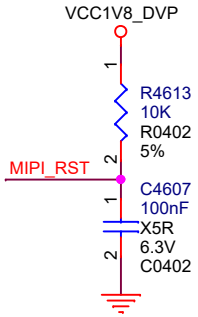



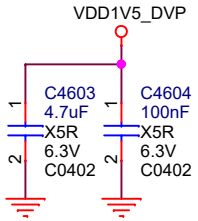



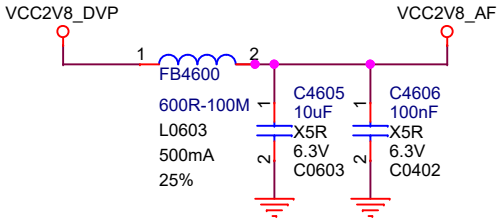










实际应用中有多余的I/O可以连接到这里
There are redundant I/O in actual application.
Please connect to here.

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 46.Camera-MIPI CSI | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 27 of 44 |

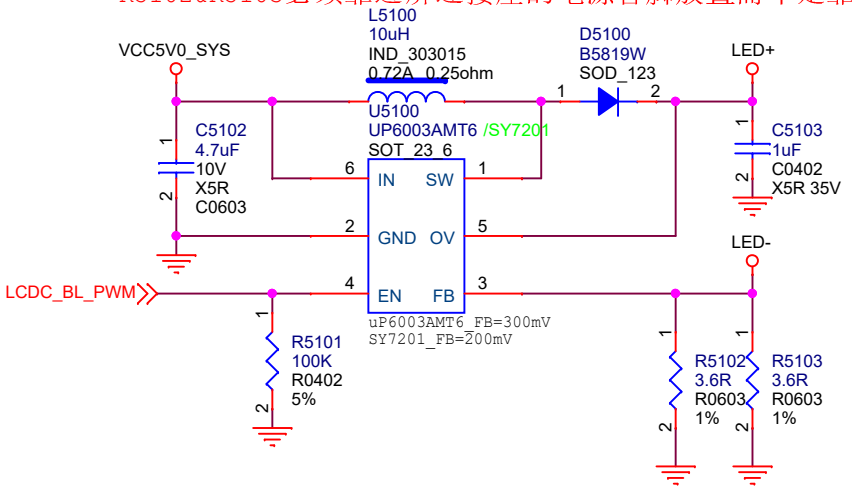
# LVDS Panel

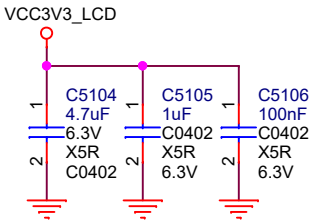
LCDC_D11_M1/LVDS_TX0N/MIPI_TX_D0N → LVDS/MIPI_TXD0N
LCDC_D8_M1/LVDS_TX0P/MIPI_TX_D0P → LVDS/MIPI_TXD0P
LCDC_D1_M1/LVDS_TX1N/MIPI_TX_D1N → LVDS/MIPI_TXD1N
LCDC_D10_M1/LVDS_TX1P/MIPI_TX_D1P → LVDS/MIPI_TXD1P
LCDC_D4_M1/LVDS_CLKN/MIPI_TX_CLKN → LVDS/MIPI_TXCLKN
LCDC_D3_M1/LVDS_CLKP/MIPI_TX_CLKP → LVDS/MIPI_TXCLKP
LCDC_VSYNC_M1/LVDS_TX2N/MIPI_TX_D2N → LVDS/MIPI_TXD2N
LCDC_D5_M1/LVDS_TX2P/MIPI_TX_D2P → LVDS/MIPI_TXD2P
LCDC_HSYNC_M1/LVDS_TX3N/MIPI_TX_D3N → LVDS/MIPI_TXD3N
LCDC_DEN_M1/LVDS_TX3P/MIPI_TX_D3P → LVDS/MIPI_TXD3P

LCD5100
B101EW04
FPC40-0.5A

| | | | |
|---|---|---|---|
| | | 1 | NC1 |
| VCC3V3_LCD | | 2 | AVDD1 |
| | | 3 | AVDD2 |
| | | 4 | NC2 |
| | | 5 | I2C_CLK_EDID |
| | | 6 | I2C_SDA_EDID |
| | | 7 | NC3 |
| TP5103 TP_0.7 / TP5102 TP_0.7 | LVDS/MIPI_TXD0N / LVDS/MIPI_TXD0P | 8 / 9 | RIN0- / RIN0+ |
| | | 10 | GND1 |
| TP5104 TP_0.7 / TP5105 TP_0.7 | LVDS/MIPI_TXD1N / LVDS/MIPI_TXD1P | 11 / 12 | RIN1- / RIN1+ |
| | | 13 | GND2 |
| TP5106 TP_0.7 / TP5107 TP_0.7 | LVDS/MIPI_TXD2N / LVDS/MIPI_TXD2P | 14 / 15 | RIN2- / RIN2+ |
| | | 16 | GND3 |
| TP5108 TP_0.7 / TP5109 TP_0.7 | LVDS/MIPI_TXCLKN / LVDS/MIPI_TXCLKP | 17 / 18 | CLKIN- / CLKIN+ |
| | | 19 | GND4 |
| TP5110 TP_0.7 / TP5111 TP_0.7 | LVDS/MIPI_TXD3N / LVDS/MIPI_TXD3P | 20 / 21 | RIN3- / RIN3+ |
| | | 22 | GND5 |
| | | 23 | NC4 |
| | | 24 | NC5 |
| | | 25 | GND6 |
| | | 26 | NC6 |
| | | 27 | Color_EN |
| | | 28 | CABC_EN |
| | | 29 | LED_PWM(I) |
| | | 30 | LED_PWM(O) |
| | | 31 | NC7 |
| LED- | | 32 | VLED_GND1 |
| | | 33 | VLED_GND2 |
| | | 34 | VLED_GND3 |
| | | 35 | VLED_GND4 |
| | | 36 | VLED_GND5 |
| | | 37 | VLED_GND6 |
| | | 38 | NC8 |
| LED+ | | 39 | VLED1 |
| | | 40 | VLED2 |

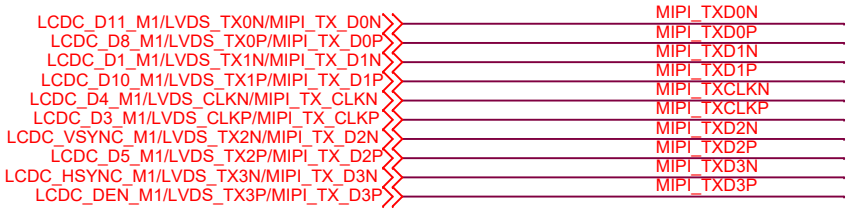
Note:
U5100 EN pin must support PWM brightness dimming control, Otherwise, it needs to be increased PWM circuit at FB pin.
R5102&R5103 should be placed close to the power pins of Panel Interface.
U5000的EN管脚需要能支持PWM动态背光调节功能，否则就需要在DCDC的FB管脚增加PWM电路来进行调节。
R5102&R5103必须靠近屏连接座的电源管脚放置而不是靠近DCDC放置。



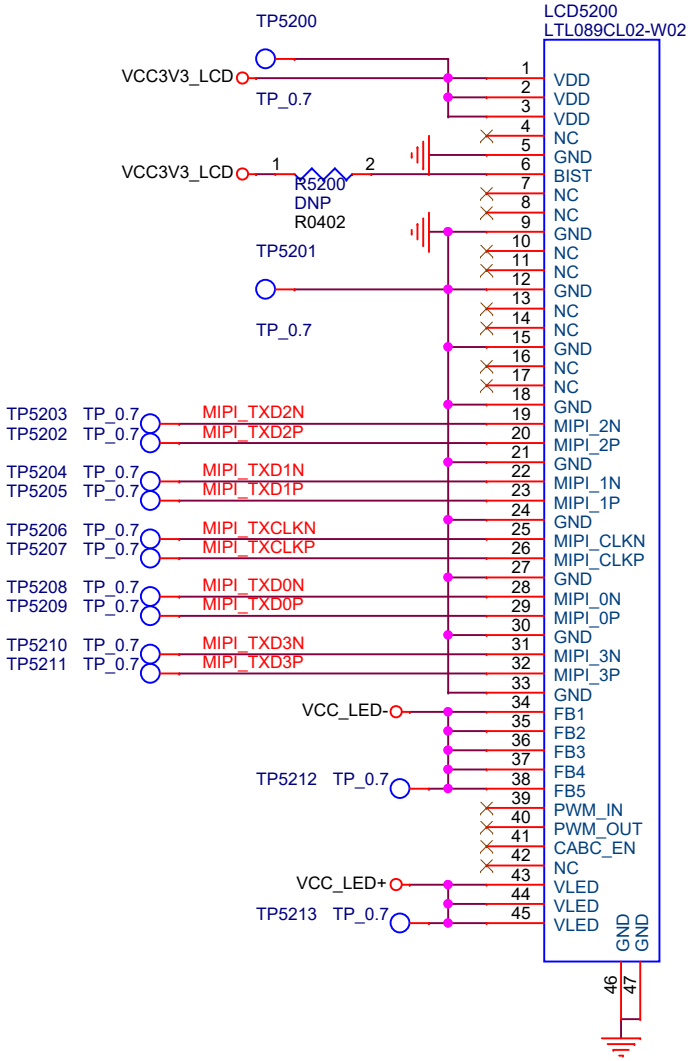



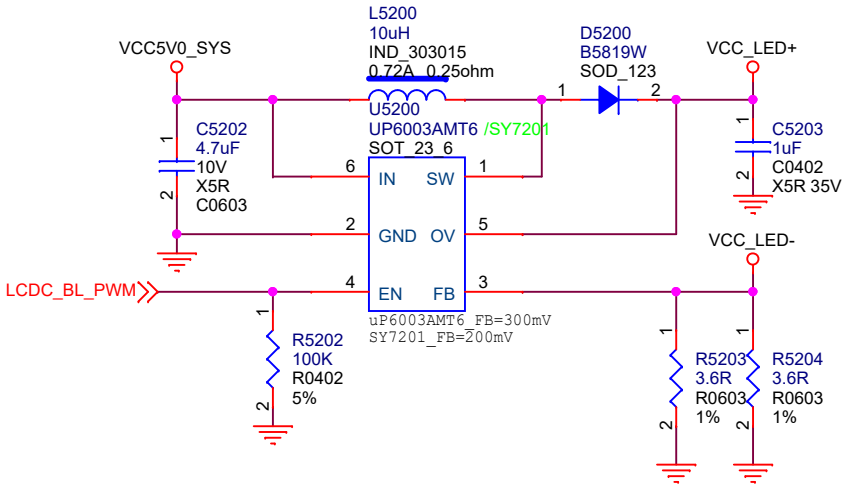

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 51.LCM-LVDS Panel(option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 28 of 44 |

# MIPI Panel

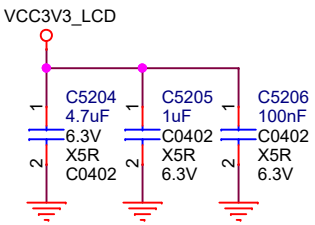



Note:
1.Use the MIPI output of RK618,please disconnect the RK3326.
2.If need to support of MIPI panel and HDMI with dual output same image,
must use the physical cross screen panel,for example 1280x800, not 800x1280
1.如果使用RK618的MIPI输出，则可以不用连接到RK3326的MIPI输出接口。
2.如果需要支持MIPI屏与HDMI的双屏同显，则必须使用物理横屏，
例如屏幕像素为1280x800而不是800x1280的



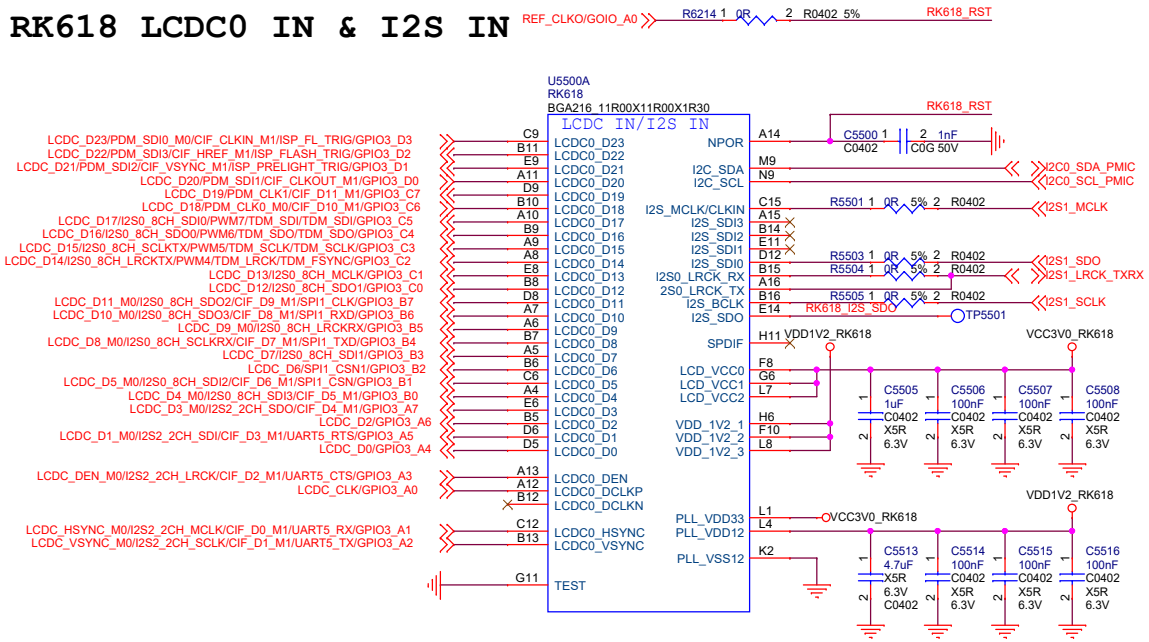



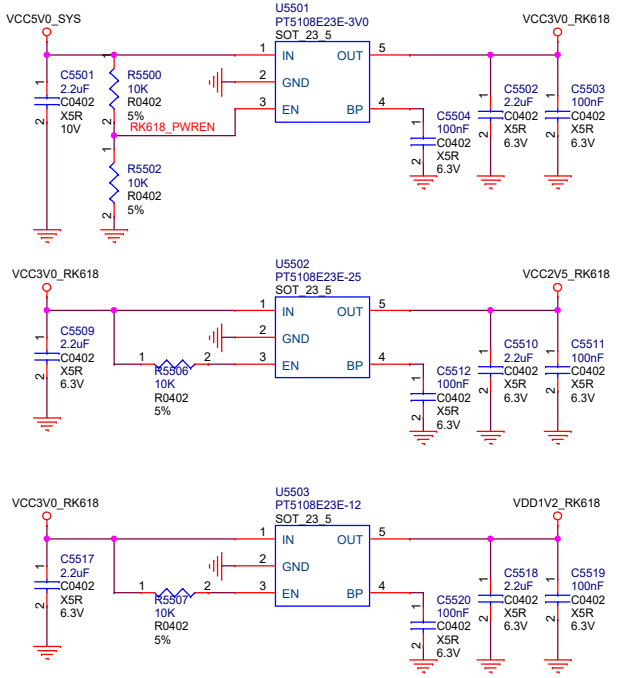

Note:
U5200 EN pin must support PWM brightness dimming control, Otherwise,
it needs to be increased PWM circuit at FB pin.
R5203&R5204 should be placed close to the power pins of Panel Interface.
U5000的EN管脚需要能支持PWM动态背光调节功能，
否则就需要在DCDC的FB管脚增加PWM电路来进行调节。
R5203&R5204必须靠近屏连接座的电源管脚放置而不是靠近DCDC放置。



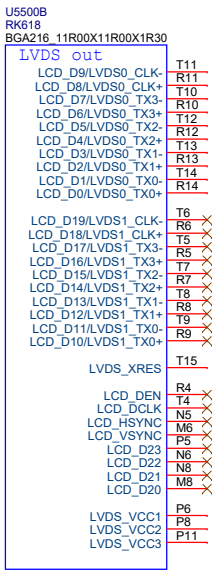

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 52.LCM-MIPI Panel | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 29 of 44 |

# RK618 LCDC0 IN & I2S IN

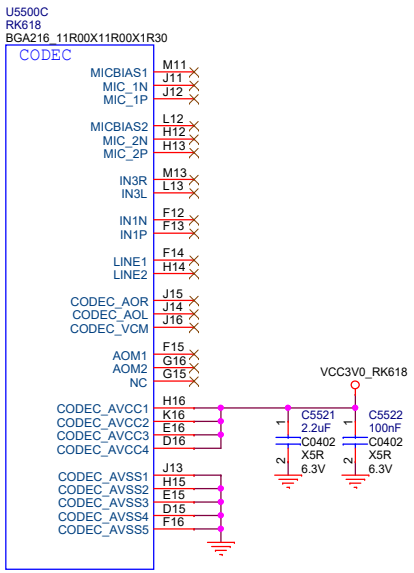


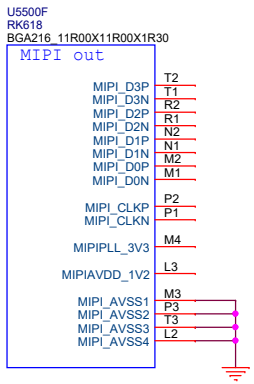

# RK618 LVDS output



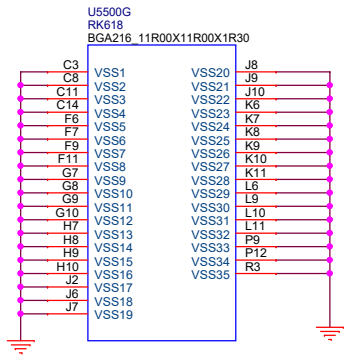

# RK618 Codec




# RK618 MIPI output

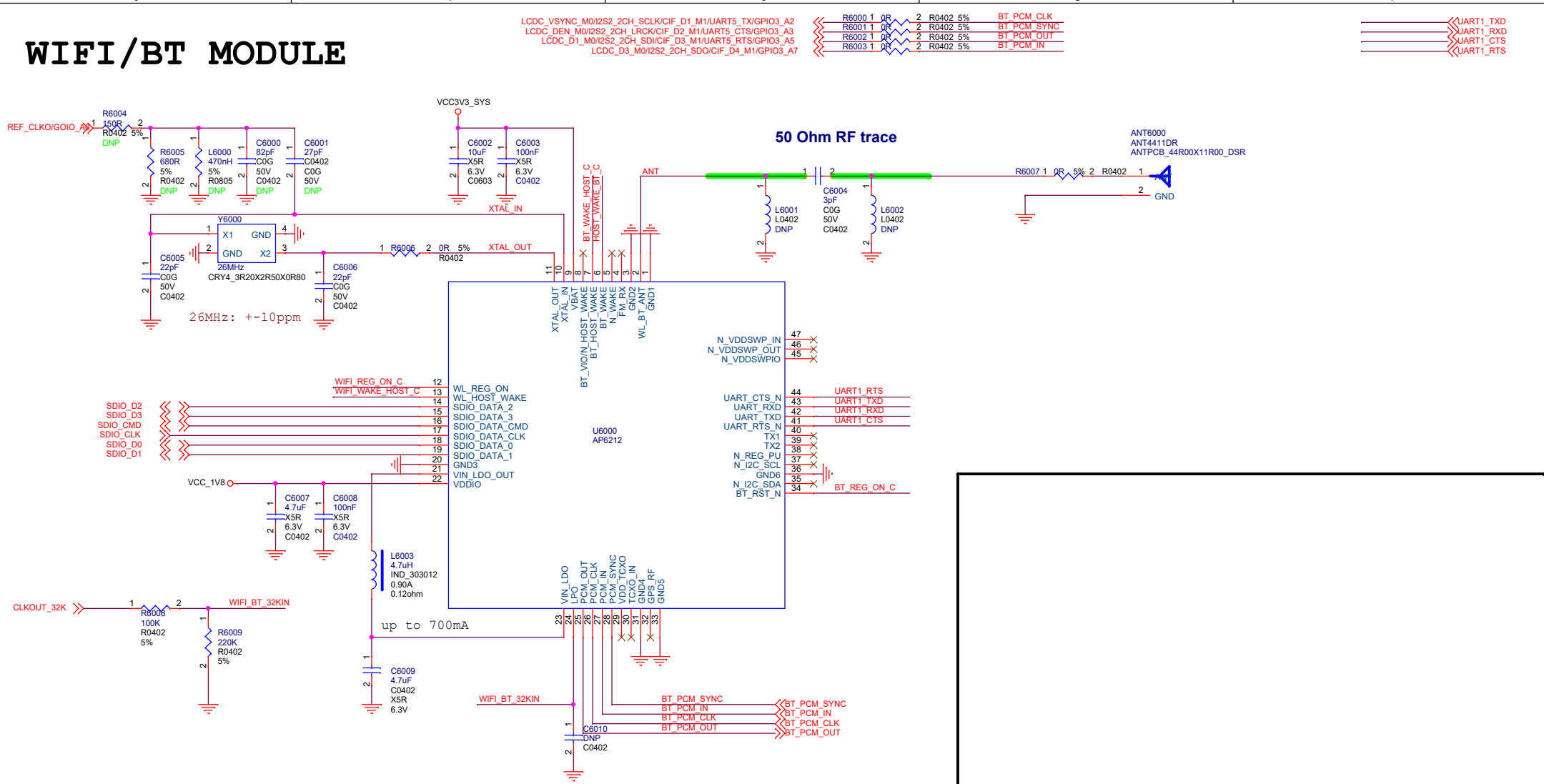



# RK618 MIPI output

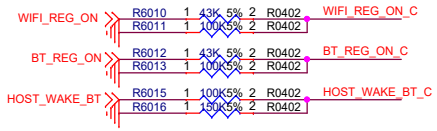


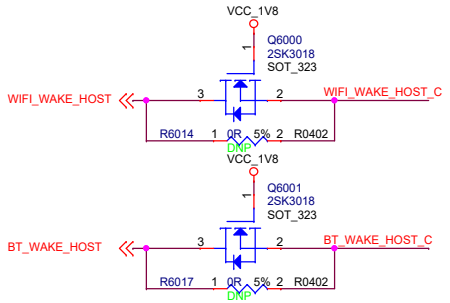

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 55.Video-RK618 | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 30 of 44 |

# WIFI/BT MODULE




## Level Shift




| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 60.SDIO WIFI/BT AP6212 | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 31 of 44 |

# WIFI/BT MODULE

LCDC_VSYNC_M0/I2S2_2CH_SCLK/CIF_D1_M1/UART5_TX/GPIO3_A2
LCDC_DEN_M0/I2S2_2CH_LRCK/CIF_D2_M1/UART5_CTS/GPIO3_A3
LCDC_D1_M0/I2S2_2CH_SDI/CIF_D3_M1/UART5_RTS/GPIO3_A5
LCDC_D3_M0/I2S2_2CH_SDO/CIF_D4_M1/GPIO3_A7

R6215 1 0R 2 R0402 5% BT_PCM_CLK
R6216 1 0R 2 R0402 5% BT_PCM_SYNC
R6217 1 0R 2 R0402 5% BT_PCM_OUT
R6218 1 0R 2 R0402 5% BT_PCM_IN

VCC3V3_SYS — R6200 1 0R 5% 2 R0603 — VCC_WL

HOST_WAKE_BT
BT_WAKE_HOST

Note:
1.F23BDSM23-W2 VCC_WL=3.2~3.6V
F23BDSM25-W1 VCC_WL=3.5~5.0V
2.VBAT voltage range is 3.2V-3.6V, and peak-current is at least 400mA.

**RF Microstrip**
**Z0= 50 ohm**

VCC_WL

C6203 10uF C0603 X5R 6.3V
C6204 10uF C0603 X5R 6.3V
C6205 100nF C0402 X5R 6.3V

L6200 2.2nH L0402

C6206 1.2pF C0402 C0G 50V
C6207 1pF C0402 C0G 50V

ANT6200 ANT_JACK ANT_JACK
GND1
GND2

BT_WAKE_HOST_CC
HOST_WAKE_BT_CC

U6200
F23BDSM23-W2_RTL8723BS12

WL_XTAL_OUT
WL_XTAL_IN
VBAT
NC
BT_HOST_WAKE
BT_WAKE
NC6
NC5
GND
WL_BT_ANT
GND5

WIFI_REG_ON_CC
WIFI_WAKE_HOST_CC
SDIO_D2
SDIO_D3
SDIO_CMD
SDIO_CLK
SDIO_D0
SDIO_D1

WL_REG_ON
WL_HOST_WAKE
SDIO_DATA_2
SDIO_DATA_3
SDIO_DATA_CMD
SDIO_DATA_CLK
SDIO_DATA_0
SDIO_DATA_1
GND1
VIN_LDO_OUT
VDDIO

TP3(NC)
TP2(NC)
TP1(NC)
UART_CTS_N
UART_RXD
UART_TXD
UART_RTS_N
NC4
NC3
BT_XTAL_OUT
BT_XTAL_IN
GND4
NC2
BT_RST_N

UART1_RTS
UART1_TXD
UART1_RXD
UART1_CTS
BT_REG_ON_CC

VCC_1V8
C6208 4.7uF C0402 X5R 6.3V
C6209 100nF C0402 X5R 6.3V

VIN_LDO
LPO
PCM_OUT
PCM_CLK
PCM_IN
PCM_SYNC
WL_VDD_TCXO
TCXO_IN
GND2
NC1
GND3

CLKOUT_32K
R6210 1 100K 5% 2 R0402
R6212 220K 5% R0402
C6210 DNP C0402

BT_PCM_SYNC
BT_PCM_IN
BT_PCM_CLK
BT_PCM_OUT

## Level Shift

WIFI_REG_ON
R6203 1 43K 5% 2 R0402
R6204 1 100K 5% 2 R0402
WIFI_REG_ON_CC

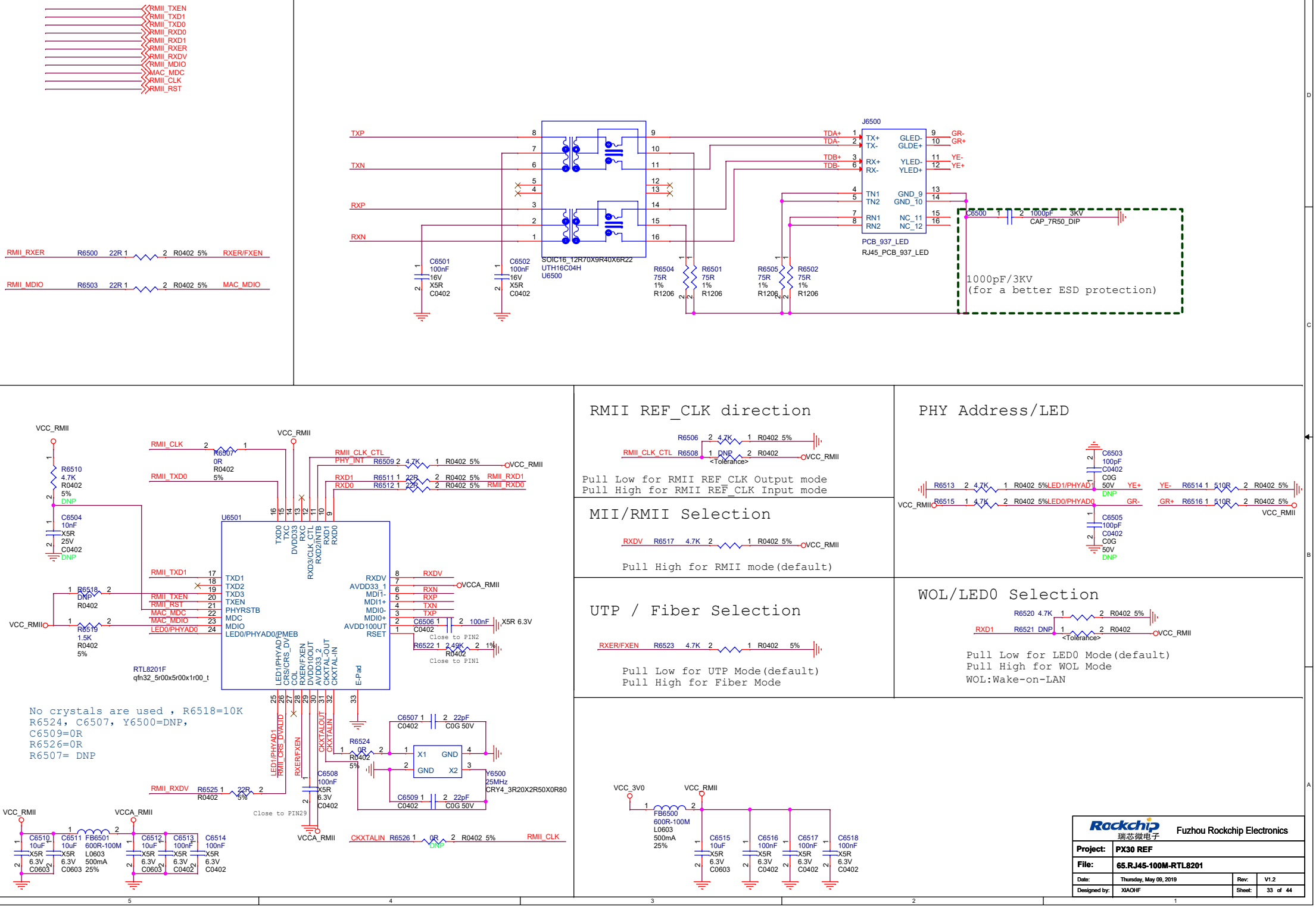
BT_REG_ON
R6205 1 43K 5% 2 R0402
R6206 1 100K 5% 2 R0402
BT_REG_ON_CC

HOST_WAKE_BT
R6207 1 100K 5% 2 R0402
R6208 1 150K 5% 2 R0402
HOST_WAKE_BT_CC

VCC_1V8
Q6201 2SK3018 SOT_323
WIFI_WAKE_HOST
R6209 1 0R 5% 2 R0402 DNP
WIFI_WAKE_HOST_CC

VCC_1V8
Q6202 2SK3018 SOT_323
BT_WAKE_HOST
R6211 1 0R 5% 2 R0402 DNP
BT_WAKE_HOST_CC

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 62.SDIO WIFI/BT-RTL8723(option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 32 of 44 |


RMII_TXEN
RMII_TXD1
RMII_TXD0
RMII_RXD0
RMII_RXD1
RMII_RXER
RMII_RXDV
RMII_MDIO
MAC_MDC
RMII_CLK
RMII_RST
RMII_RXER R6500 22R 1 2 R0402 5% RXER/FXEN
RMII_MDIO R6503 22R 1 2 R0402 5% MAC_MDIO
TXP
TXN
RXP
RXN
C6501 100nF 16V X5R C0402
C6502 100nF 16V X5R C0402
SOIC16_12R70X9R40X6R22
UTH16C04H
U6500
R6504 75R 1% R1206
R6501 75R 1% R1206
R6505 75R 1% R1206
R6502 75R 1% R1206
J6500
TDA+
TDA-
TDB+
TDB-
TX+
TX-
RX+
RX-
GLED-
GLDE+
YLED-
YLED+
TN1
TN2
RN1
RN2
GND_9
GND_10
NC_11
NC_12
PCB_937_LED
RJ45_PCB_937_LED
C6500 1 2 1000pF 3KV
CAP_7R50_DIP
1000pF/3KV
(for a better ESD protection)
VCC_RMII
R6510 4.7K R0402 5% DNP
C6504 10nF X5R 25V C0402 DNP
RMII_CLK
R6507 0R R0402 5%
RMII_TXD0
RMII_CLK_CTL
PHY_INT
R6509 4.7K R0402 5%
RXD1
RXD0
R6511 22R R0402 5%
R6512 22R R0402 5%
RMII_RXD1
RMII_RXD0
U6501
TXD0
TXC
DVDD33
RXC
RXD3/CLK_CTL
RXD2/INTB
RXD1
RXD0
RMII_TXD1
RMII_TXEN
RMII_RST
MAC_MDC
LED0/PHYAD0
R6518 DNP R0402
R6519 1.5K R0402 5%
TXD1
TXD2
TXD3
TXEN
PHYRSTB
MDC
MDIO
LED0/PHYAD0/PMEB
RXDV
AVDD33_1
MDI1-
MDI1+
MDIO-
MDIO+
AVDD100UT
RSET
VCCA_RMII
C6506 100nF X5R 6.3V C0402
Close to PIN2
R6522 2.49K R0402 1%
Close to PIN1
RTL8201F
qfn32_5r00x5r00x1r00_t
LED1/PHYAD1
CRS/CRS_DV
COL
RXER/FXEN
DVDD10OUT
AVDD33_2
CKXTAL-OUT
CKXTAL-IN
E-Pad
No crystals are used , R6518=10K
R6524, C6507, Y6500=DNP,
C6509=0R
R6526=0R
R6507= DNP
C6507 22pF C0402 C0G 50V
R6524 0R R0402 5%
X1
X2
GND
Y6500 25MHz CRY4_3R20X2R50X0R80
C6509 22pF C0402 C0G 50V
C6508 100nF X5R 6.3V C0402
RMII_RXDV
R6525 22R R0402 5%
Close to PIN29
CKXTALIN
R6526 0R DNP
RMII_CLK
VCC_RMII
VCCA_RMII
C6510 10uF X5R 6.3V C0603
C6511 10uF X5R 6.3V C0603
FB6501 600R-100M L0603 500mA 25%
C6512 10uF X5R 6.3V C0603
C6513 100nF X5R 6.3V C0402
C6514 100nF X5R 6.3V C0402
RMII REF_CLK direction
R6506 4.7K R0402 5%
RMII_CLK_CTL R6508 DNP R0402
<Tolerance>
Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode
MII/RMII Selection
RXDV R6517 4.7K R0402 5%
Pull High for RMII mode(default)
UTP / Fiber Selection
RXER/FXEN R6523 4.7K R0402 5%
Pull Low for UTP Mode(default)
Pull High for Fiber Mode
PHY Address/LED
R6513 4.7K R0402 5% LED1/PHYAD1 YE+
R6515 4.7K R0402 5% LED0/PHYAD0 GR-
C6503 100pF C0G 50V C0402 DNP
C6505 100pF C0G 50V C0402 DNP
YE- R6514 510R R0402 5%
GR+ R6516 510R R0402 5%
WOL/LED0 Selection
R6520 4.7K R0402 5%
RXD1 R6521 DNP R0402
<Tolerance>
Pull Low for LED0 Mode(default)
Pull High for WOL Mode
WOL:Wake-on-LAN
VCC_3V0
FB6500 600R-100M L0603 500mA 25%
C6515 10uF X5R 6.3V C0603
C6516 100nF X5R 6.3V C0402
C6517 100nF X5R 6.3V C0402
C6518 100nF X5R 6.3V C0402
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: PX30 REF
File: 65.RJ45-100M-RTL8201
Date: Thursday, May 09, 2019
Rev: V1.2
Designed by: XIAOHF
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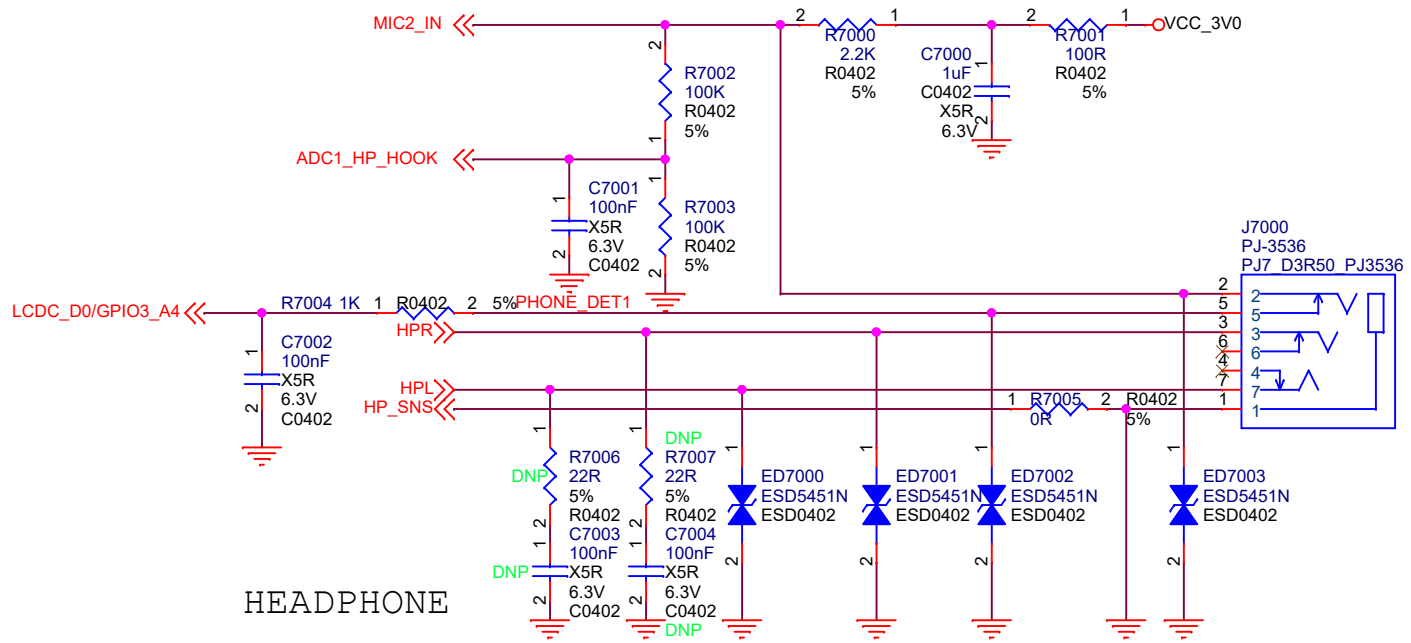
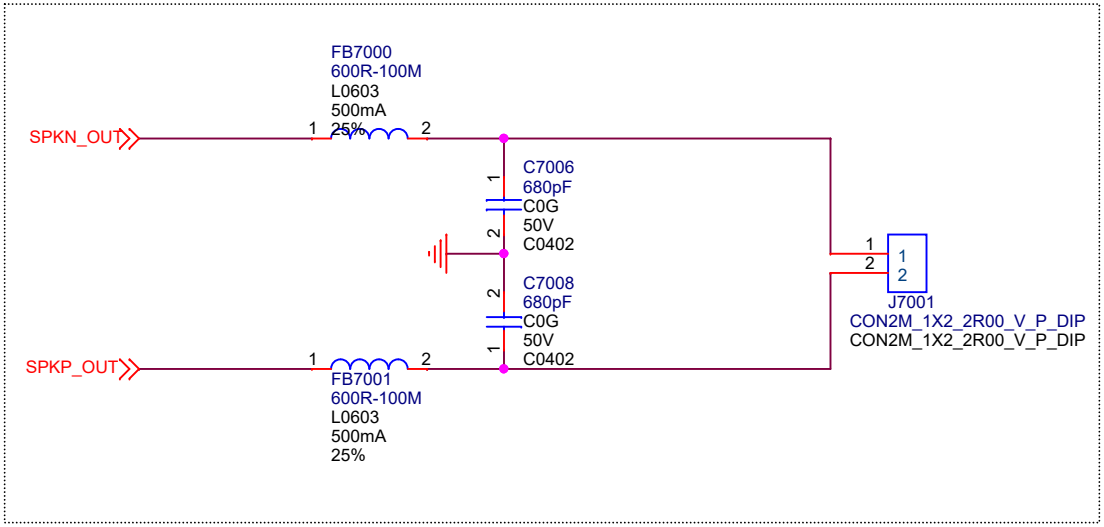
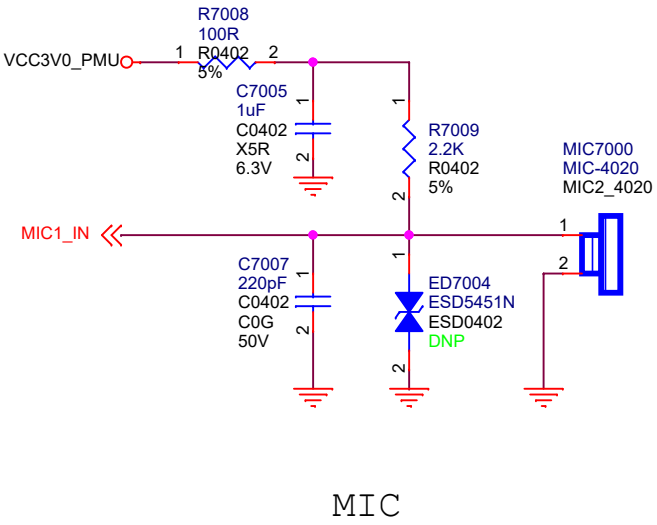
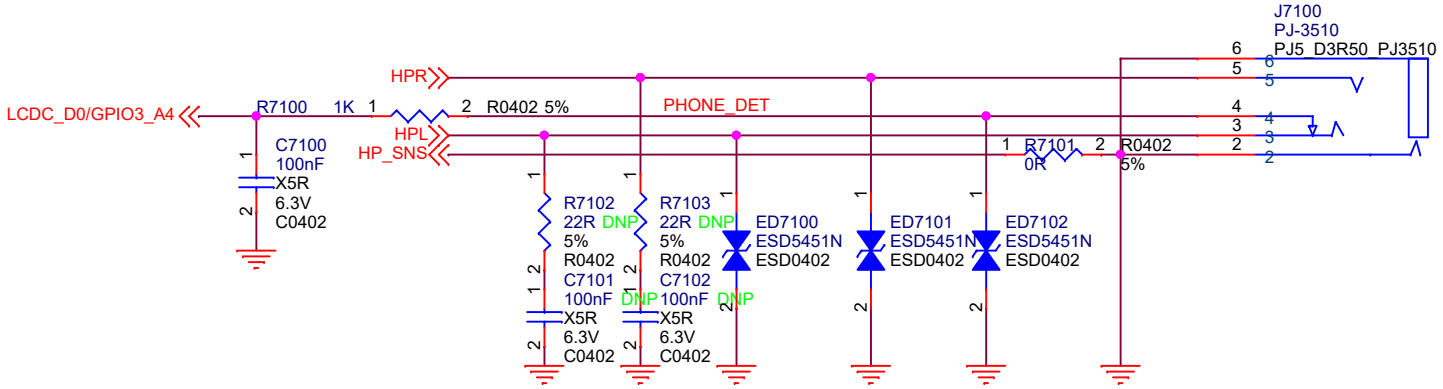


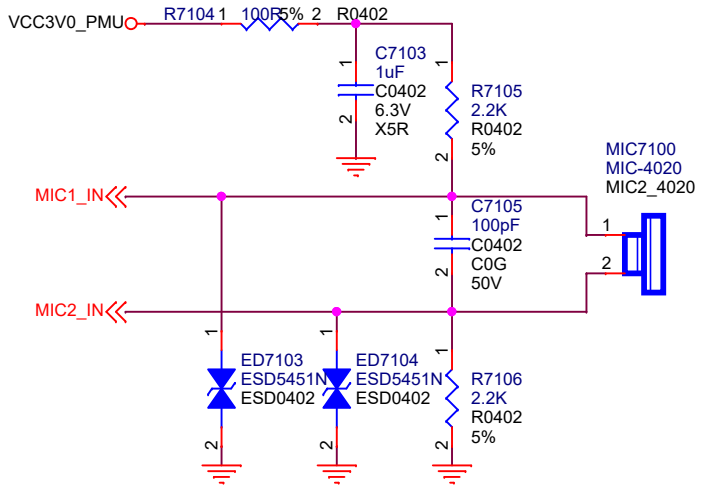




| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 70.AUDIO1 | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 34 of 44 |

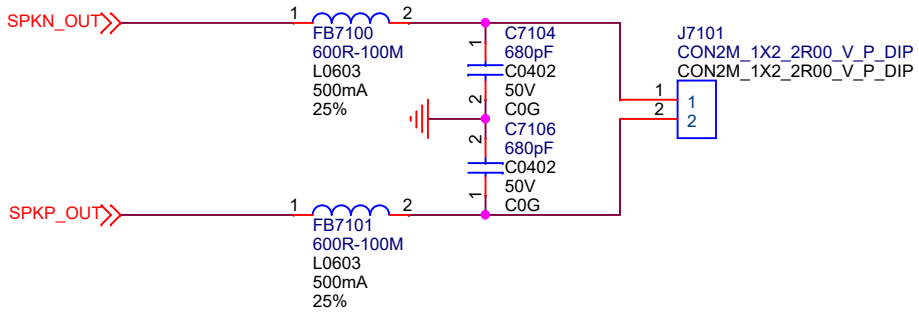
# Headphone




# Microphone

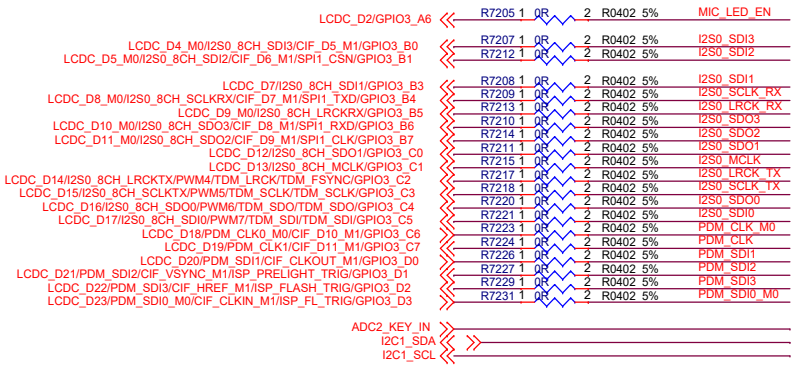



# Speaker



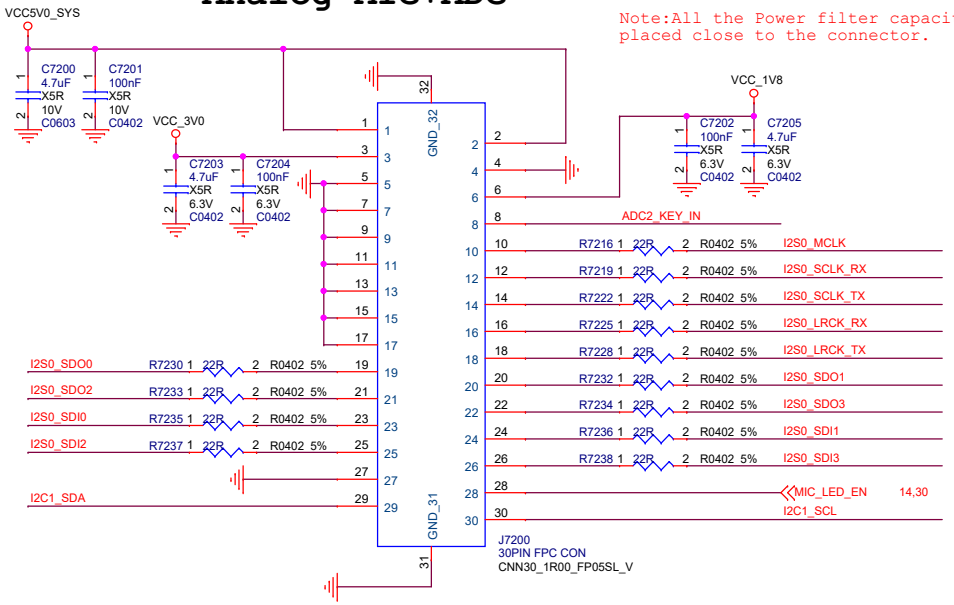

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 71.AUDIO2(option) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 35 of 44 |

# MIC Array-Digital Interface

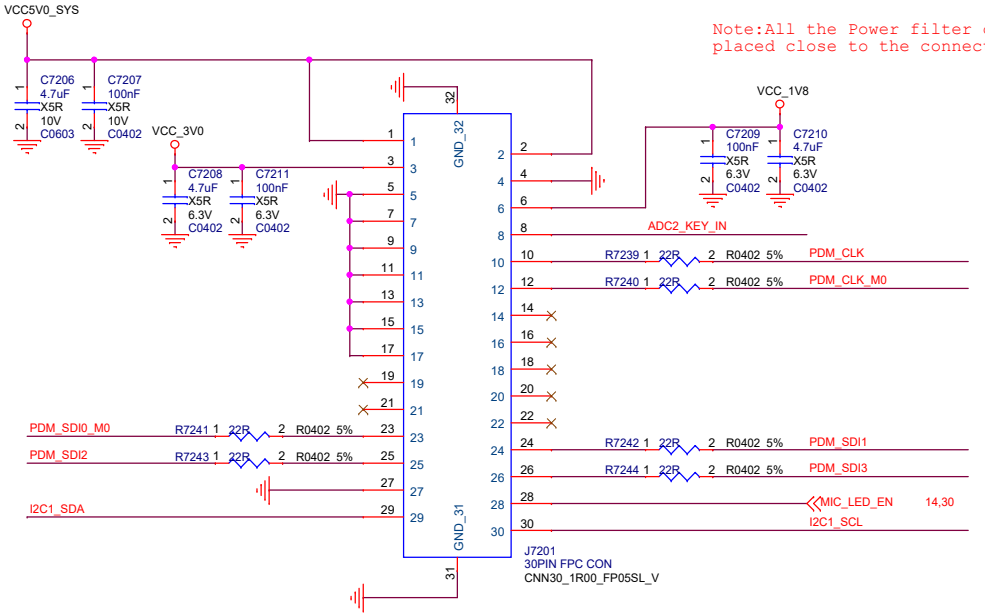



## I2S(Option)
## Support I2S MIC or Analog MIC+ADC

Note:All the Power filter capacitors should be placed close to the connector.



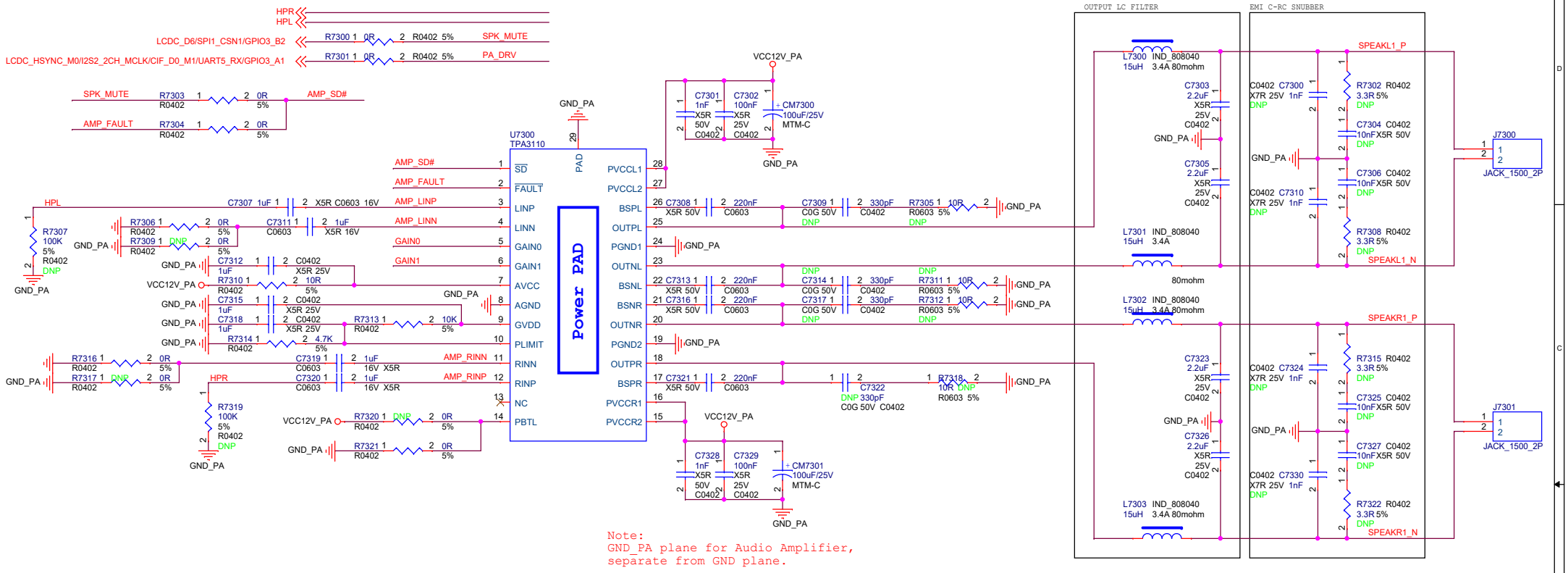

Note:All the Power filter capacitors should be placed close to the connector.




## PDM(Default)

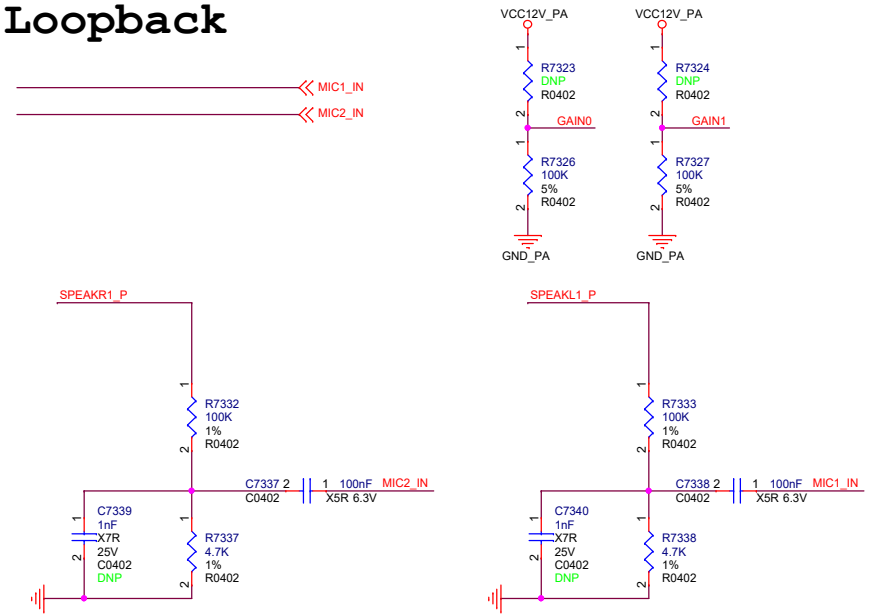
| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 72_AUDIO-MIC Array Connector | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 36 of 44 |

# AUDIO_AnalogAmp

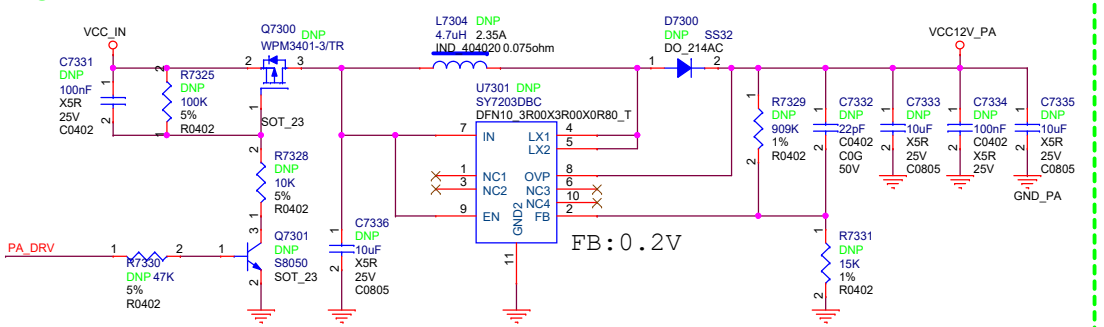



Note:
GND_PA plane for Audio Amplifier,
separate from GND plane.

# Loopback

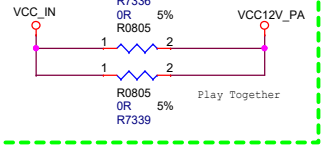



## OPTION 2




## POWER

### OPTION 1




| | Only DC IN Without Battery (Default) | With Battery |
|---|---|---|
| Option1 | Be mounted | Not be mounted |
| Option2 | Not be mounted | Be mounted |

R7334 0R R0805 5%
R7335 0R R0805 5%
Place Together
GND_PA

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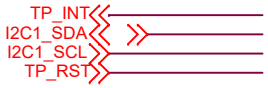
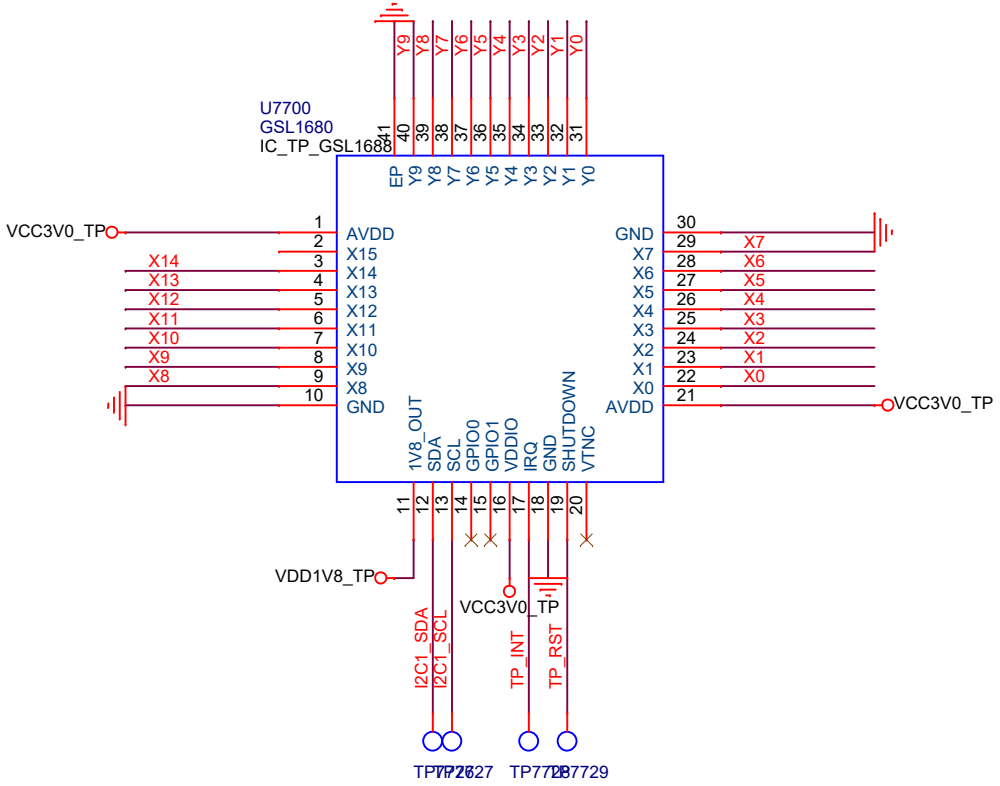
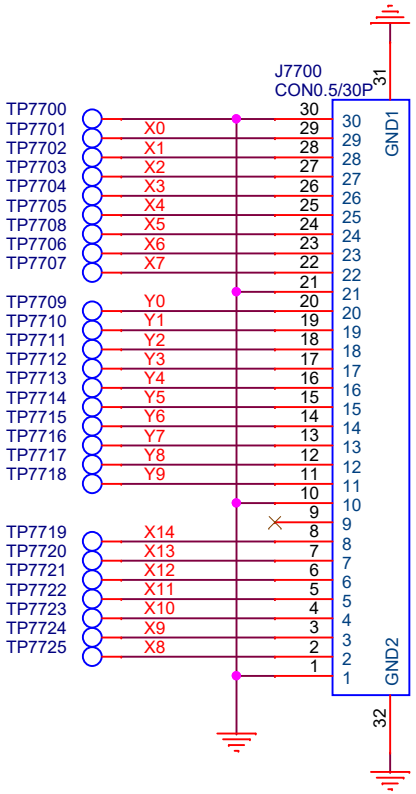
| | | | |
|---|---|---|---|
| Project: | PX30 REF | | |
| File: | 73.AUDIO-AnalogAmp_TPA3110 | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 37 of 44 |

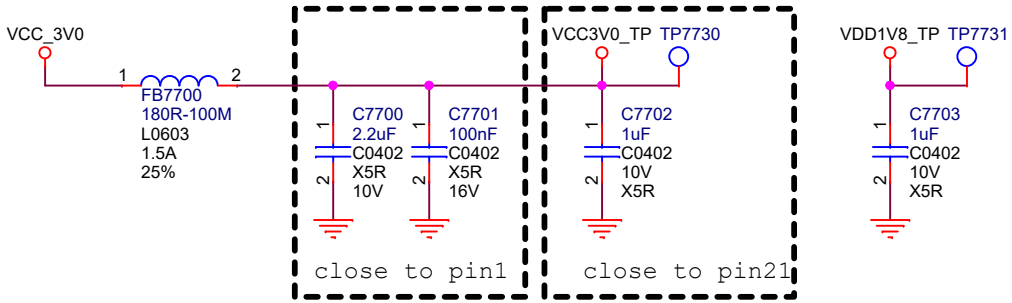
# TP COB GSL1680

Note:16x10 channel,suit for Touch Panel size≤10''



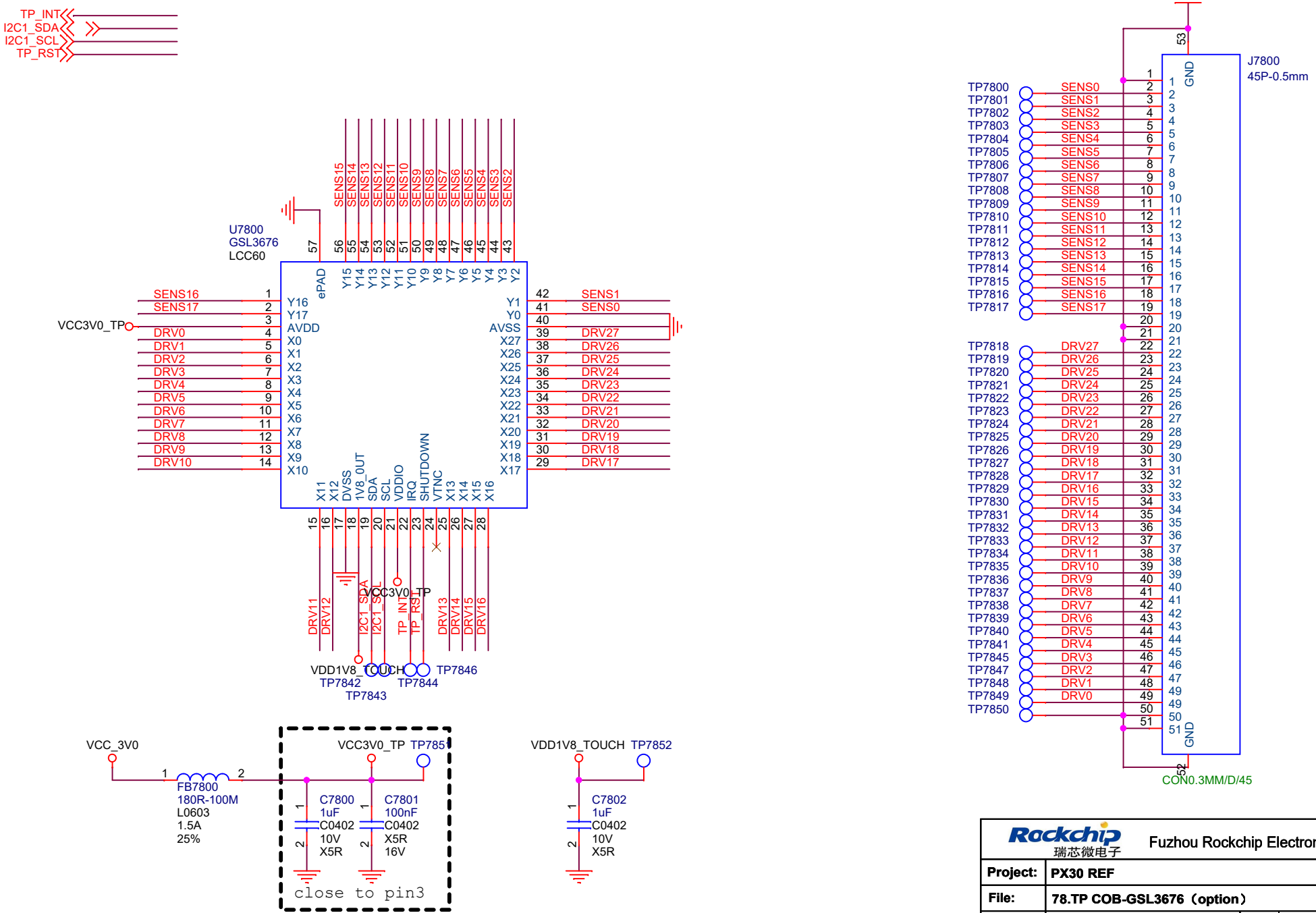




| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 77.TP COB-GSL1680 | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XHF | Sheet: | 38 of 44 |

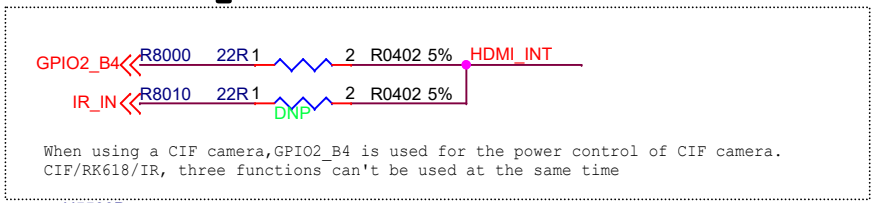
# TP COB GSL3676

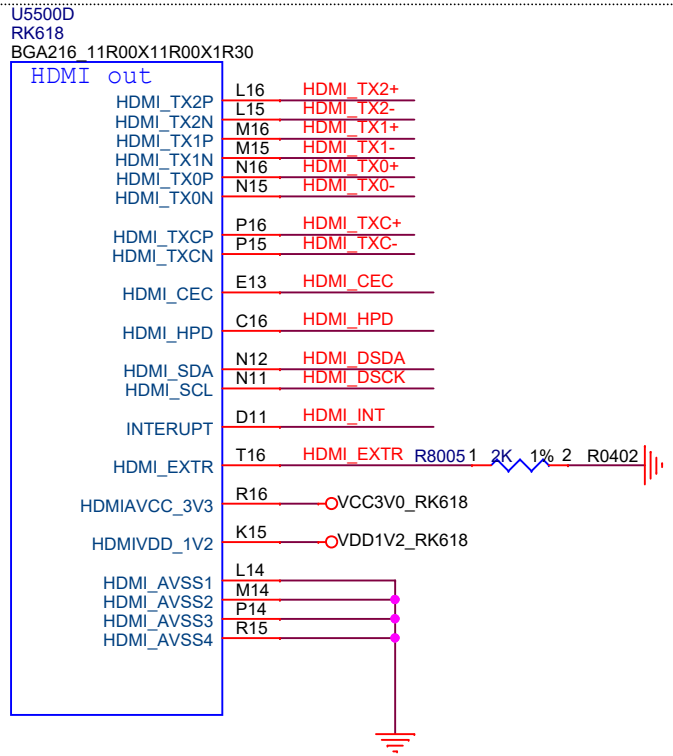
Note:26x14 channel,suit for Touch Panel size≤12''

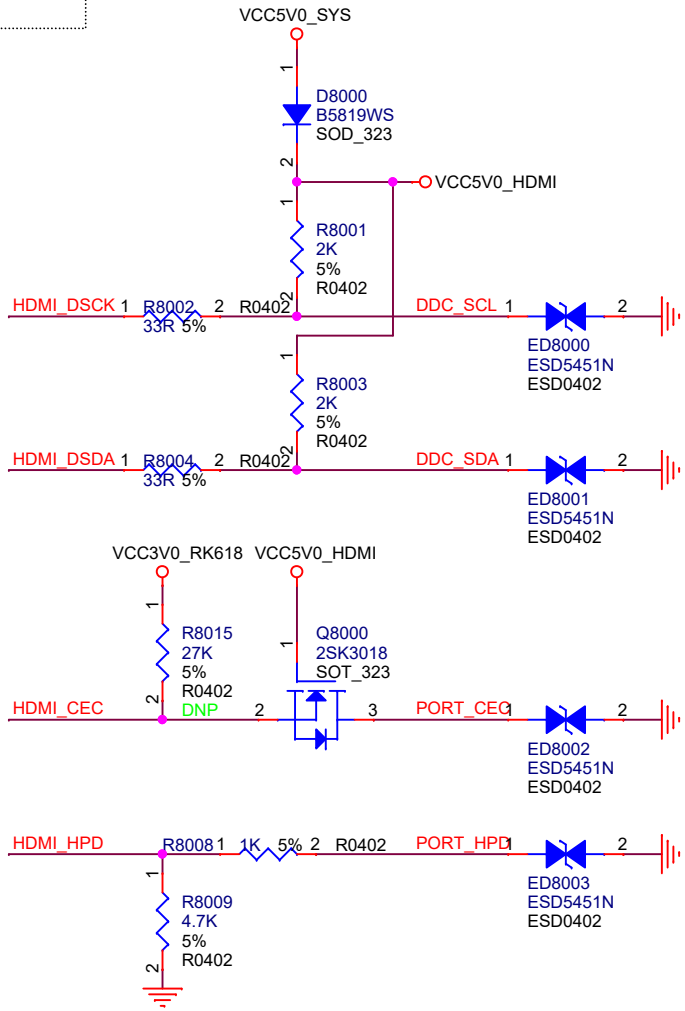


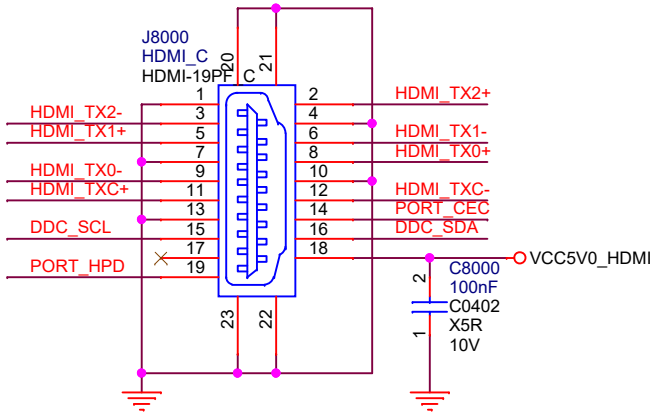

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 78.TP COB-GSL3676（option） | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XHF | Sheet: | 39 of 44 |

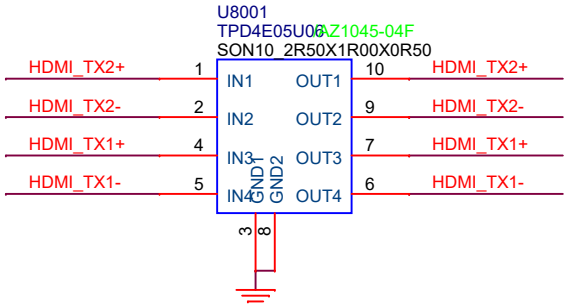
# HDMI Output

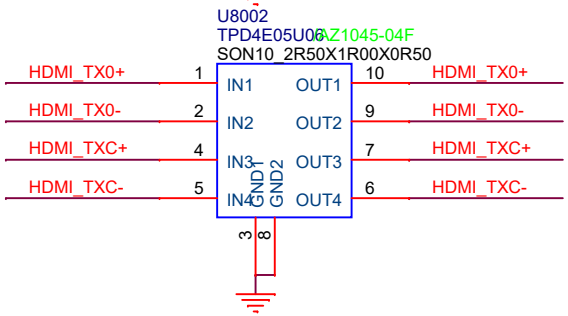


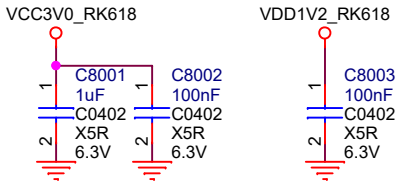



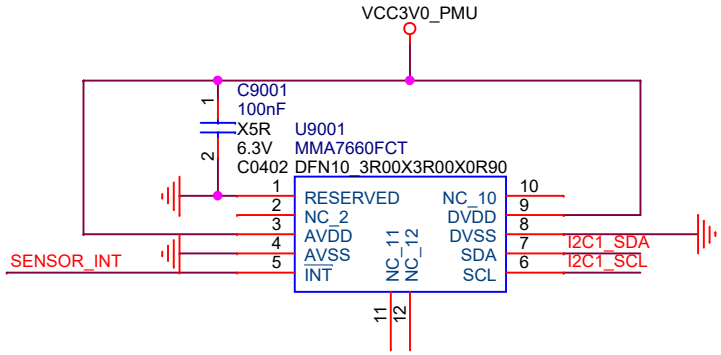




| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 80.HDMI Output(RK618) | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 40 of 44 |

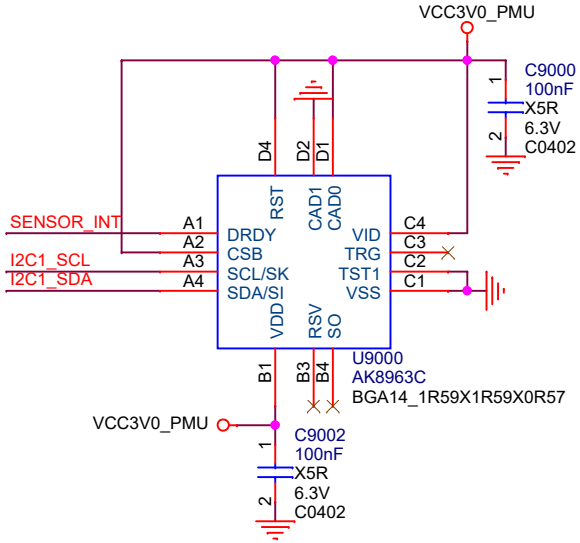
I2C1_SDA
I2C1_SCL
SENSOR_INT

# G-sensor



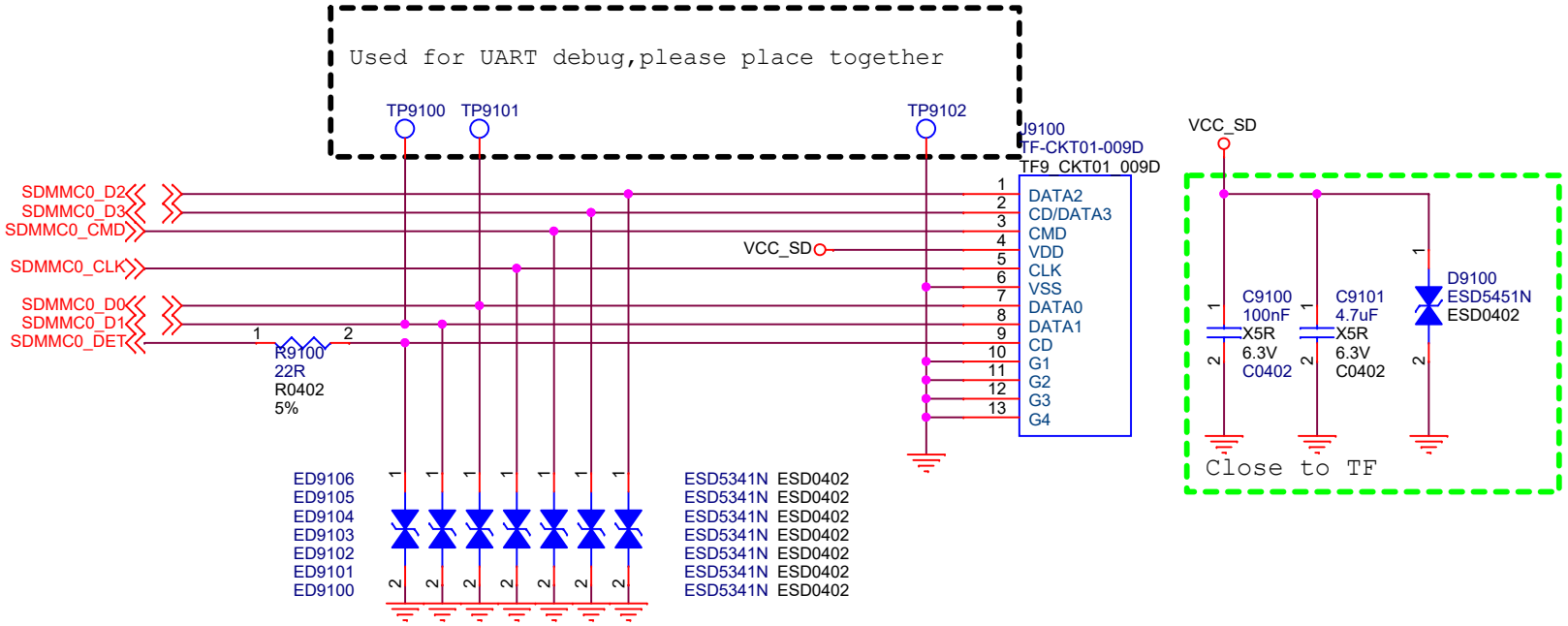

# Compass

Note:
The first pin of AK8963C must be place on the lower left corner of PCB.



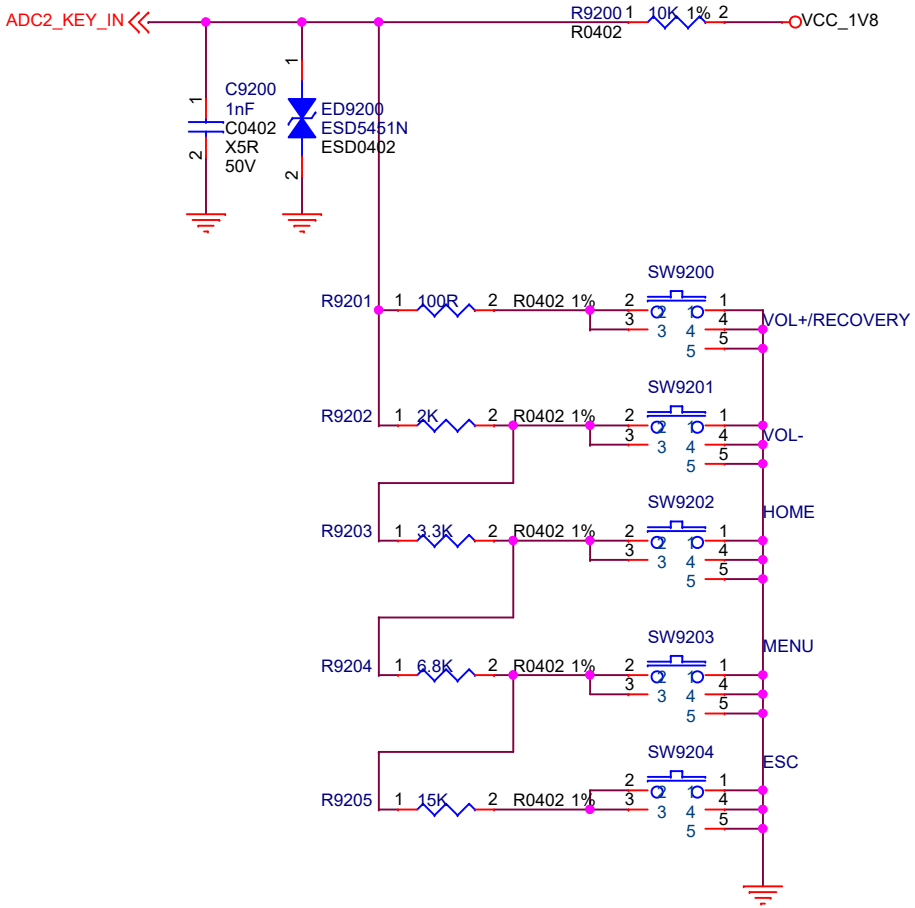

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 90.Sensor | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 41 of 44 |

# TF Card



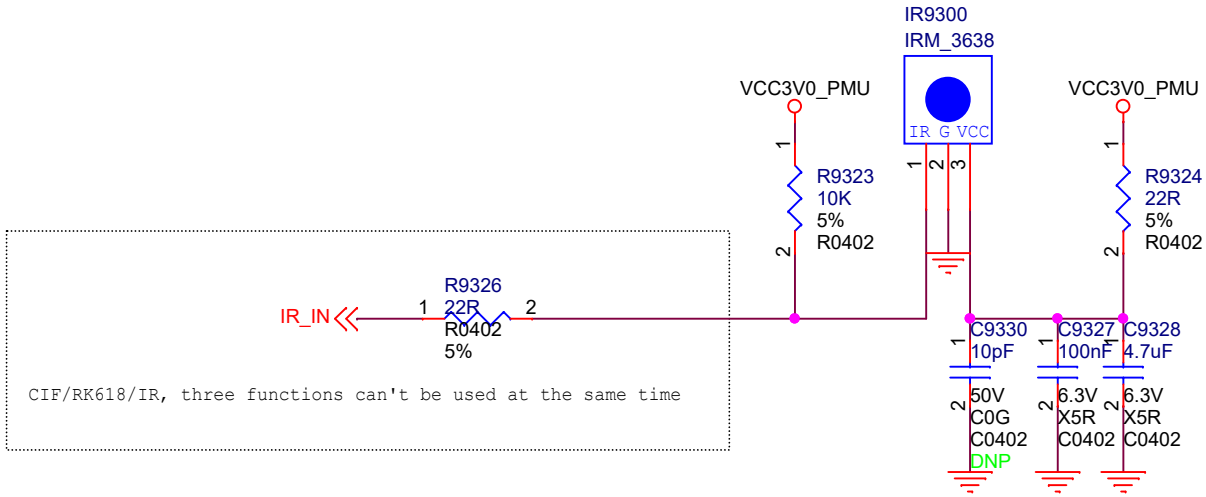

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 91.TF Card | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 42 of 44 |

# KEY BAORD




| Key Name | SARADC |
|---|---|
| VOL+/RECOVERY | 10 |
| VOL- | 170 |
| HOME | 354 |
| MENU | 560 |
| ESC | 747 |

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| Project: | PX30 REF | | |
| File: | 92.KEY Board | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 43 of 44 |




# IR Receiver

| | | | |
|---|---|---|---|
| Rockchip 瑞芯微电子 | Fuzhou Rockchip Electronics | | |
| **Project:** | **PX30 REF** | | |
| **File:** | **93.IR** | | |
| Date: | Thursday, May 09, 2019 | Rev: | V1.2 |
| Designed by: | XIAOHF | Sheet: | 44 of 44 |